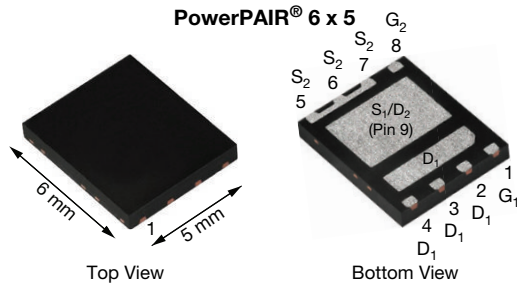


Dual N-Channel 30 V (D-S) MOSFET With Schottky Diode



FEATURES

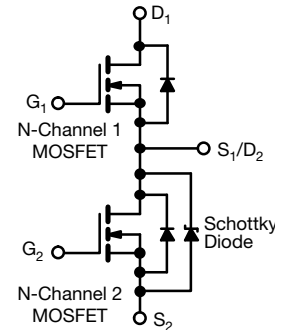
- TrenchFET® Gen IV power MOSFET
- SkyFET® low side MOSFET with integrated Schottky
- Very low $R_{DS(on)} \times Q_g$ FOM improves efficiency
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- CPU core power
- Computer / server peripherals
- POL
- Synchronous buck converter
- Telecom DC/DC



PRODUCT SUMMARY		
	CHANNEL-1	CHANNEL-2
V_{DS} (V)	30	30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00439	0.0024
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.00712	0.0038
Q_g typ. (nC)	5.7	14.6
I_D (A) ^a	54.8	94.6
Configuration	Dual plus integrated Schottky (SkyFET)	

ORDERING INFORMATION	
Package	PowerPAIR 6 x 5
Lead (Pb)-free and halogen-free	SiZ998BDT-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)					
PARAMETER	SYMBOL	CHANNEL-1	CHANNEL-2	UNIT	
Drain-source voltage	V_{DS}	30	30	V	
Gate-source voltage	V_{GS}	+20, -16	+20, -16		
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	54.8	A	
		$T_C = 70$ °C	43.8		
		$T_A = 25$ °C	23.7 ^{b, c}		
		$T_A = 70$ °C	19 ^{b, c}		
Pulsed drain current ($t = 100$ μ s)	I_{DM}	90	130	A	
Continuous source-drain diode current	I_S	$T_C = 25$ °C	16.7		
		$T_A = 25$ °C	3.2 ^{b, c}	4 ^{b, c}	
Single pulse avalanche current	I_{AS}	15	20	mJ	
Single pulse avalanche energy					E_{AS}
Maximum power dissipation	P_D	$T_C = 25$ °C	20	W	
		$T_C = 70$ °C	12.9		
		$T_A = 25$ °C	3.8 ^{b, c}		4.8 ^{b, c}
		$T_A = 70$ °C	2.4 ^{b, c}		3.1 ^{b, c}
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150		°C	
Soldering recommendations (peak temperature) ^{c, d}		260			

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	CHANNEL-1		CHANNEL-2		UNIT
		TYP.	MAX.	TYP.	MAX.	
Maximum junction-to-ambient ^{b, f}	R_{thJA}	26	33	21	26	°C/W
Maximum junction-to-case (drain)	R_{thJC}	4.7	6.2	3	3.8	

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 68 °C/W for channel-1 and 57 °C/W for channel-2



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT		
Static								
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 5\text{ mA}$	Ch-1	30	-	-	V	
			Ch-2	30	-	-		
Drain-source breakdown voltage (transient) ^c	V_{DSt}	$V_{GS} = 0\text{ V}, t_{transient} \leq 1\text{ }\mu\text{s}$	Ch-1	36	-	-		
			Ch-2	36	-	-		
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	1.2	-	2.2		
			Ch-2	1.1	-	2.2		
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = +20\text{ V}, -16\text{ V}$	Ch-1	-	-	± 100	nA	
			Ch-2	-	-	± 100		
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-1	-	-	1	μA	
			Ch-2	-	40	200		
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-1	-	-	5		
			Ch-2	-	200	2000		
On-state drain current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	20	-	-	A	
			Ch-2	20	-	-		
Drain-source on-state resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	Ch-1	-	0.00338	0.00439	Ω	
			Ch-2	-	0.0018	0.0024		
			$V_{GS} = 4.5\text{ V}, I_D = 12\text{ A}$	Ch-1	-	0.00547		0.00712
				Ch-2	-	0.0026		0.0038
Forward transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 15\text{ A}$	Ch-1	-	55	-	S	
			Ch-2	-	230	-		
Dynamic ^a								
Input capacitance	C_{iss}	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1	-	790	-	pF	
			Ch-2	-	2130	-		
Output capacitance	C_{oss}		Ch-1	-	390	-		
			Ch-2	-	1050	-		
Reverse transfer capacitance	C_{rss}		Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1	-	38		-
				Ch-2	-	40		-
C_{rss}/C_{iss} ratio		Ch-1		-	0.046	0.092		
		Ch-2		-	0.019	0.038		
Total gate charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 19\text{ A}$		Ch-1	-	12	18	nC
				Ch-2	-	31.1	46.7	
			$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 19\text{ A}$	Ch-1	-	5.7	8.6	
				Ch-2	-	14.6	21.9	
Gate-source charge	Q_{gs}	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 19\text{ A}$	Ch-1	-	3	-		
			Ch-2	-	7.1	-		
Gate-drain charge	Q_{gd}		Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 19\text{ A}$	Ch-1	-	1.4	-	
				Ch-2	-	3.4	-	
Output charge	Q_{oss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$		Ch-1	-	10	-	
				Ch-2	-	30	-	
Gate resistance	R_g	$f = 1\text{ MHz}$	Ch-1	0.2	1.1	2.2	Ω	
			Ch-2	0.16	0.8	1.6		



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Dynamic ^a							
Turn-on delay time	t _{d(on)}	Channel-1 V _{DD} = 15 V, R _L = 1.5 Ω, I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1	-	20	40	ns
Rise time	t _r		Ch-2	-	30	60	
Turn-off delay time	t _{d(off)}	Channel-2 V _{DD} = 15 V, R _L = 1.5 Ω, I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1	-	100	200	
			Ch-2	-	120	240	
Fall time	t _f	Channel-1	Ch-1	-	15	30	
			Ch-2	-	40	80	
Turn-on delay time	t _{d(on)}	Channel-2	Ch-1	-	12	24	
			Ch-2	-	18	36	
Rise time	t _r	Channel-1 V _{DD} = 15 V, R _L = 1.5 Ω, I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1	-	10	20	
			Ch-2	-	15	30	
Turn-off delay time	t _{d(off)}	Channel-2	Ch-1	-	20	40	
			Ch-2	-	10	20	
Fall time	t _f	Channel-1	Ch-1	-	20	40	
			Ch-2	-	30	60	
		Channel-2	Ch-1	-	10	20	
			Ch-2	-	10	20	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	T _C = 25 °C	Ch-1	-	-	16.7	A
			Ch-2	-	-	27.4	
Pulse diode forward current ^a	I _{SM}		Ch-1	-	-	90	
			Ch-2	-	-	130	
Body diode voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V	Ch-1	-	0.8	1.2	V
			Ch-2	-	0.47	0.71	
Body diode reverse recovery time	t _{rr}	Channel-1 I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	Ch-1	-	18	36	ns
			Ch-2	-	27	54	
Body diode reverse recovery charge	Q _{rr}	Channel-2 I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	Ch-1	-	18	36	nC
			Ch-2	-	17	34	
Reverse recovery fall time	t _a	Channel-1	Ch-1	-	10	-	ns
			Ch-2	-	15	-	
Reverse recovery Rise time	t _b	Channel-2	Ch-1	-	8	-	
			Ch-2	-	12	-	

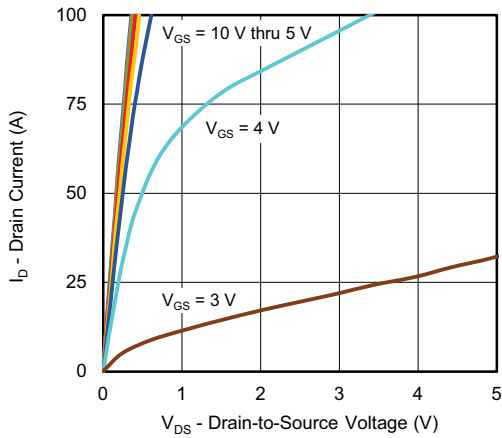
Notes

- a. Guaranteed by design, not subject to production testing
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- c. Derived from UIS characterization data at time of product release. Production data log is not available

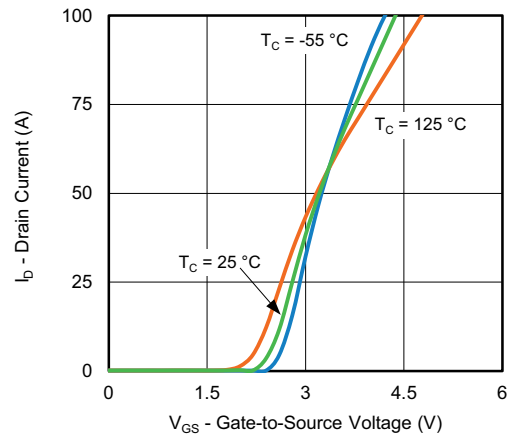
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



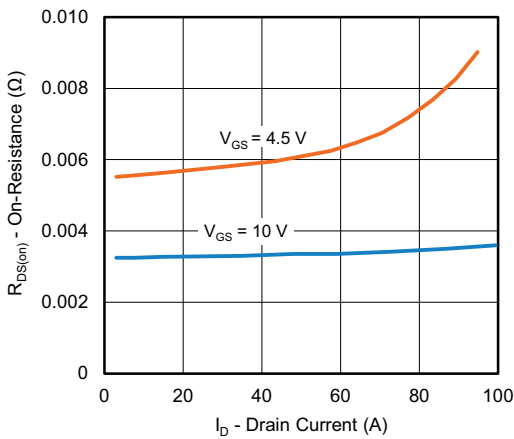
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



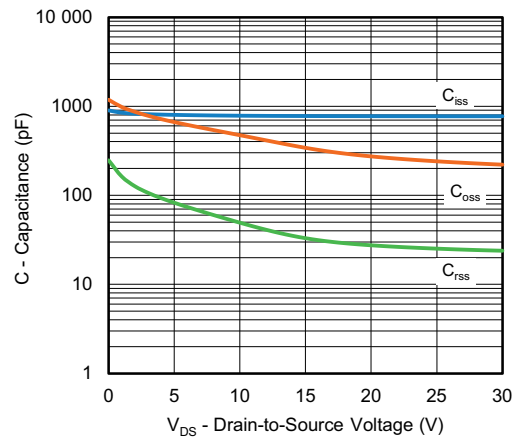
Output Characteristics



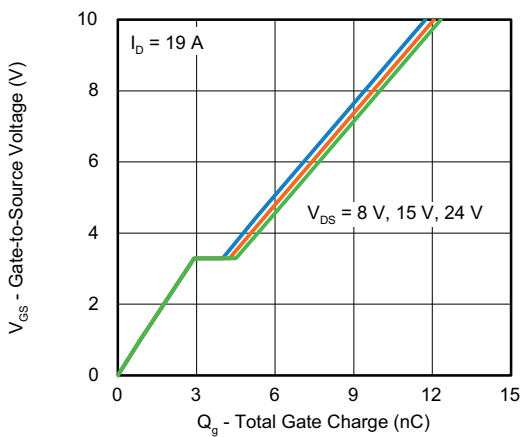
Transfer Characteristics



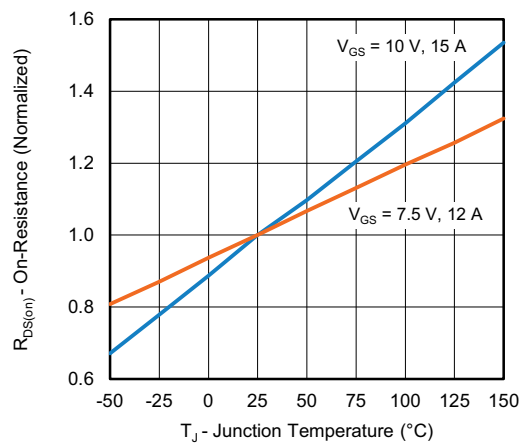
On-Resistance vs. Drain Current



Capacitance



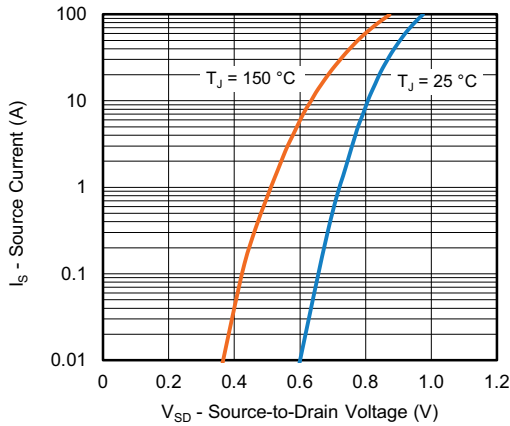
Gate Charge



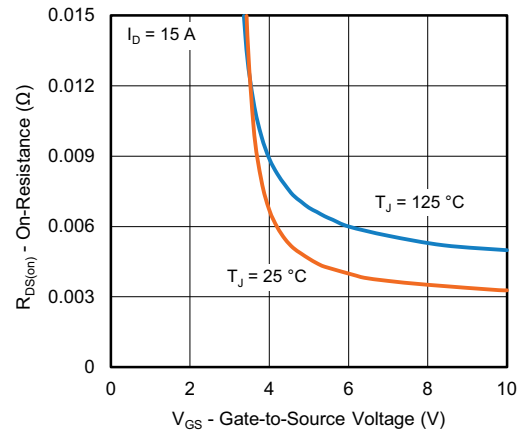
On-Resistance vs. Junction Temperature



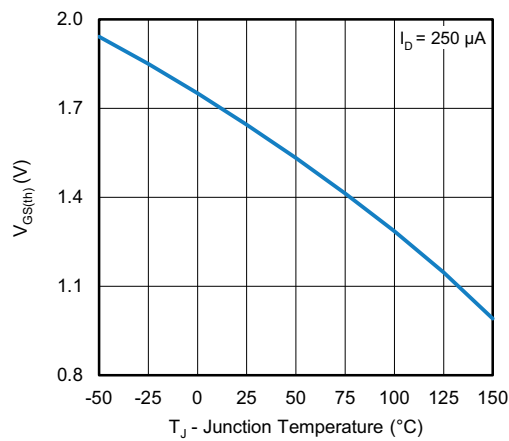
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



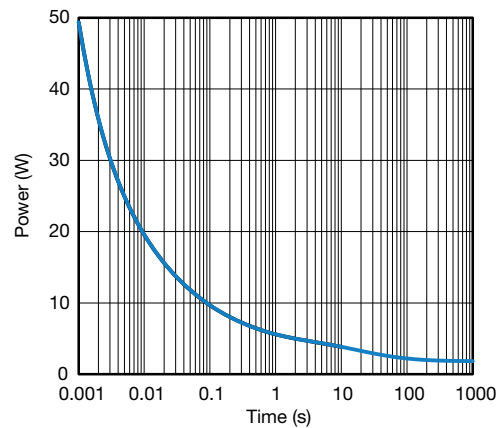
Source-Drain Diode Forward Voltage



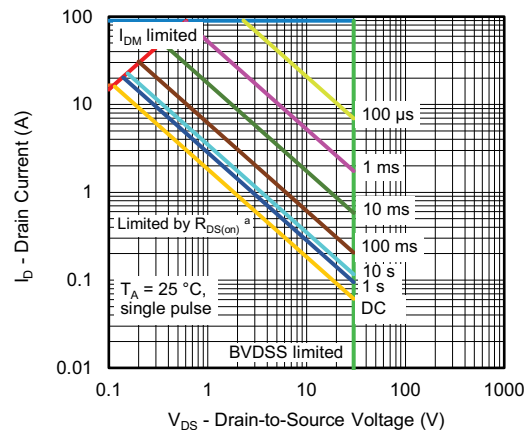
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



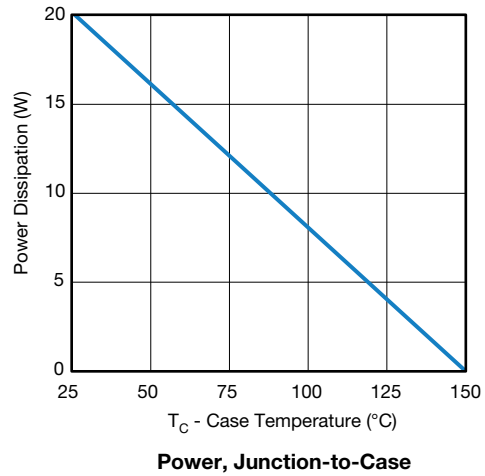
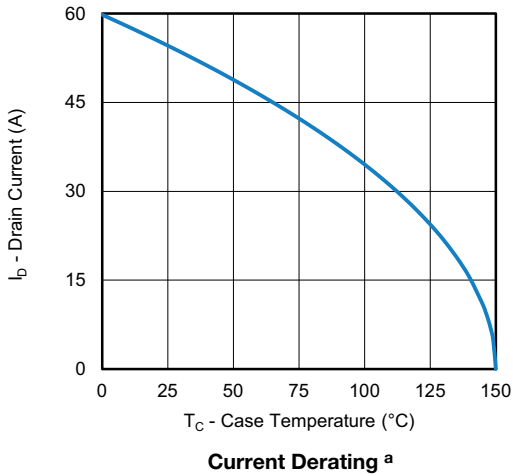
Safe Operating Area, Junction-to-Ambient

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

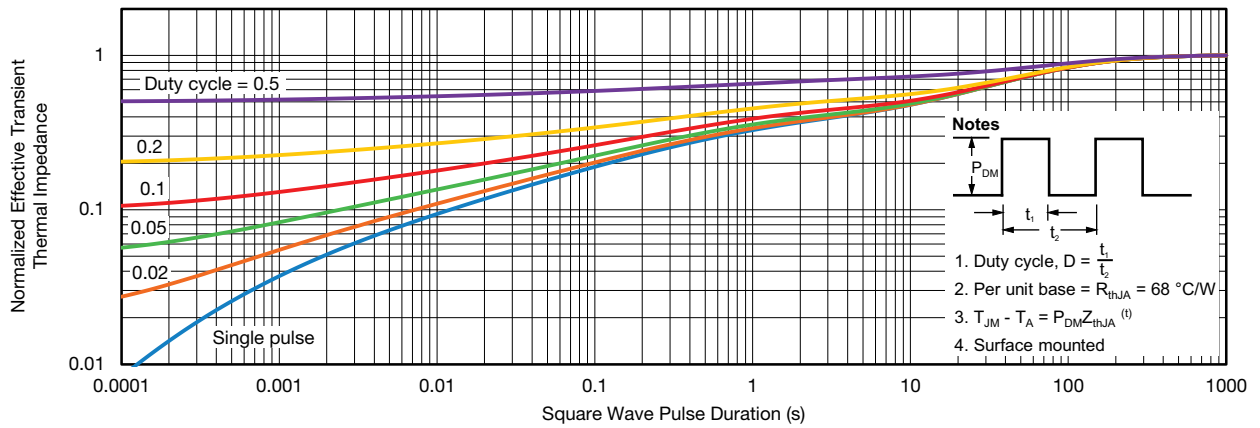


Note

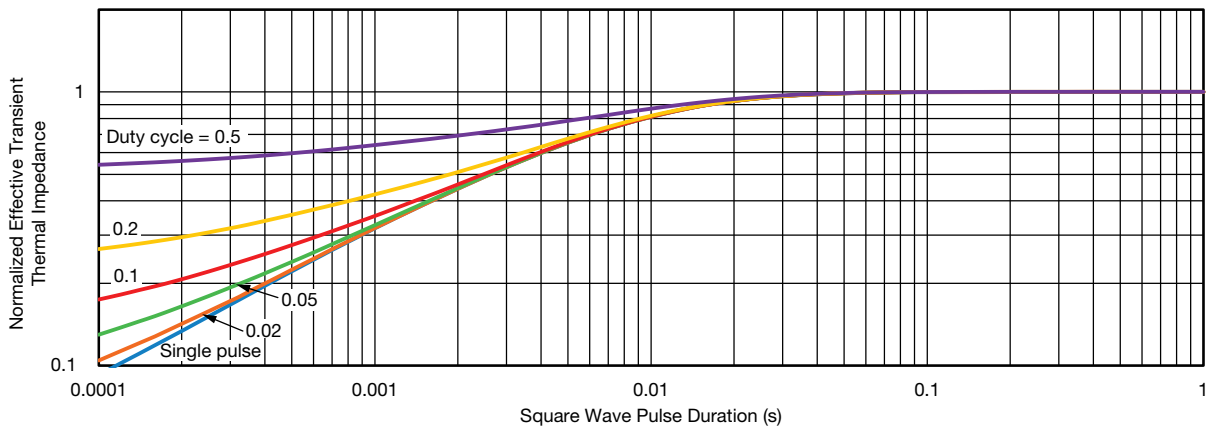
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



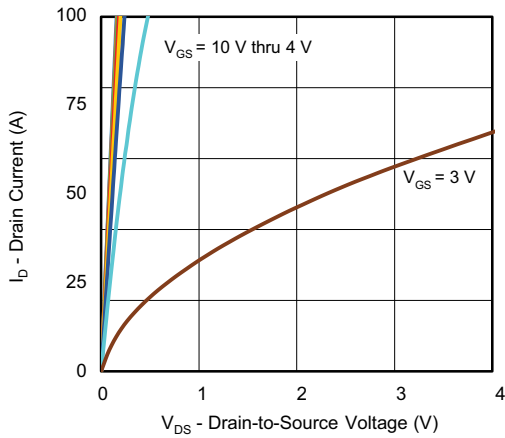
Normalized Thermal Transient Impedance, Junction-to-Ambient



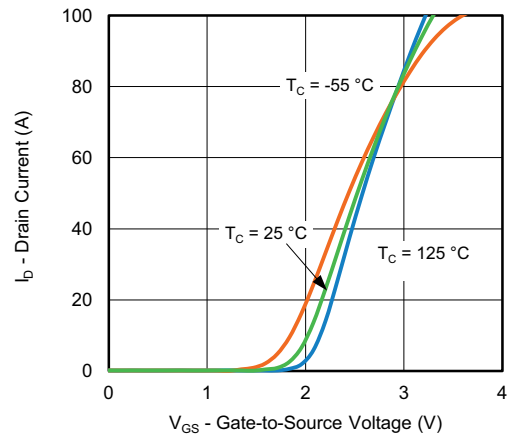
Normalized Thermal Transient Impedance, Junction-to-Case



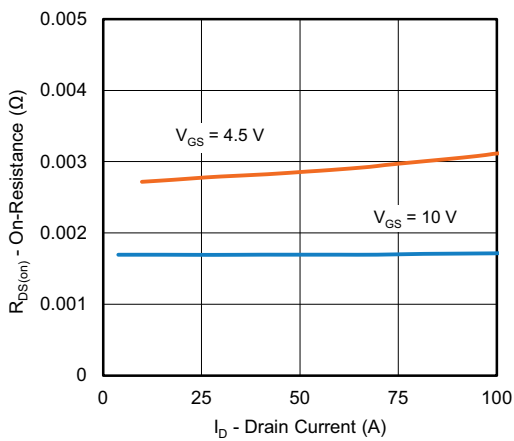
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



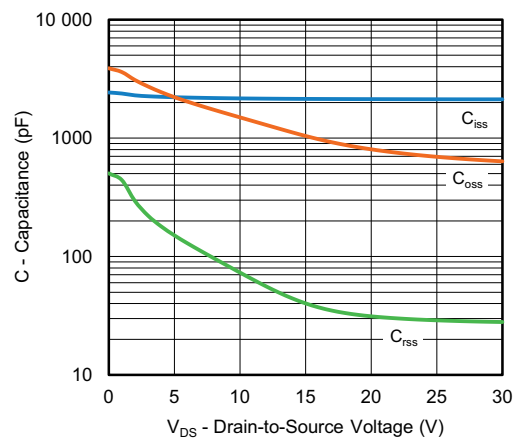
Output Characteristics



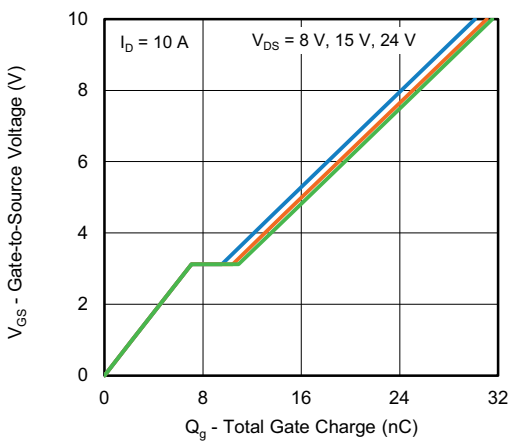
Transfer Characteristics



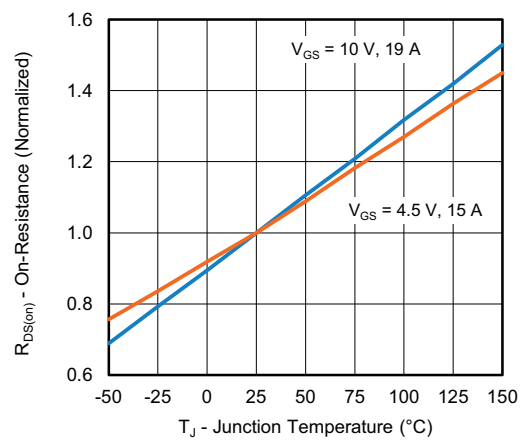
On-Resistance vs. Drain Current



Capacitance



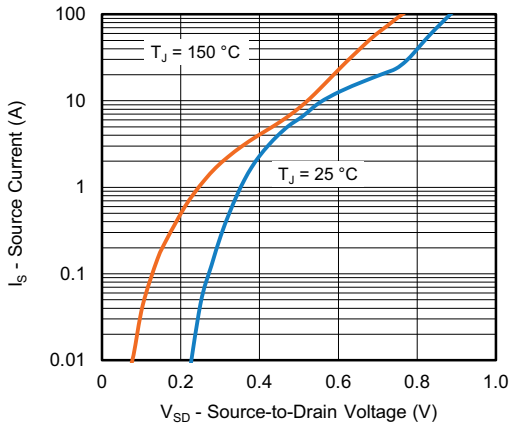
Gate Charge



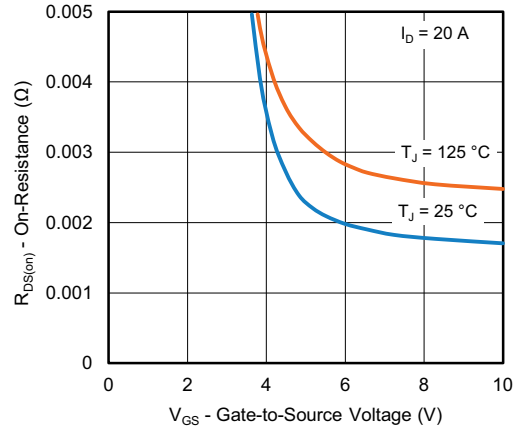
On-Resistance vs. Junction Temperature



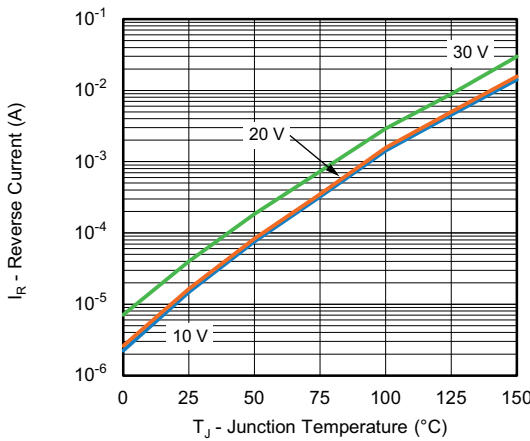
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



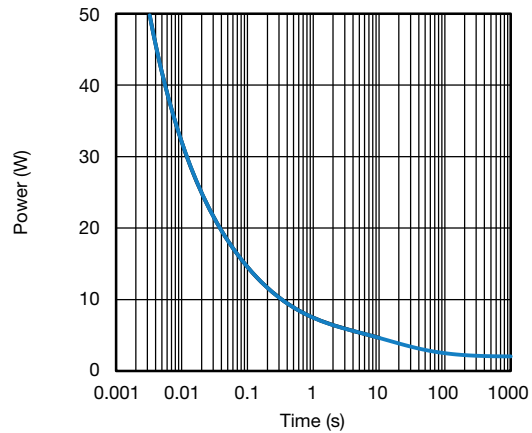
Source-Drain Diode Forward Voltage



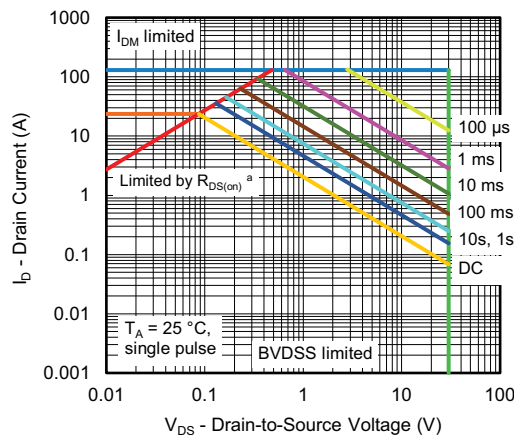
On-Resistance vs. Gate-to-Source Voltage



Reverse Current (Schottky)



Single Pulse Power, Junction-to-Ambient



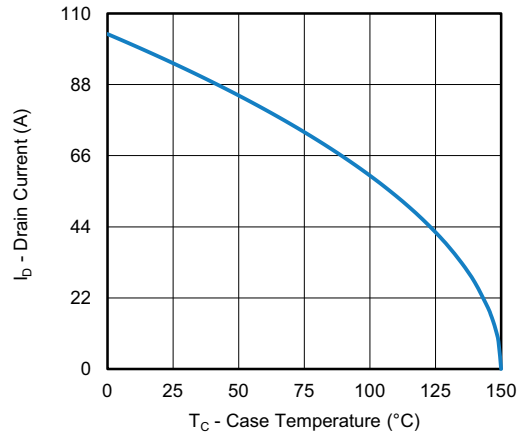
Safe Operating Area, Junction-to-Ambient

Note

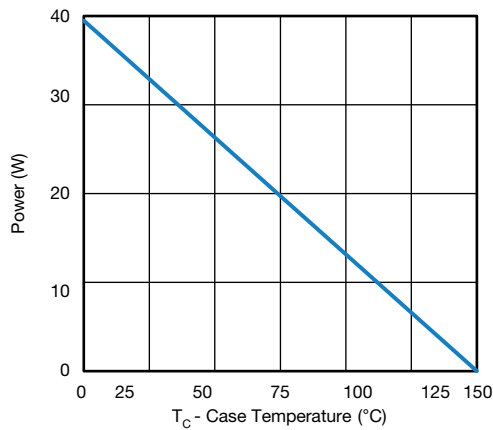
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



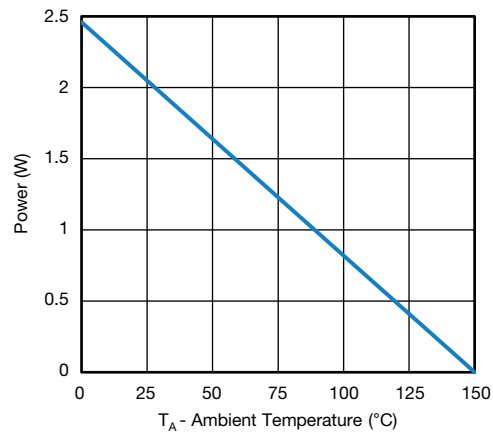
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power, Junction-to-Case



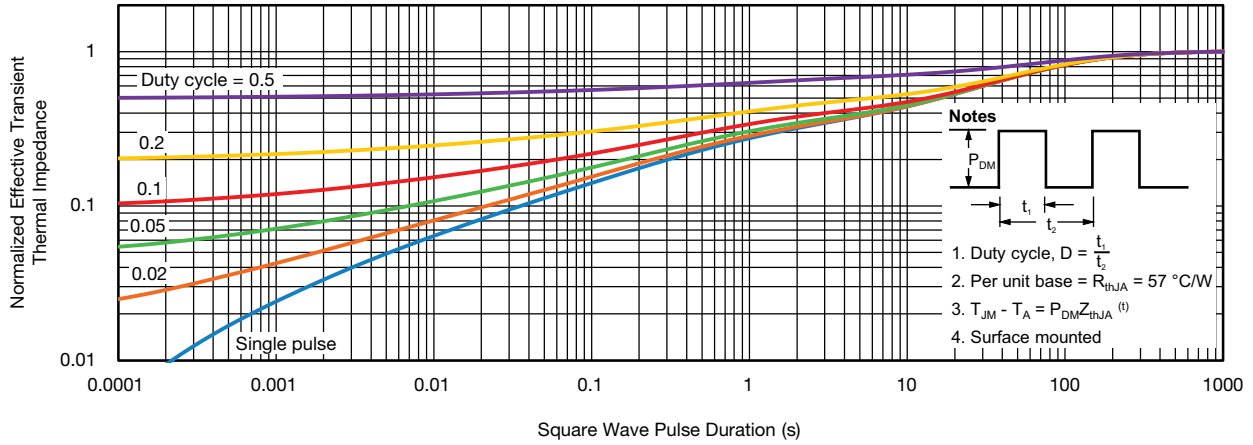
Power, Junction-to-Ambient

Note

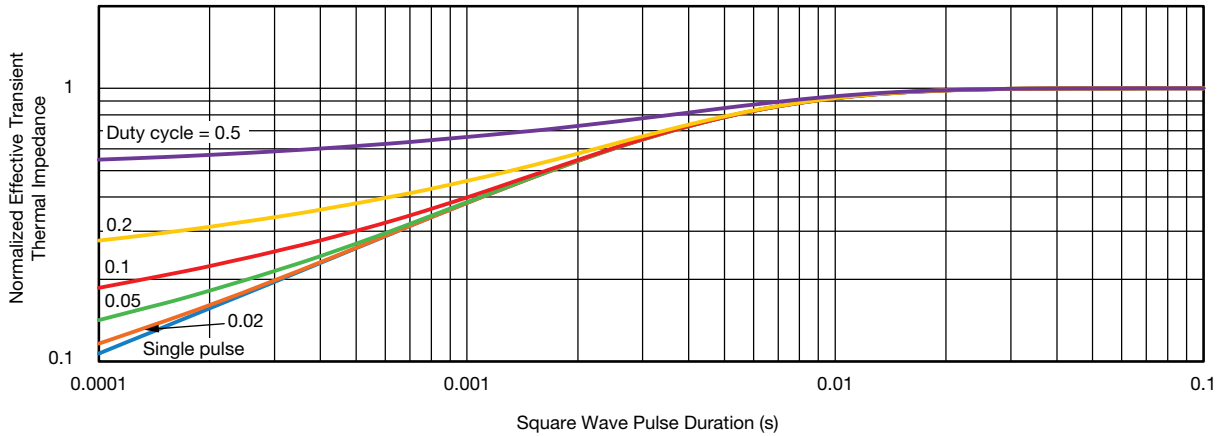
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?77875.

PowerPAIR® 6 x 5 Case Outline



Top side view

Back side view

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	-	0.10	0.000	-	0.004
A3	0.15	0.20	0.25	0.006	0.007	0.009
b	0.43	0.51	0.61	0.017	0.020	0.024
b1	0.25 BSC			0.010 BSC		
D	4.90	5.00	5.10	0.192	0.196	0.200
D1	3.75	3.80	3.85	0.148	0.150	0.152
E	5.90	6.00	6.10	0.232	0.236	0.240
E1 Option AA (for W/B)	2.62	2.67	2.72	0.103	0.105	0.107
E1 Option AB (for BWL)	2.42	2.47	2.52	0.095	0.097	0.099
E2	0.87	0.92	0.97	0.034	0.036	0.038
e	1.27 BSC			0.050 BSC		
K Option AA (for W/B)	0.45 typ.			0.018 typ.		
K Option AB (for BWL)	0.65 typ.			0.025 typ.		
K1	0.66 typ.			0.025 typ.		
L	0.33	0.43	0.53	0.013	0.017	0.020
L3	0.23 BSC			0.009 BSC		
z	0.34 BSC			0.013 BSC		
ECN: T14-0782-Rev. C, 22-Dec-14						
DWG: 6005						

Recommended Minimum PAD for PowerPAIR® 6 x 5



Dimensions in millimeters (inch)

Note

- Linear dimensions are in black, the same information is provided in ordinate dimensions which are in blue.



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