

N-Channel 250 V (D-S) MOSFET

DESCRIPTION

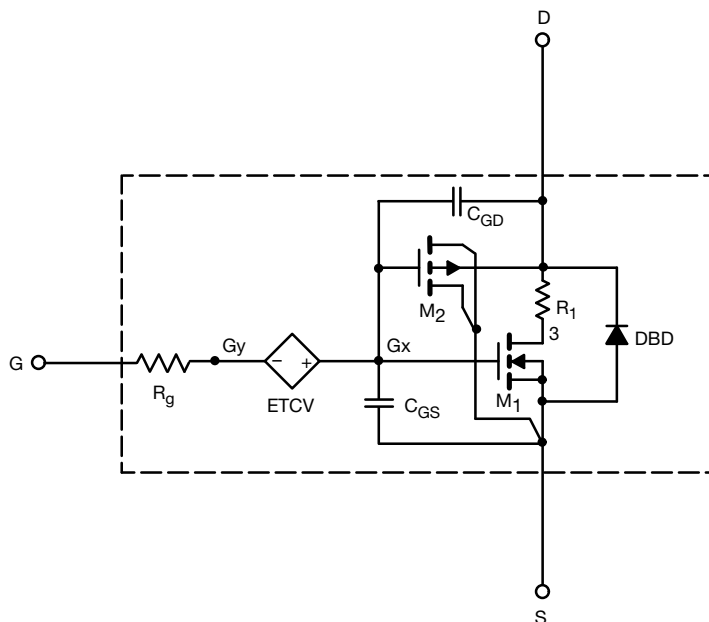
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to 125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



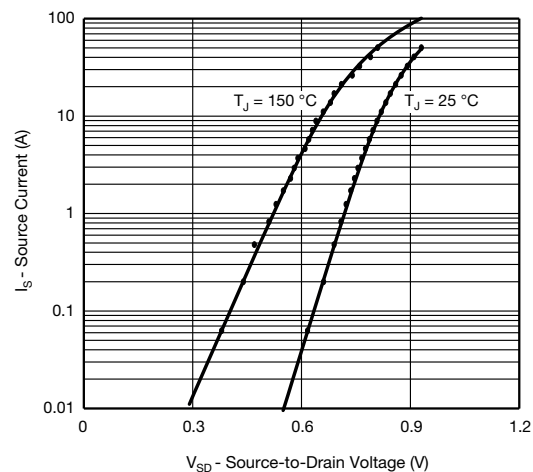
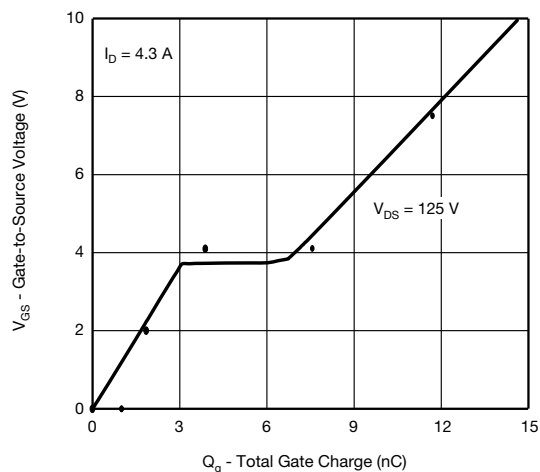
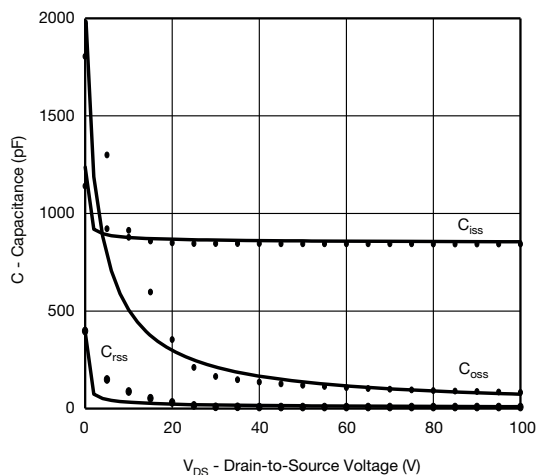
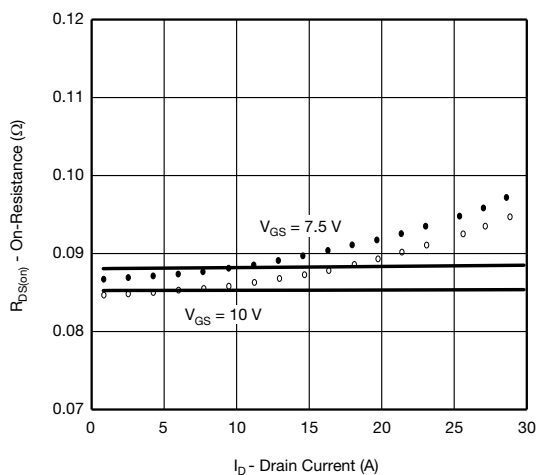
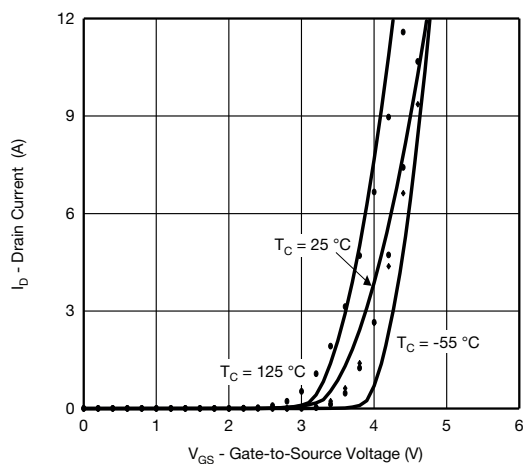
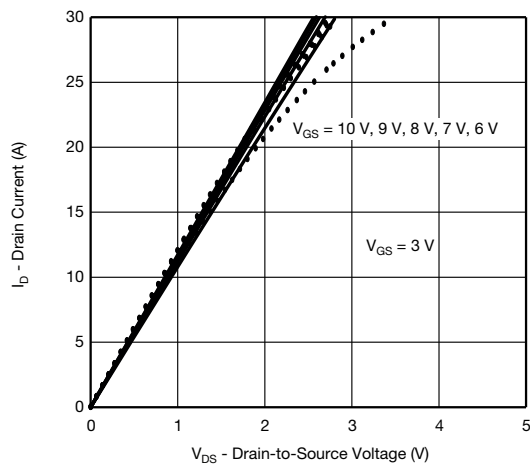
| SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted) | | | | | |
|---|--------------|--|----------------|---------------|----------|
| PARAMETER | SYMBOL | TEST CONDITIONS | SIMULATED DATA | MEASURED DATA | UNIT |
| Static | | | | | |
| Gate-source threshold voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 3 | - | V |
| Drain-source on-state resistance ^a | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$, $I_D = 4.3\text{ A}$ | 0.085 | 0.085 | Ω |
| | | $V_{GS} = 7.5\text{ V}$, $I_D = 4.1\text{ A}$ | 0.088 | 0.088 | |
| Forward transconductance ^a | g_{fs} | $V_{DS} = 15\text{ V}$, $I_D = 4.3\text{ A}$ | 11 | 11 | S |
| Diode forward voltage | V_{SD} | $I_S = 3.4\text{ A}$ | 0.76 | 0.75 | V |
| Dynamic ^b | | | | | |
| Input capacitance | C_{iss} | $V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$ | 855 | 860 | pF |
| Output capacitance | C_{oss} | | 74 | 85 | |
| Reverse transfer capacitance | C_{rss} | | 10 | 7 | |
| Total gate charge | Q_g | $V_{DS} = 125\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 4.3\text{ A}$ | 14.8 | 14.9 | nC |
| | | $V_{DS} = 125\text{ V}$, $V_{GS} = 7.5\text{ V}$, $I_D = 4.3\text{ A}$ | 11.6 | 11.7 | |
| Gate-source charge | Q_{gs} | | 3 | 3.9 | |
| Gate-drain charge | Q_{gd} | | 3.7 | 3.7 | |

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data

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