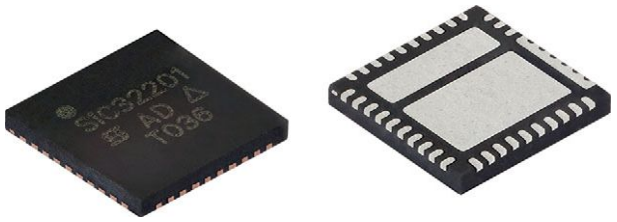
0.45 mΩ, Integrated OR-ing Switch With OR-ing Controller, Lossless Current Sense, and Temperature Report



DESCRIPTION

The SiC32201 is a highly integrated smart OR-ing solution featuring an advanced lossless current sensing design. Compared to conventional designs with shunt resistors, OR-ing MOSFETs and other discrete and ICs, the SiC32201 reduces the overall solution size and component count while increasing power density and efficiency.

The SiC32201 integrates a 0.45 mΩ n-channel OR-ing MOSFET, a MOSFET driver, forward and reverse voltage detection for OR-ing control and precision current and temperature sensing. Its internal fast reverse current protection circuit significantly reduces the reverse current level during the OR-ing input short fault, improving system bus voltage stability.

The SiC32201 is optimized for 12 V operation. It operates over the voltage range of 9 V to 20 V and can be paralleled to support different power range requirements. The current through the OR-ing switch is reported at the I_{MON} pin. The T_{MON} pin reflects the highest temperature of the parallel parts. It also flags overtemperature and insufficient OR-ing MOSFET gate drive.

The SiC32201 is available in the compact, thermally enhanced 6 mm x 6 mm PowerPAK® MLP66-40L package.

FEATURES

- High efficiency
  - Integrated 0.45 mΩ n-channel current sense MOSFET
  - Lossless current sense without shunt resistor
- Compact
  - Integrated current sensing and reporting circuits
  - Integrated OR-ing control and OR-ing FET driver
- Versatile
  - Guaranteed precise current reporting, ± 2 % for ≥ 10 A Load current. IMON offset is ± 10 µA at 0.5 A load current
  - Can be paralleled for different power ranges
  - Device temperature reporting through T_{MON}. Highest temperature reported when multiple T_{MON} pins are connected together
- Protection and alert
  - Fast response to reverse condition, 200 ns/typ. OR-ing FET off time
  - Reverse detection indicated pulling COMM1 low
  - T_{MON} pulled high, alert junction temperature is higher than 120 °C or internal charge pump UVLO

APPLICATIONS

- High availability system power
- N+1 redundant power supplies
- Telecom infrastructure
- Server and networking

APPLICATION CIRCUIT

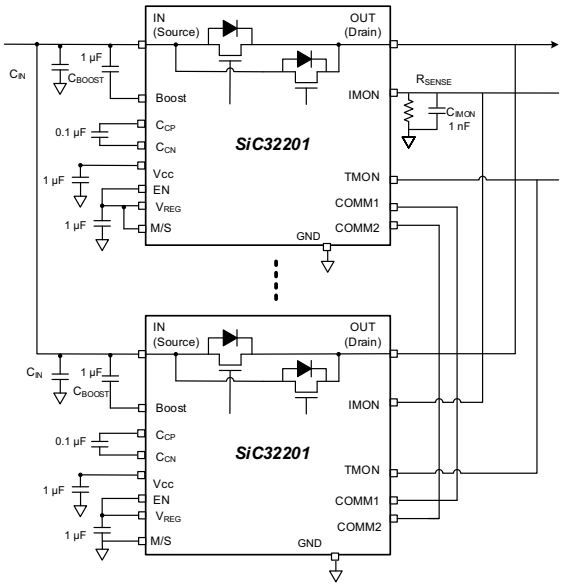


Fig. 1 - Typical Application Circuit

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TYPICAL PARALLEL MODE APPLICATION

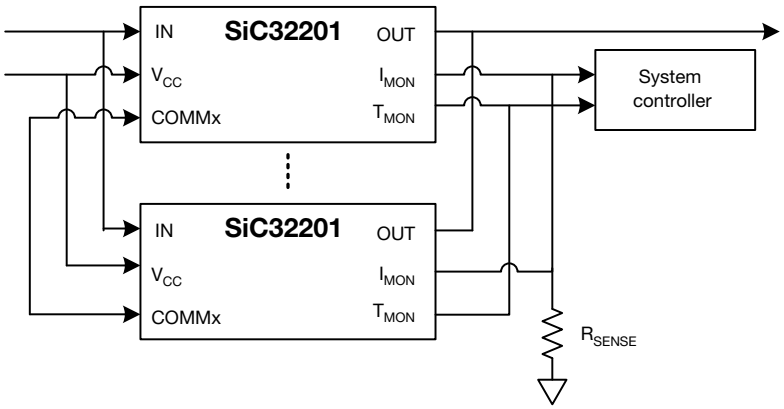

Fig. 2 - Typical Parallel Mode Application

PACKAGE OUTLINE

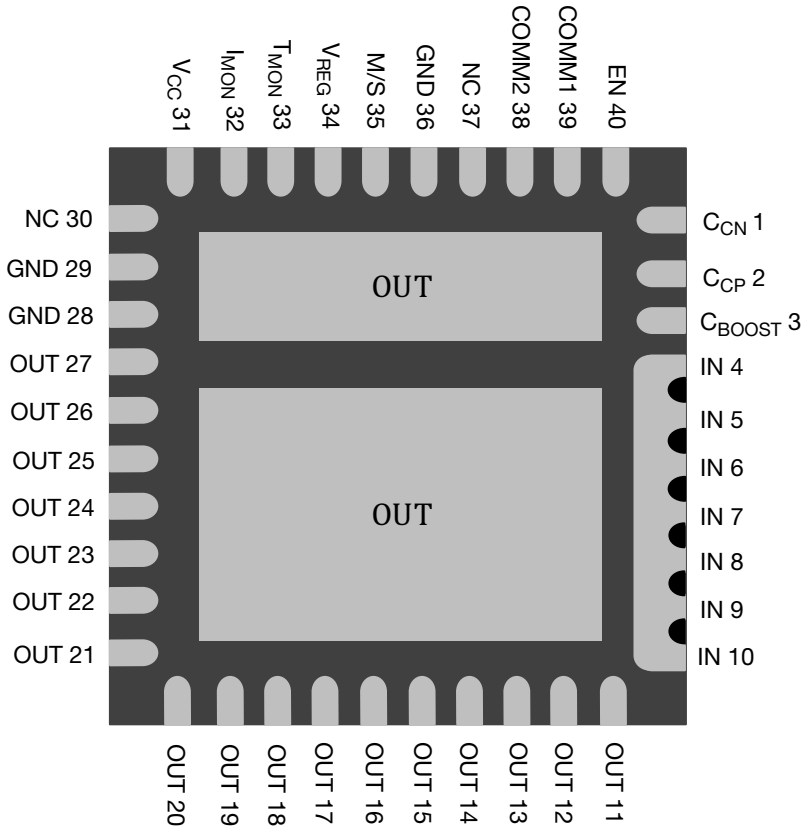

Fig. 3 - Device Pin Out (Bottom View)

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PIN DESCRIPTION

PIN NUMBER	PIN NAME	FUNCTION
1	C_{CN}	Negative terminal of the flying capacitor for the internal charge pump. Connect a 0.1 µF capacitor between C_{CN} and C_{CP}
2	C_{CP}	Positive terminal of the flying capacitor for the internal charge pump. Connect a 0.1 µF capacitor between C_{CN} and C_{CP}
3	C_{BOOST}	Storage capacitor for the internal charge pump. Connect a 1 µF capacitor from C_{BOOST} to V_{IN}
4 to 10	IN	OR-ing switch power input (source of the n-channel MOSFET)
11 to 27	OUT	OR-ing switch power output (drain of the n-channel MOSFET)
28, 29	GND	Product test pins. Connect them to GND on PCB
36	GND	Ground
30	NC	No connect
31	V_{CC}	Power supply for the controller. Connect a 1 µF or larger capacitor between V_{CC} and GND
32	I_{MON}	I_{MON} is an output pin that reports current through the OR-ing switch. Connect a resistor from I_{MON} to GND to convert the current to voltage. When using several SiC32201 in parallel the I_{MON} outputs may be connected to the same resistor to monitor the total current of the system
33	T_{MON}	T_{MON} is a temperature reporting and over temperature alert pin. T_{MON} outputs a voltage that is proportional to the die temperature. When the die temperature reaches over temperature threshold, this pin is pull up to 3 V. When using several SiC32201 in parallel the T_{MON} outputs may be connected together, in this case, only the highest temperature of all chips is reported. T_{MON} is pulled high also when internal charge pump is at UVLO condition
34	V_{REG}	5 V regulator output. Connect a 1 µF capacitor from V_{REG} to GND as close as possible to this pin
35	M / S	Master / slave setting pin. Connect to V_{REG} (“master”) or to GND (“slave”)
37	NC	No connect
38	COMM2	COMM2 is a communication pin between the paralleled parts. In master operation, COMM2 is an output pin that indicates light load or full on mode. In slave operation, drive COMM2 by external control signal or COMM2 of a master device to set the selected mode
39	COMM1	COMM1 is a communication pin which allows all SiC32201 units working in parallel to share information on the OR-ing switch status. It is an input and output pin. The COMM1 pin of all unites working in parallel should be connected together. COMM1 indicates forward current detection by a weak logic high. Forcing COMM1 high will turn on the OR-ing switch unless unit detects a reverse condition. When COMM1 is at logic high all the OR-ing switches are conducting forward current (IN to OUT). When a reverse condition is detected, the COMM1 will output a logic low
40	EN	The EN pin controls the OR-ing switch. When the EN is pulled low, the OR-ing switch off at any time. With the EN pin at logic high, the OR-ing switch status is defined by the internal controller functions. The EN pin can't be left unconnected

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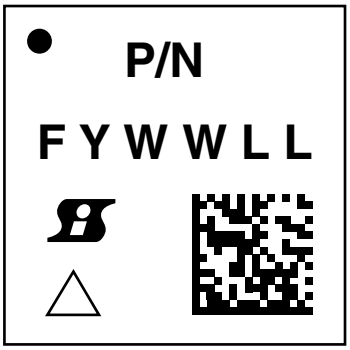
ORDERING INFORMATION		
PART NUMBER	**PACKAGE**	**MARKING**
SiC32201CD-T1E3	MLP40, 6 mm x 6 mm	Si32201

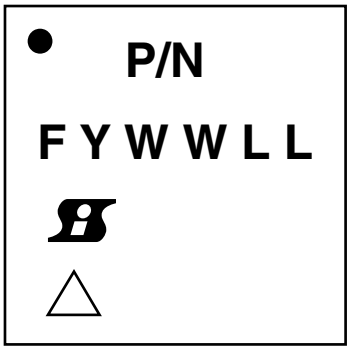
PART MARKING INFORMATION

With 2D code



or

Without 2D code



●	=	pin 1 indicator
P/N	=	part number code
F	=	assembly factory code
Y	=	year code
WW	=	week code
LL	=	lot code
	=	Siliconix logo
△	=	ESD symbol

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ABSOLUTE MAXIMUM RATINGS			
ELECTRICAL PARAMETER	**CONDITIONS**	**LIMIT**	**UNIT**
IC power supply V_{CC}		-0.3 to +24 (DS 20 V), and ≥ V_{IN} - 2 V	V
Continuous current	T_C = 25 °C	100 [a]	A
Pulsed current	t = 100 µs	300	
Avalanche current, single pulse	L = 0.1 mH	60	
Avalanche energy, single pulse		180	mJ
IN		-0.3 to +20 -0.6 V for 100 ns	V
OUT			
I_{MON}		-0.3 to V_{REG} + 0.3	
T_{MON}			
COMM1, COMM2			
EN		-0.3 to +6	
M / S			
V_{REG}			
C_{BOOST}		-0.3 to +32	
C_{CP}			
C_{CN}		V_{CC} - 12 to V_{CC} + 1	
Moisture sensitivity level (JEDEC®)-STD-020A		1	Level
Latch up current per JESD78		500	mA
Electrostatic discharge	Human body model	2	kV
	Machine model	500	V
Operating junction temperature		-40 to +150	°C
Storage temperature		-65 to +150	

Note

a. Package limited

THERMAL RESISTANCE RATINGS				
PARAMETER		**SYMBOL**	**TYPICAL**	**UNIT**
Junction-to-case (out / drain)	Steady state	R_{thJC}	0.9	°C/W

RECOMMENDED OPERATING RANGE			
PARAMETER	**CONDITIONS**	**LIMIT**	**UNIT**
V_{CC}		9 to 18	V
IN		0 to 18, and < V_{CC} + 2 V	
OUT		0 to 18	
I_{MON}		3	
T_{MON}		3	
EN, COMMx		0 to 5	
Operating junction temperature		-40 to +125	°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS unless otherwise specified, V_{CC} = 12 V, V_{IN} = 12 V, T_J = -40 °C **to** +125 °C, **typical values are at** 25 °C	LIMIT MIN.	LIMIT TYP.	LIMIT MAX.	UNIT
V_{CC} quiescent current	I_Q	M / S = GND, COMM1 and COMM2 = high, OUT open	-	1.8	3	mA
V_{CC} under voltage lock out	UVLO	M / S = GND, COMM1 and COMM2 = high, OUT open, V_{CC} rising	-	7.8	8.5	V
V_{CC} under voltage lock out hysteresis		M / S = GND, COMM1 and COMM2 = high, OUT open	-	400	-	mV
Charge pump under voltage lock out	$UVLO_{CP}$	M / S = GND, COMM1 and COMM2 = high, OUT open, V_{CP} rising	-	6.4	-	V
Charge pump under voltage lock out hysteresis		M / S = GND, COMM1 and COMM2 = high, OUT open	-	250	-	mV
OR-ing FET						
Source to drain resistance (full on mode)	R_{SD}	T_J = 25 °C, I_D = 30 A	-	0.45	0.6	mΩ
Source to drain resistance (light on mode)		T_J = 25 °C, I_D = 1 A	-	5.7	-	
Diode current		DC when T_{CASE} = 25 °C	-	-	100	A
Diode forward voltage	V_F	I_{OUT} = -100 mA	-	600	-	mV
OR-ing Controller						
Switch on forward threshold current	I_{FWD}	Current from V_{IN} to V_{OUT}	75	400	800	mA
Switch on forward threshold current hysteresis	I_{FWD_HYST}		-	260	-	
Reverse voltage detection	V_{REV}	V_{OUT} - V_{IN}	3	7	12	mV
Light load to full on mode current threshold		M / S = high, current goes from low to high	-	4	-	A
Full on mode to Light load current threshold		M / S = high, current goes from high to low	-	2.8	-	A
Light load and full on mode current threshold hysteresis		M / S = high	-	1.2	-	A
Turn on time		M / S = high, COMM1and COMM2 floating, from I_{FWD} load step reaching 1.5 A to V_{SD} (V_{IN} - V_{OUT}) ≤ 250 mV	-	2	-	µs
Turn off time		COMM1 = high, from V_{OUT} - V_{IN} = 20 mV to I_{OUT} ≤ 1 A (switch off)	-	200	-	ns
On time on COMM1		Time from COMM1 rising to switch turned on	-	1	-	µs
Forward detect response on COMM1		COMM1 high from I_{FWD} detect	-	56	-	ns
I_{MON}						
Accuracy		≥ 10 A, R_{SENSE} = 600 Ω, 25 °C	-2	-	2	%
		≥ 10 A, R_{SENSE} = 600 Ω, -40 °C to +125 °C	-3	-	3	
		≥ 2 A, R_{SENSE} = 600 Ω, 25 °C	-3	-	3	
		≥ 2 A, R_{SENSE} = 600 Ω, -40 °C to +125 °C	-5	-	5	
Offset		I_{OUT} = 0.5 A, R_{SENSE} = 600 Ω, 25 °C	-10	-	10	µA
		I_{OUT} = 0 A, R_{SENSE} = 600 Ω, 25 °C	-5	-	5	
Hot Swap						
Reverse leakage	I_R	V_{CC} = 0 V to 12 V, V_{IN} = 0 V to 12 V, V_{OUT} > V_{IN} + 10 mV (measured on OUT)	-	-	1	mA
T_{MON}						
25 °C T_{MON} voltage		T = 25 °C, R_{TMON} = 1 MΩ, C_{TMON} = 50 pF		0.8		V
Temperature sense gain		R_{TMON} = 1 MΩ, C_{TMON} = 50 pF		8		mV/°C
Temperature Protection						
OTP threshold		Temperature increasing	-	150	-	°C
OTP hysteresis			-	20	-	
T_{MON} OTP FLAG voltage		T > 150 °C	2.5	-	-	V
T_J threshold to disable light load mode		Temperature increasing	-	120	-	°C
T_J hysteresis to disable light load mode			-	10	-	

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ELECTRICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS unless otherwise specified, V_{CC} = 12 V, V_{IN} = 12 V, T_J = -40 °C to +125 °C, typical values are at 25 °C	LIMIT MIN.	LIMIT TYP.	LIMIT MAX.	UNIT
COMM1						
High level threshold	V_{MH}		-	2.5	2.8	V
Mid level threshold (upper)	V_{MIDH}		2.2	2.5	-	
Mid level threshold (lower)	V_{MIDL}		-	1.0	1.2	
Low level threshold	V_{ML}		0.8	1.0	-	
Output logic high	V_{OH}	M / S = V_{REG}, I_{LOAD} ≥ 1.5 A, I_{COMM1} = -10 µA	2.5	-	-	
Output logic mid-level	V_{OM}	M / S = V_{REG}, I_{LOAD} = 0 A, COMM1 floating	1.4	1.75	2.0	
COMM2						
Input logic low	V_{IL}	M / S = GND, COMM1 = GND	0.8	-	-	V
Input logic high	V_{IH}	M / S = GND, COMM1 = GND	-	-	2.4	
Output logic low	V_{OL}	M / S = V_{REG}, 1.5 A ≤ I_{LOAD} ≤ 10 A, I_{COMM2} = 1 mA	-	-	0.4	
Output logic high	V_{OH}	M / S = V_{REG}, I_{LOAD} ≥ 10 A I_{COMM2} = -1 mA	2.5	-	-	
EN						
Input logic low	V_{IL}	I_{LOAD} ≥ 1.5 A	0.8	-	-	V
Input logic high	V_{IH}	I_{LOAD} ≥ 1.5 A	-	-	2.4	

FUNCTIONAL BLOCK DIAGRAM

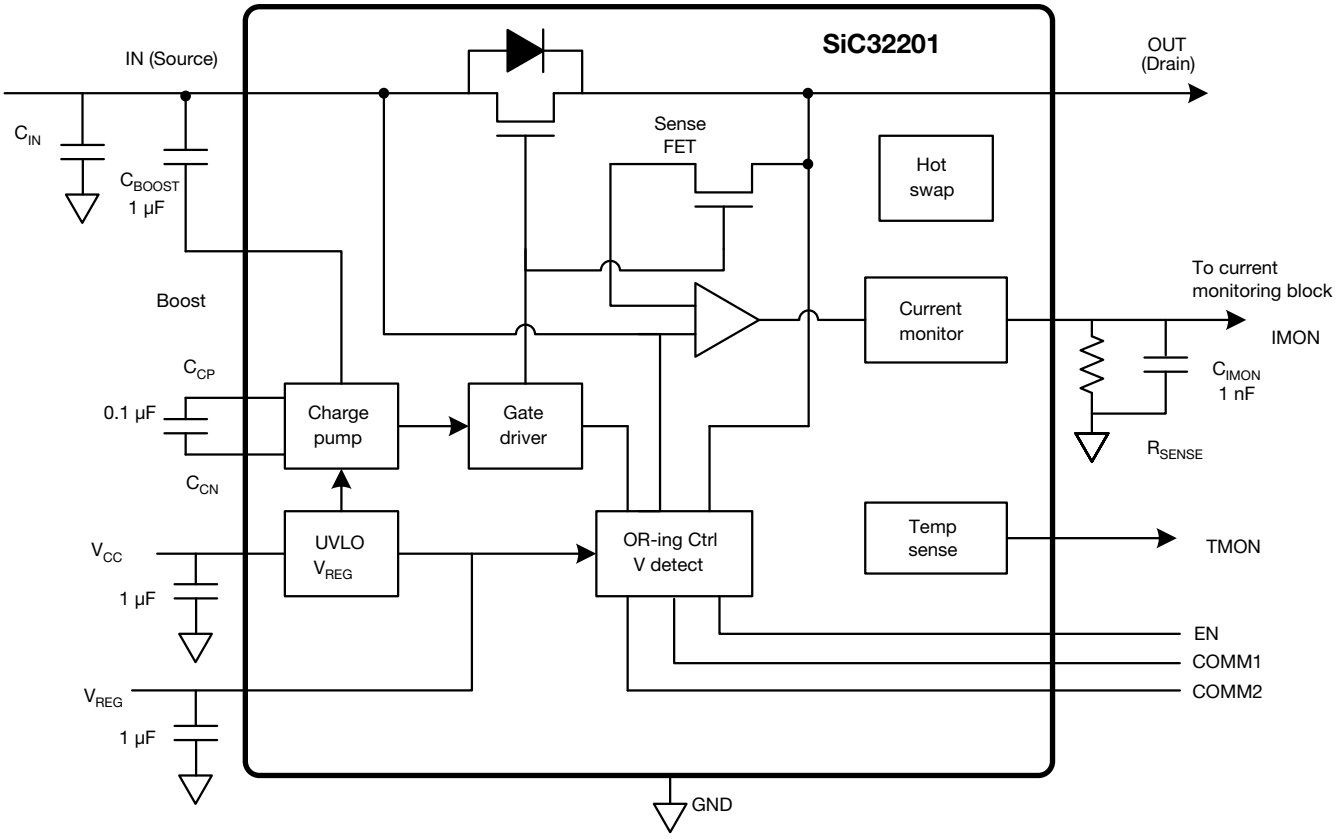

Fig. 4 - Functional Block Diagram

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OPERATIONAL DESCRIPTION

Device Overview

The SiC32201 is a highly integrated smart OR-ing solution with advanced lossless current sensing design.

The SiC32201 integrates a 0.45 mΩ OR-ing n-channel. Multiple devices can be paralleled to support higher power requirements. Up to maximum eight parts can be in paralleled mode. The OR-ing control, MOSFET driver, current and temperature sensing and reporting circuits are integrated. The proprietary current sensing design eliminates the shunt resistor, achieving lossless power sensing, shorter power path, and compact solution size. Integrated design also enables ultra-fast response to reverse condition, minimizes reverse charge and impact on power path.

The integrated OR-ing MOSFET is partition into two portions, a small FET and a large FET. At light load mode, the small FET is on, otherwise both large and small FET is on. Such a design enables the part to provide precision current reporting and fast response to reverse condition.

The SiC32201 operates in the voltage range of 9 V to 20 V, features precision and faster current reporting at its I_{MON}. The current can be sum at shorting all I_{MON} pins to a current reporting resistor under paralleled configuration. The device temperature is reported at T_{MON} pin. When multiple T_{MON} pins of paralleled parts are tied together, the highest temperature is reported.

Operation of the EN

The EN pin controls the OR-ing switch. When the EN is pulled low, the OR-ing switches off. The SiC32201 continues to report current and voltage detection through the switch, even when EN is low. With the EN pin at logic high, the OR-ing switch status is defined by the internal controller functions. The OR-ing switch will remain off until forward mode is detected, or COMM1 is forced high. In OR-ing design using multiple chips, all of the EN pins can be tied together. The EN pin can't be left unconnected.

The Operation of M/S

The M/S (master/slave) pin is an input. Pulling the M/S pin high sets the device to master. A master device will detect the current level and determine if it should be at light load, or full on mode. The master device outputs a logic high on COMM2 for full on mode and low for light load mode.

In a system with multiple SiC32201 operating in parallel, only one controller can be set to “master”, while all other controllers need to be set to “slave”. Connect the M/S pin to V_{REG} to set the “master” functionality, connect it to GND to set the “slave” functionality. If all paralleled devices are set to slave mode, all their COMM2 pins need to be connected together and driven externally.

Operation of COMM1

The COMM1 communicates between paralleled parts. It is a bidirectional pin with a tristate output.

The COMM1 pins of all paralleled parts should be connected together. If this COMM1 node is left floating, the load current will determine the state of the COMM1 node. Alternatively, the COMM1 node may be pulled high to V_{REG} through a resistor in order to bypass diode mode.

When the voltage applied on COMM1 exceeds the 2.5 V input high threshold, the OR-ing switch will turn on, assuming no reversed condition or other faults are present. If COMM1 is left floating and the output current is less than 400 mA, the controller forces the COMM1 pin to 1.75 V by a push-pull output section, with a 2 µA current limit.

In multiple parts parallel designs with COMM1 floating, once any part in parallel output current exceeds 400 mA, this part will turn on its OR-ing switch and force the COMM1 node high, with a 20 µA internal current source. This will signal all other parts in parallel to turn on as well. The current between the paralleled parts will not be exactly the same. Once the first part detects forward current and turns on, all current will flow through it as it is of the lowest resistance path. Without the COMM1 communication, other parts in parallel will not see forward current, and turn on. The COMM1 pin synchronizes the paralleled parts to turn them on once one of them detects forward current. The OR-ing switch on at light load, or full on mode will be described in “Operation of COMM2”.

In order to bypass diode mode, a resistor should be placed between the COMM1 node and V_{REG}. This will keep the outputs on, even when the load current is less than 400 mA per controller. The value of the resistor should be 200 k/N, where N is the number of controllers on the bus.

If any controller detects a reverse voltage condition, the COMM1 node will be forced to ground through a 500 Ω resistor, overriding all other COMM1 inputs.

When EN is low, the COMM1 will continue to pull high when a forward current is detected and low when a reversed current detected.

Operation of COMM2

The COMM2 is a communication pin between the parallel parts, synchronizing them to light load, or full on mode.

The COMM2 pin is an output pin for the master and an input pin for all slaves. All COMM2 pins of the paralleled parts need to be tied together.

The part set as “master” controls the state of light load mode for all the parallel parts in the system, in order to achieve good current monitor accuracy, even at low current levels.

When the COMM2 pin is at logic low level, the small OR-ing switch of 5.7 mΩ resistance is on.

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When the COMM2 pin is at logic high level, the full OR-ing switch of 0.45 mΩ resistance is on.

At initial power-up or when coming out of reverse mode operation, the master and all slaves will start in light load mode ($R_{DS(on)}$ = 5.7 mΩ).

When a current level (4 A/typ) sufficient to provide good accuracy is detected, the master will drive the COMM2 pin to a logic high level (OR-ing MOSFET switch is fully ON and the resistance is 0.45 mΩ).

When the master controller detects a current above 4 A, it will:

1. Switch to full on mode. The switch resistance will be $R_{DS(on)}$ = 0.45 mΩ
2. Drive the COMM2 pin high to signal full on mode to the slave(s)

Note that when switching from light load mode to full on mode, the master will switch first, momentarily increasing the master's share of the load current. This provides some intrinsic hysteresis at the transition threshold from light load mode, to full on mode.

Additionally, there is 1.2 A hysteresis, so the trip point of full on mode is 4 A and the trip point of light load mode is 2.8 A.

When the master controller detects a current less than 2.8 A, it will:

3. Switch to light load mode ($R_{DS(on)}$ = 5.7 mΩ)
4. Drive the COMM2 pin low to signal light load mode to the slave(s)

The light load mode is disabled whenever the temperature is greater than 120 °C. In other words, if the temperature is greater than 120 °C, the chip will always operate with the output fully on or off.

Logic State Diagrams

The SiC32201 can be biased in one of the four configurations in application circuit designs.

TRUTH TABLE

CONFIGURATION	MASTER / SLAVE	COMM1
1	Master	Tied high through 100 kΩ
2	Master	Float
3	Slave	Tied high through 100 kΩ
4	Slave	Float

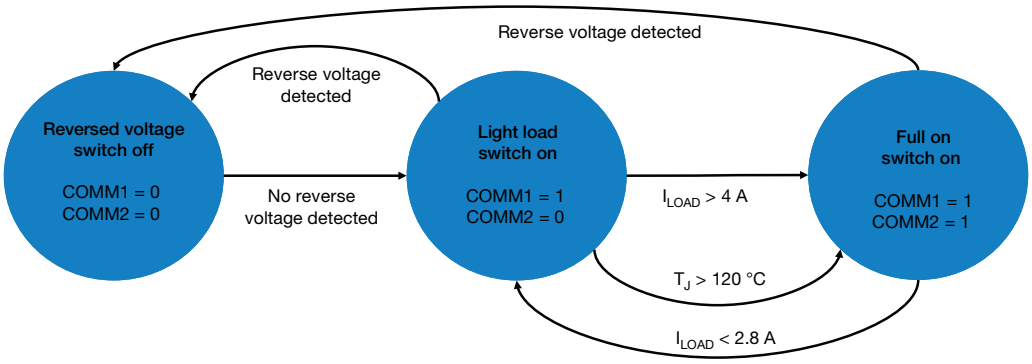

Fig. 5 - Logic State: Master, COMM1 Tied to High Through 100 kΩ

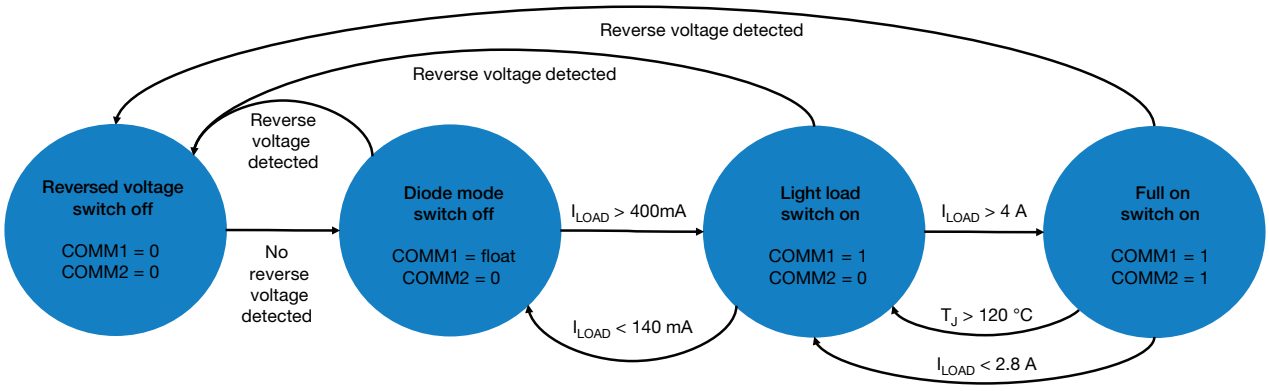

Fig. 6 - Logic State: Master, COMM1 is Floating

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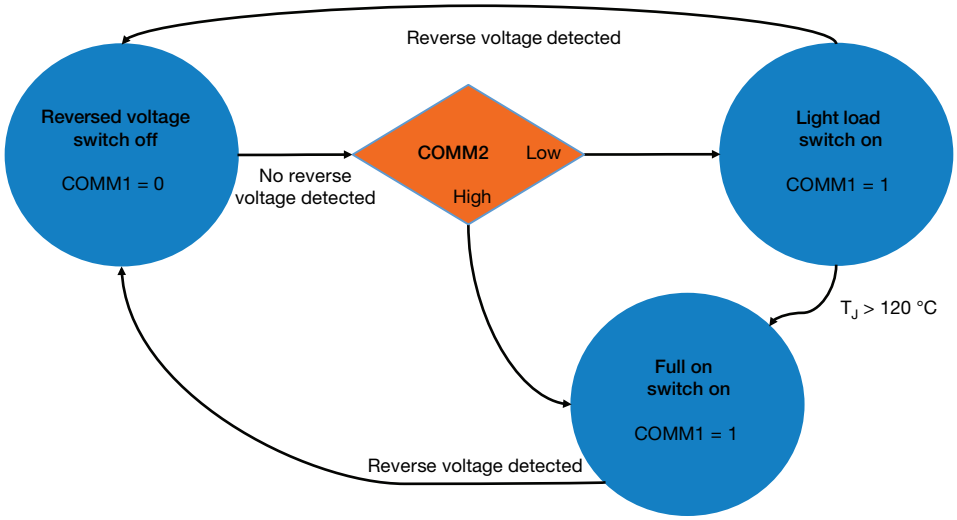

Fig. 7 - Logic State: Slave, COMM1 Tied to High Through 100 kΩ

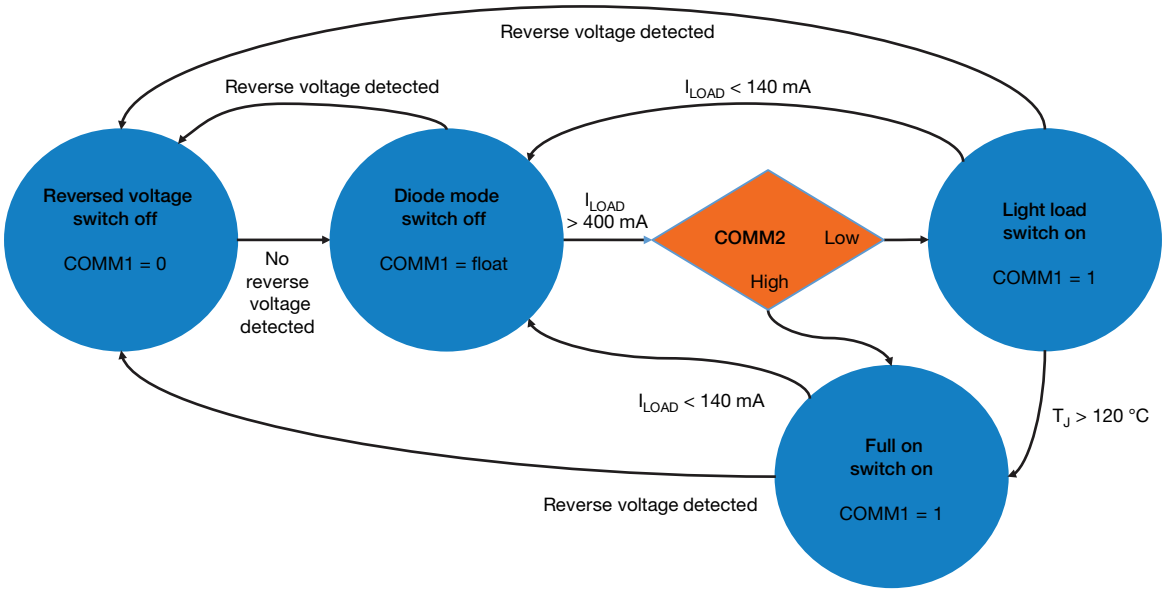

Fig. 8 - Logic State: Slave, COMM1 is Floating

The I_{MON} only reports switch forward current, which flows out of the source (V_{OUT}) pins.

The I_{MON} pin should never be left floating and should be grounded if unused.

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Operation of T_{MON}

T_{MON} is an output pin, used to monitor the device temperature. Over temperature alert is activated either if the controller detects temperature 150 °C, or higher and is signaled by outputting a logic high of 2.5 V, or higher on the T_{MON} pin. Over temperature alert has 20 °C hysteresis.

When over temperature alert is not active, a voltage proportional to the device temperature is produced at the T_{MON} pin. The reported voltage on the T_{MON}

$$V_{TMON} = 800\ mV + 8\ mV/°C \times (t - 25)$$

The T_{MON} pins of multiple devices can be connected and the resulting T_{MON} voltage will correspond to the highest temperature of all devices in the group.
The maximum load of the T_{MON} pin should not exceed 100 kΩ and 100 pF

An OR-ing MOSFET failure causes higher gate leakage, bring excessive load to charge pump. A charge pump malfunction, causing its output to UVLO, will trigger the TMON logic high output alert.

The system design should switch off the current following into the OR-ing circuit.

When T_{MON} is high and there is no reverse condition detected, the internal control circuit will keep the OR-ing at full on mode; even if the load current is in the light load mode range. This is to avoid more heat being generated.

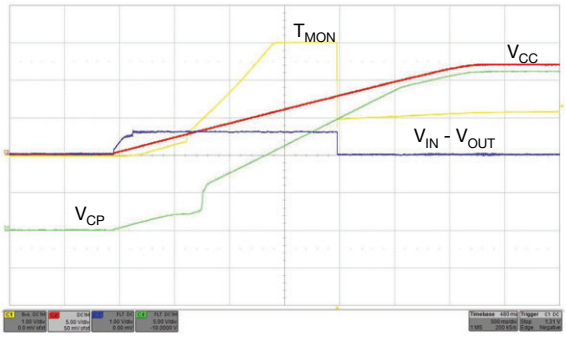

Fig. 9 - T_{MON} During Power Up

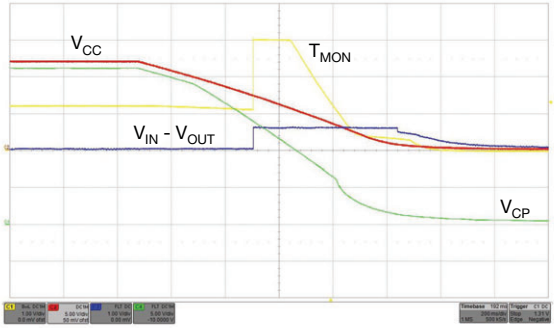

Fig. 10 - T_{MON} During Power Down

Operation of I_{MON}

The I_{MON} pin is an output pin used to report the load current flowing from output pin. The value of the I_{MON} current source is equal to the load current divided by 30 000.

$$I_{MON} = I_{LOAD} / 30\ 000$$

The I_{MON} pins of all paralleled devices on the bus should be tied together and a resistor must be placed from the I_{MON} node to ground. The value of the resistor depends on the number of paralleled devices sharing the bus and the desired full scale I_{MON} voltage.
For a single device design, $R_{IMON} = 30\ 000 \times V_{max.} / I_{max.}$, where $V_{max.}$ is the full scale voltage corresponding to the maximum load current of $I_{max.}$.

For example, to achieve a 2.5 V full scale voltage corresponding to 50 A:

$$R_{IMON} = 30\ 000 \times 2.5\ V / 50\ A = 1.5\ k\Omega$$

When multiple devices in parallel are sharing a bus, R_{IMON} should be divided by N, where N is the number of controllers on the bus. If 4 controllers are used in the previous example, R_{IMON} should be reduced to:

$$R_{IMON} = 30\ 000 \times 2.5\ V / (N \times 50\ A) = 375\ \Omega$$

The SiC32201 I_{MON} pin is designed for a maximum operating voltage of 3.3 V, for proper current reporting.
A filtering capacitor, C_{IMON}, should be placed from I_{MON} to GND, in parallel with the R_{IMON}. The value of C_{IMON} should meet the requirements below:

$$C_{IMON\ (min.)} \geq \frac{k}{2\pi(f_{INT} / 2) \times R_{IMON}} \quad (1)$$

$$C_{IMON\ (max.)} \leq \frac{T_{1\ \%}}{5R_{IMON}} \quad (2)$$

k is the filtering factor; its minimum value is 1.
f_{INT} is the internal clock frequency of 100 kHz. Per formula (1), the C_{IMON} should be greater than 8.5 nF.
$T_{1\ \%}$ is the maximum reporting delay time system design can tolerate.
In case R_{IMON} is 300 Ω, allowable maximum response delay time is 20 µs, the maximum C_{IMON} is 13 nF.

The graph below shows typical current reporting accuracy vs. load current.

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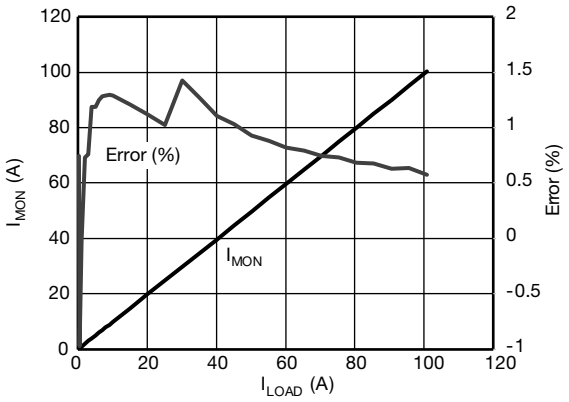

Fig. 11 - Current Reporting Through I_{MON}

The graph below shows typical current reporting error vs load current, when the COMM2 pin is forced high. The switch is forced at full on mode, ignoring the load current level.

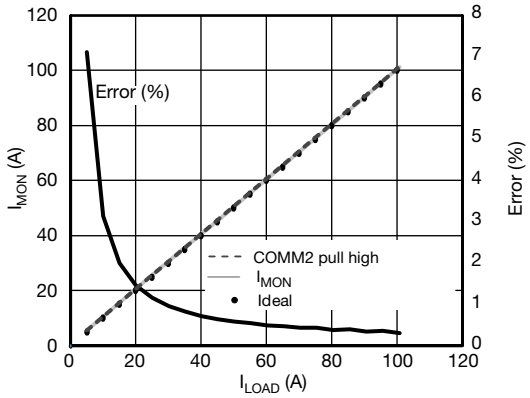

Fig. 12 - Current Reporting Through I_{MON}

The SiC32201 has a low propagation on current reporting. The graphs below show the dynamic current reporting at a single switch, when the load current changes from light to heavy (5 A to 30 A) and heavy to light (from 30 A to 5 A).

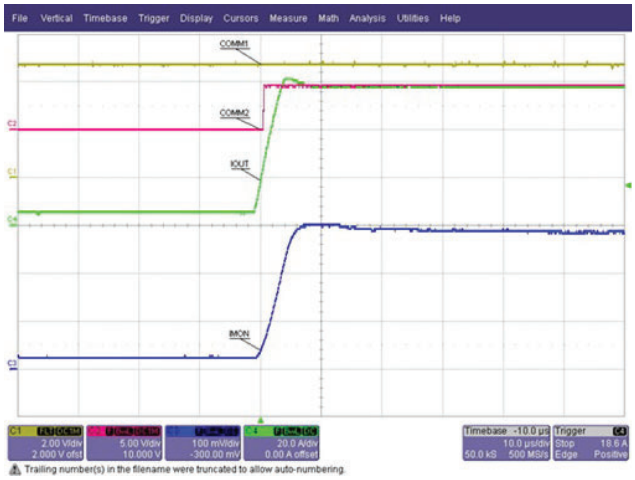

Fig. 13 - I_{MON} Reporting on Load Dynamic, 5 A to 60 A

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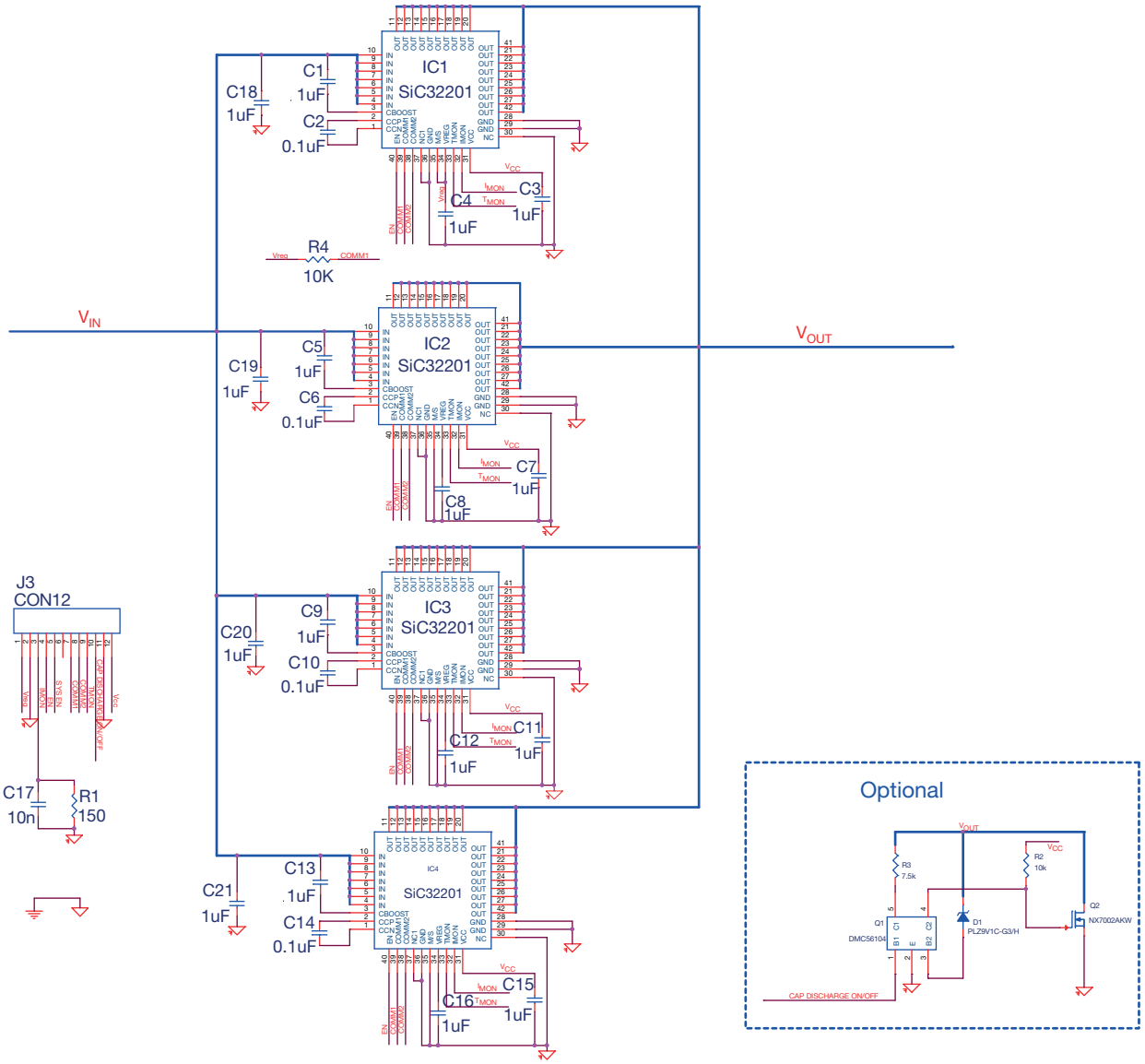

Fig. 14 - Typical Design Schematic of 4 Pieces in Parallel

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Operation of Reverse Blocking

Whenever a reverse condition is detected, the SiC32201 turns off its internal OR-ing FET in 200 ns typically, no matter the status of control pins. Parts in parallel configuration will respond to reverse condition individually for a fast total OR-ing block reverse response time. The V_{OUT} to V_{IN} reverse voltage threshold is typically 6 mV.

In multiple device parallel configuration design, when the forward current through the master switch reduces below 2.8 A, COMM2 will be high. All parallel parts will turn to light load mode; 5.7 mΩ switch resistance. The reverse current is about 1 A plus that will trigger the protection.

Typical, a 3 kW design using 7 pieces in parallel shows 14 A peak reverse current, when tested input short at product performance evaluation. The test set up is per diagram below. The COMM1 nodes are pulled high.

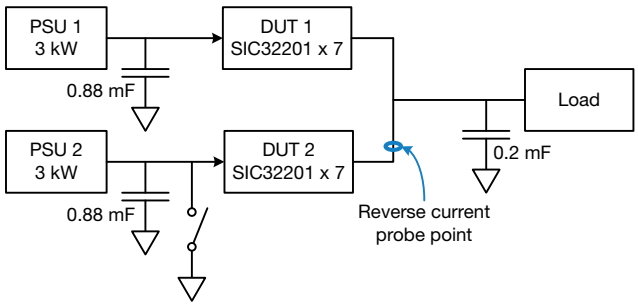

Fig. 15 - Operation of Reverse Blocking

PCB LAYOUT RECOMMENDATIONS

Two PCB layout recommendations are provided below. One is with OR-ing switches on one side of PCB, the other is with the OR-ing switches on both side of PCB board.
In both layout recommendations, the inner 3 and inner 4 are optional for better thermal performance.
The layout recommendations are of 4 paralleled OR-ing switches as example. Designs with more switches in parallel can use the same guideline.
The recommendations are done with consideration of fitting CRPS AC/DC designs.

RECOMMENDED LAYOUT		
LAYER	**DESCRIPTION**	**NOTE**
Top	IC and passive components placement	-
Inner 1	Ground plane	This ground plane helps to shield I_{MON}, T_{MON}, and other noise sensitive signal paths
Inner 2	Signals such as I_{MON}, T_{MON} etc.	-
Inner 3	Ground plane	Optional layers
Inner 4	Power plane	
Bottom	IC and passive components placement	-

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PCB LAYOUT RECOMMENDATIONS

Layout option 1, all OR-ing switches are on top layer

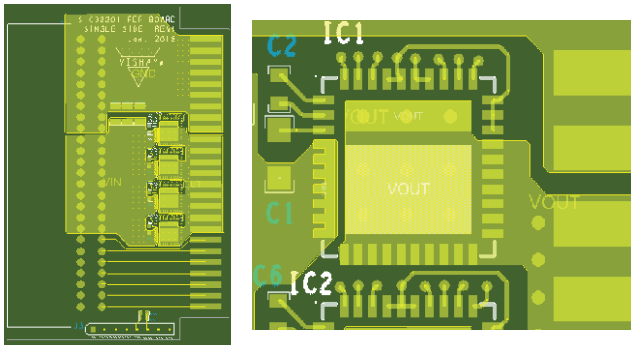

Fig. 16 - Top Layer

1. The charge pump flying capacitor (C2) and charge pump output capacitor (C1) should be put as close to the IC as possible
5. With this option, the decouple capacitors for V_{REG} (C4) and V_{CC} (C3) pins are placed on the bottom side and connected through VIAs
6. Power plane for V_{IN}, V_{OUT} and P_{GND} are in this layer for better thermal performance
7. VIAs can be placed underneath the package to get better thermal performance. Please consult assembly house for IVA size and pitch. A typical thermal VIA diameter is 0.2 mm to 0.4 mm. A thermal VIAs array of pitch 1 mm to 0.2 mm pitch can be a reasonable starting point for most design cases. This can be optimized further per designs and applications

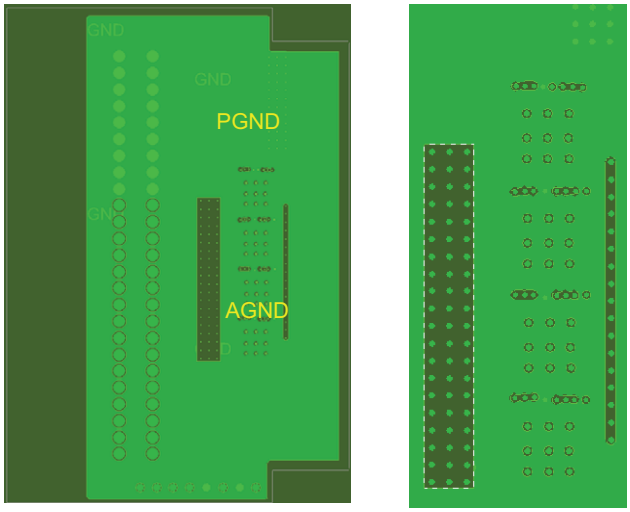

Fig. 17 - Inner 1 Layer

8. Inner 1 layer is a ground plane. Connect the IC A_{GND} pin with this layer through a VIA to minimize the inductance between IC A_{GND} and P_{GND}

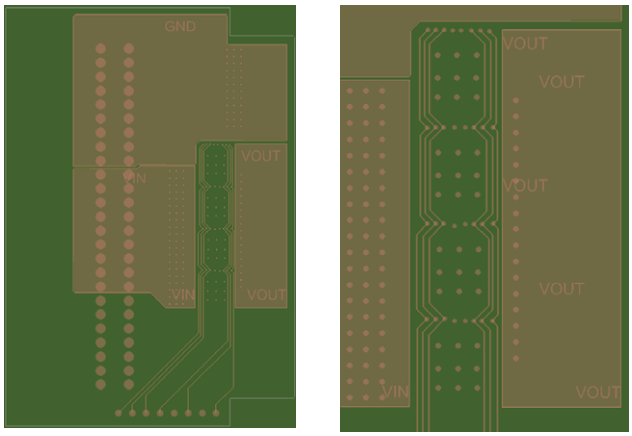

Fig. 18 - Inner 2 Layer

1. This is low power signal layer. Device control, communication, and reporting signal are routed in this layer. They include I_{MON}, T_{MON}, V_{CC}, COMM1, COMM2, and EN signals

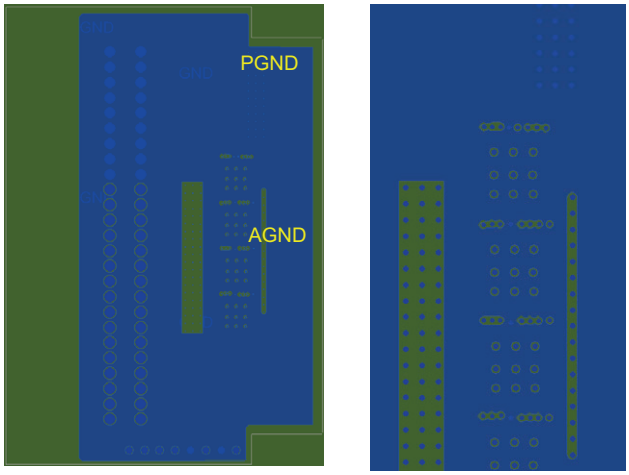

Fig. 19 - Inner 3 Layer

1. The layer can be a duplicated layer of inner 1 layer to further lower the A_{GND} and P_{GND} inductance. Meanwhile, the two ground layers will sandwiched all the signals and provide noise shield

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PCB LAYOUT RECOMMENDATIONS

Layout option 1, all OR-ing switches are on top layer

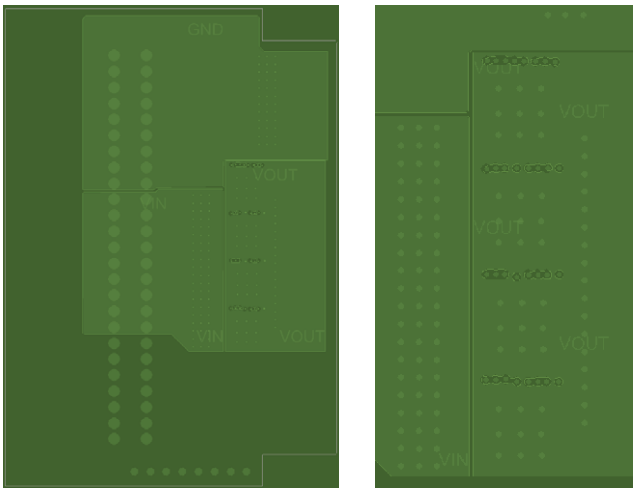

Fig. 20 - Inner 4 Layer

1. Power plane for high current path including V_{IN}, V_{OUT}, and PGN

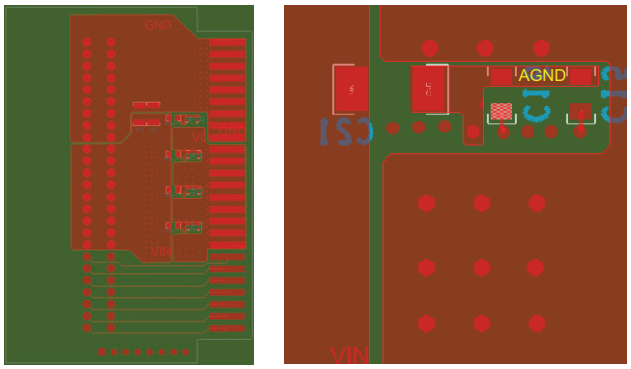

Fig. 21 - Bottom Layer

1. Place V_{CC}, V_{REG} decoupling capacitors as close to the VIAs as possible
2. Plane connected is recommended A_{GND}
3. A 1 µF decoupling capacitor (C20) between V_{IN} and A_{GND} is recommended
4. Power plane for high current path like V_{IN}, V_{OUT} and P_{GND} can be placed in this layer to get better thermal performance

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PCB LAYOUT RECOMMENDATIONS

Layout option 2, OR-ing switches are on both top and bottom layers

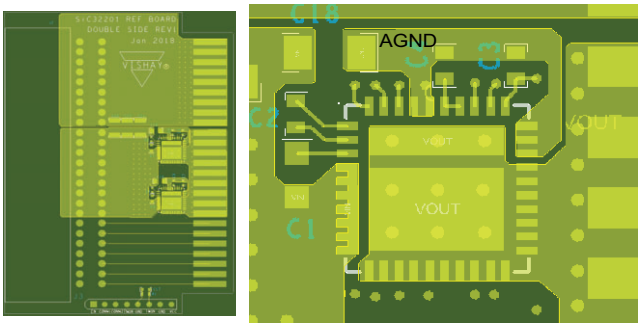

Fig. 22 - Top Layer

1. Put the charge pump flying cap (C2) and charge pump output capacitor (C1) closed to the IC
2. Put the V_{CC} (C3) and V_{REG} (C4) decoupling capacitors close to the IC
3. Analog ground plane is recommended
4. A 1 µF decoupling capacitor (C18) between V_{IN} and A_{GND} is recommended
5. Power plane for high current path like V_{IN}, V_{OUT}, and P_{GND} are in this layer for better thermal performance
6. VIAs can be placed underneath the package to get better thermal performance. Please consult assembly house for IVA size and pitch. A typical thermal VIA diameter is 0.2 mm to 0.4 mm. A thermal VIAs array of pitch 1 mm to 0.2 mm pitch can be a reasonable starting point for most design cases. This can be optimized further per designs and applications

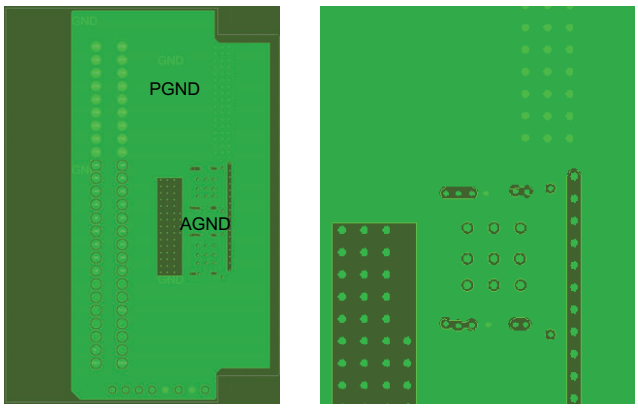

Fig. 23 - Inner 1 Layer

1. Inner 1 layer is a ground plane. Connect the IC A_{GND} Pin with this layer through a VIA to minimize the inductance between IC A_{GND} and P_{GND}

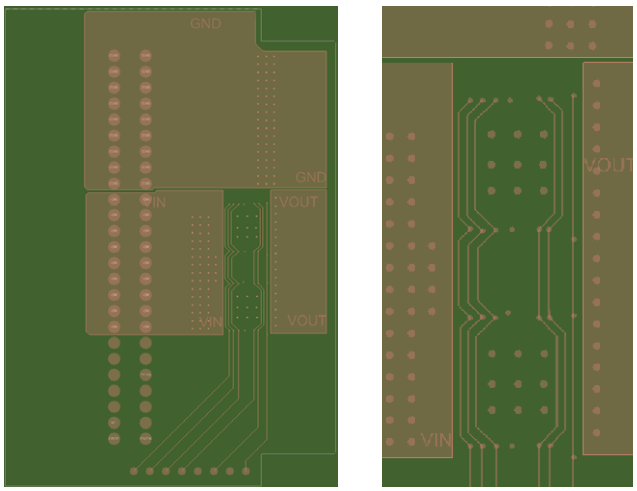

Fig. 24 - Inner 2 Layer

1. This is low power signal layer. Device control, communication, and reporting signal are routed in this layer. They include I_{MON}, T_{MON}, V_{CC}, COMM1, COMM2, and EN signals

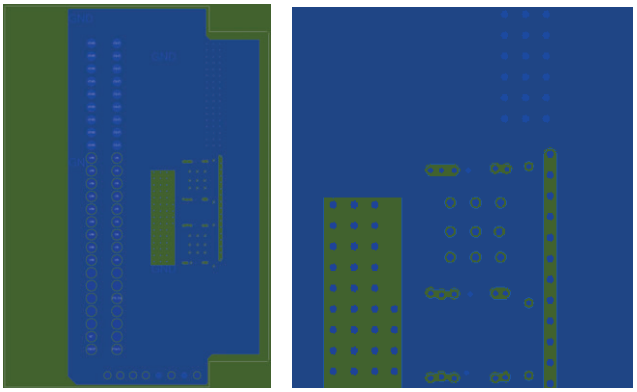

Fig. 25 - Inner 3 Layer

1. The layer can be a duplicated layer of inner 1 layer to further lower the A_{GND} and P_{GND} inductance. Meanwhile, the two ground layers will sandwiched all the signals and provide noise shield

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PCB LAYOUT RECOMMENDATIONS

Layout option 2, OR-ing switches are on both top and bottom layers

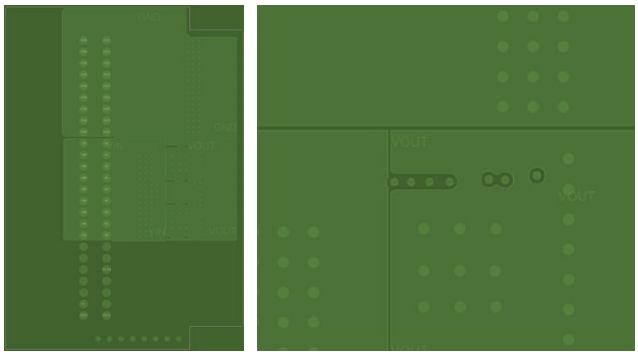

Fig. 26 - Inner 4 Layer

1. Power plane for high current path including V_{IN}, V_{OUT}, and PGN

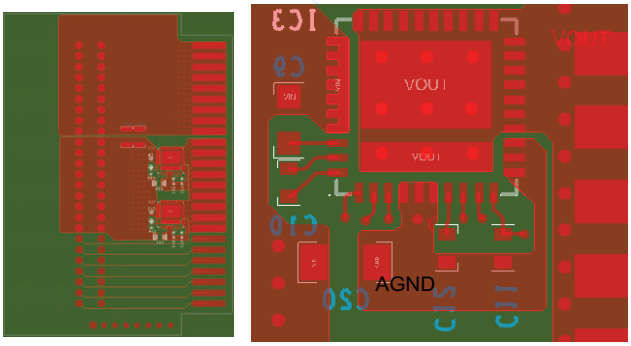

Fig. 27 - Bottom Layer

1. Put the charge pump flying capacitor (C10) and charge pump output capacitor (C9) close to the IC
2. Put V_{CC} (C11) and V_{REG} (C12) decoupling capacitors close to the IC
3. Plane connected is recommended A_{GND}
4. A 1 µF decoupling capacitor (C20) between V_{IN} and A_{GND} is recommended
5. Power plane for high current path like V_{IN}, V_{OUT}, and P_{GND} can be placed in this layer to get better thermal performance

LAYOUT CONSIDERATION

- Decoupling capacitors for V_{CC} and V_{REG}, charge pump flying capacitor and its output capacitor need to placed close to the related pins of the IC to minimize the stray inductance
- The inner 1 ground layer helps to shield I_{MON}, T_{MON}, and other noise sensitive signal paths
- There is a built-in charger pump in SiC32201, therefore no floating power supply from auxiliary winding is required. The charge pump and other circuits take V_{IN} as a reference. Excessive stray inductance between P_{GND} of V_{IN} and A_{GND} of the IC may impact performance of the SiC32201. To ensure the proper circuit performance, IC A_{GND} needs to be as close as possible to P_{GND} of the V_{IN} rail to minimize the stray inductance. Also a capacitor between V_{IN} and A_{GND} of the IC is highly recommended

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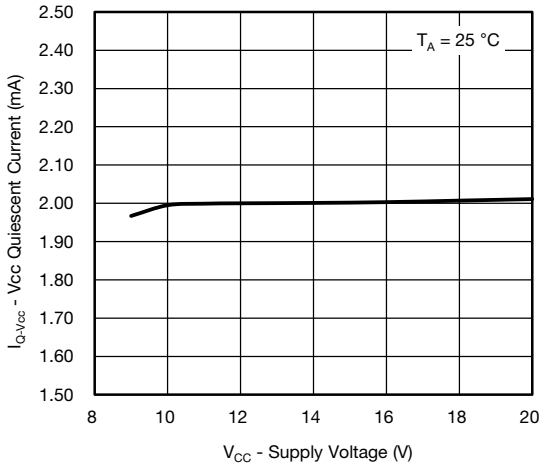

Fig. 28 - Quiescent Current vs. Supply Voltage

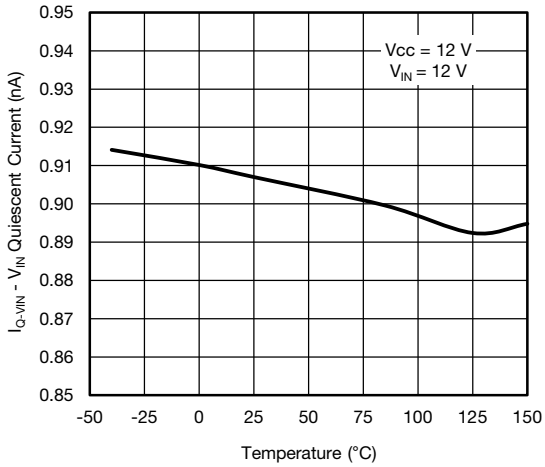

Fig. 31 - Quiescent Current vs. Temperature

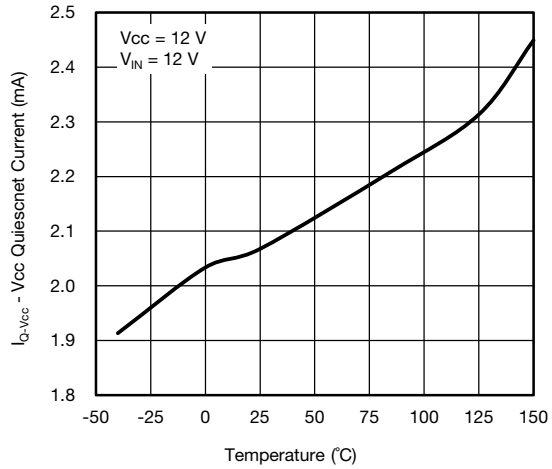

Fig. 29 - Quiescent Current vs. Supply Voltage

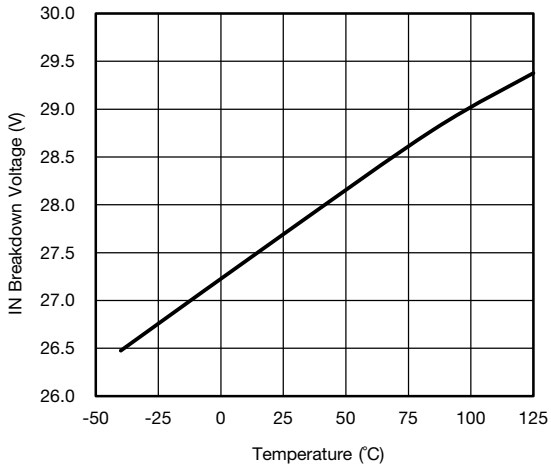

Fig. 32 - Breakdown Voltage vs. Temperature

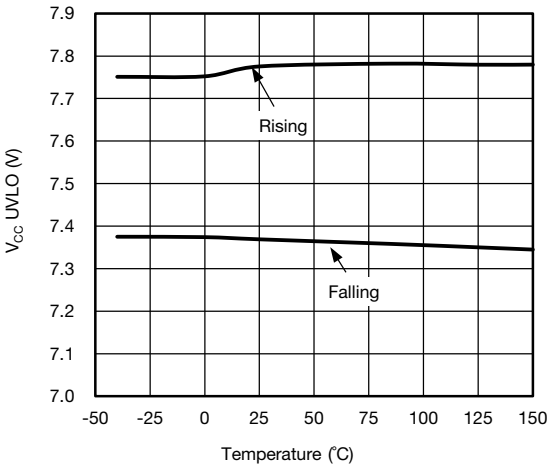

Fig. 30 - UVLO vs. Temperature

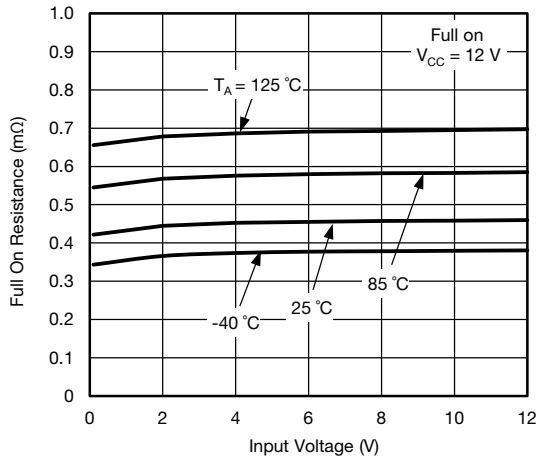

Fig. 33 - Full On Resistance vs. Input Voltage

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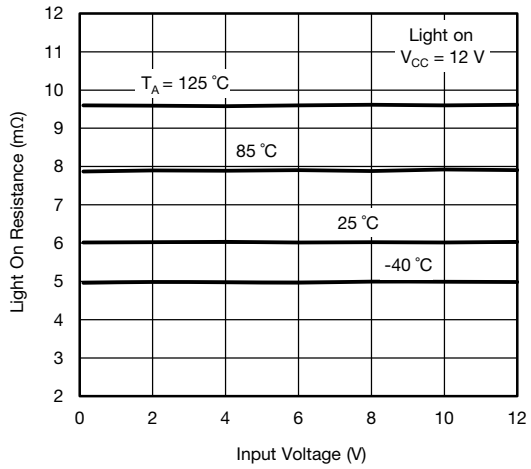

Fig. 34 - Light On Resistance vs. Input Voltage

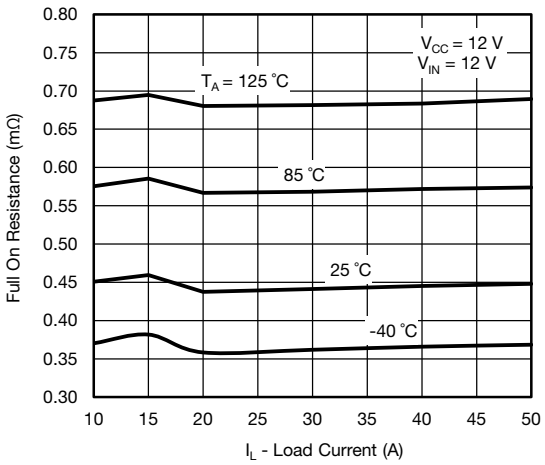

Fig. 37 - Full On Resistance vs. Load Current

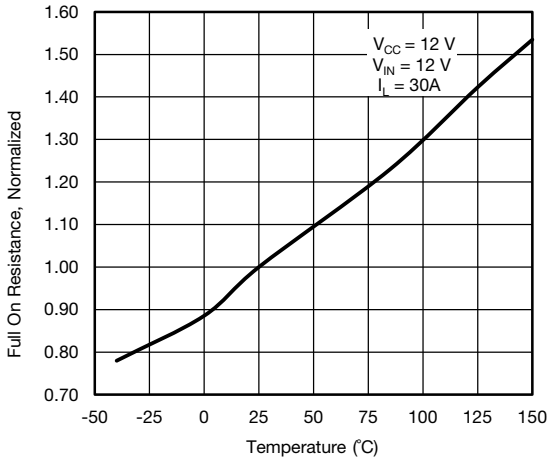

Fig. 35 - Full On Resistance vs. Temperature

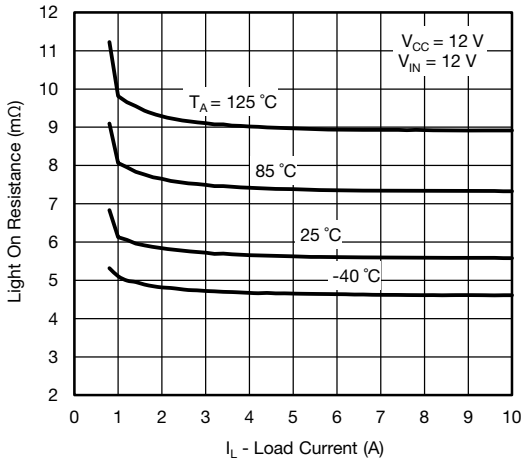

Fig. 38 - Light On Resistance vs. Load Current

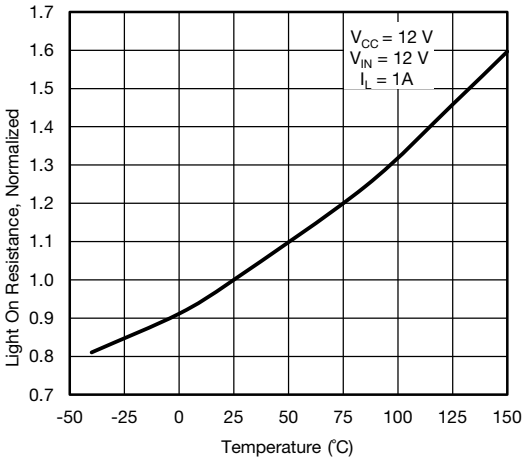

Fig. 36 - Light On Resistance vs. Temperature

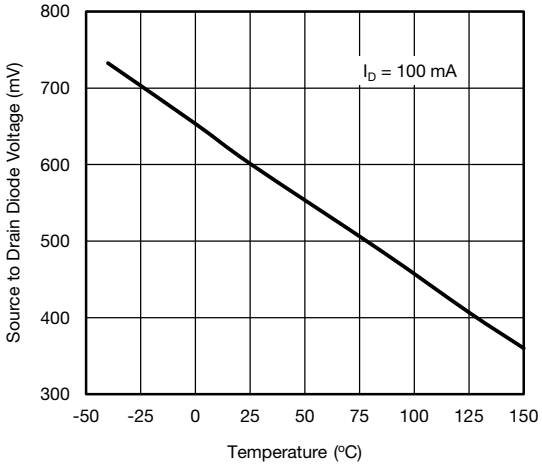

Fig. 39 - Source to Drain Diode Voltage vs. Temperature

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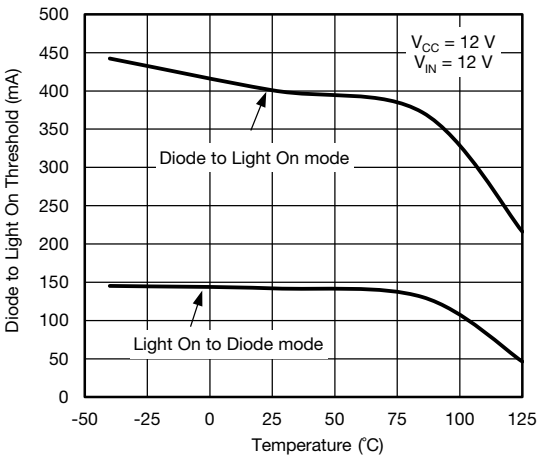

Fig. 40 - Diode to Light On Threshold vs. Temperature

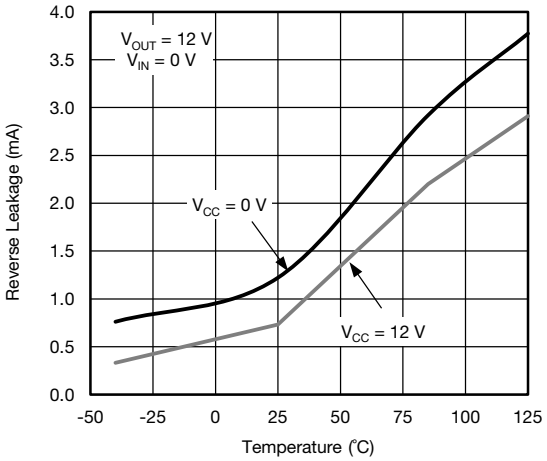

Fig. 43 - Reverse Leakage vs. Temperature

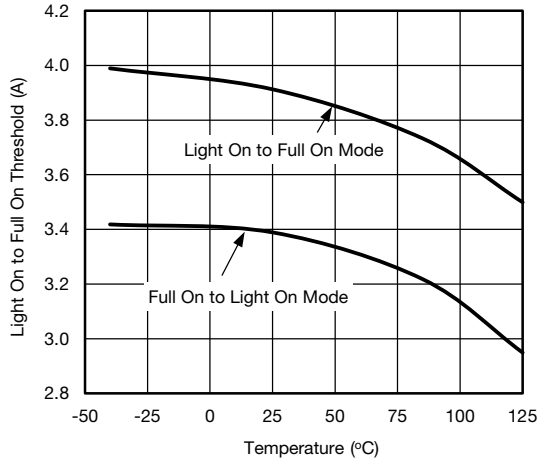

Fig. 41 - Light On to Full On Threshold vs. Temperature

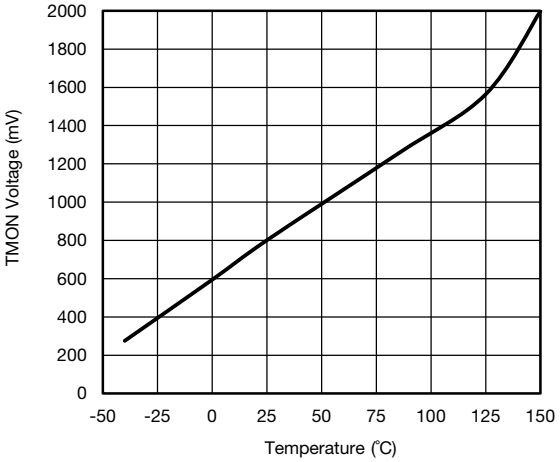

Fig. 44 - T_{MON} Voltage vs. Temperature

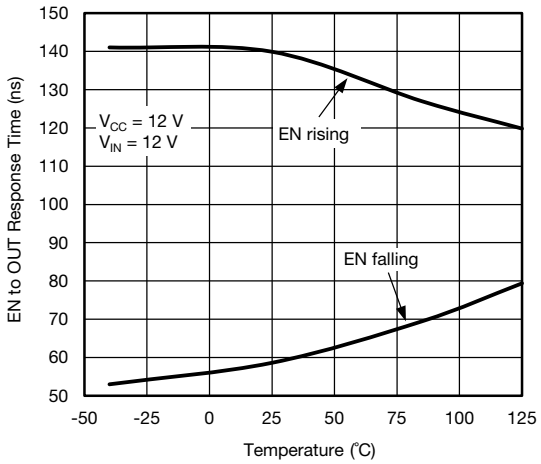

Fig. 42 - EN to Out Response Time vs. Temperature

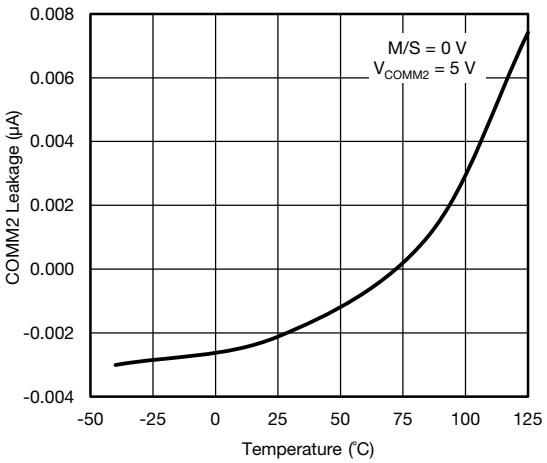

Fig. 45 - COMM2 Leakage vs. Temperature

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

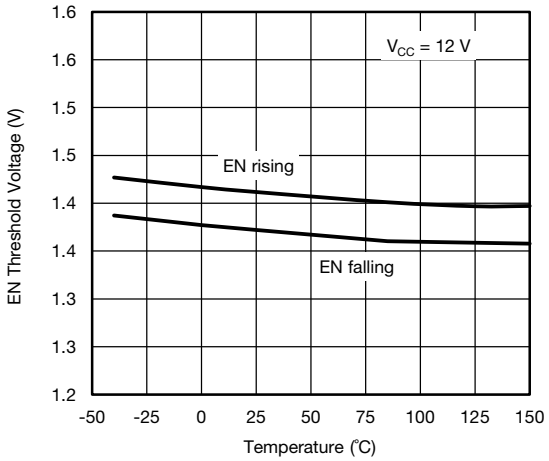

Fig. 46 - EN Threshold Voltage vs. Temperature

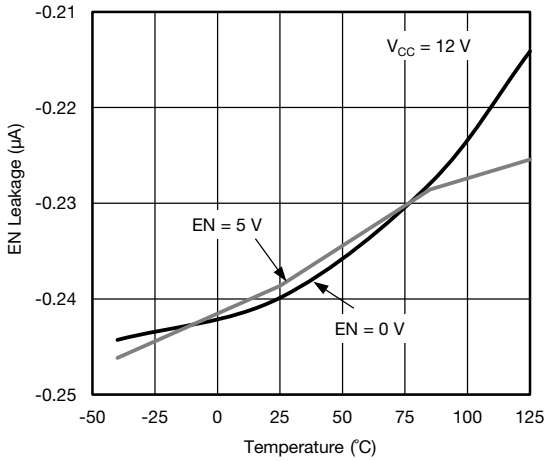

Fig. 47 - EN Leakage vs. Temperature

PRODUCT SUMMARY	
Part number	SiC32201
Description	0.45 mO, integrated OR-ing switch with OR-ing controller, lossless current sense, and temperature report
Configuration	Parallelable
Slew rate time (µs)	-
On delay time (µs)	-
Input voltage min. (V)	9
Input voltage max. (V)	18
On-resistance at input voltage min. (mΩ)	-
On-resistance at input voltage max. (mΩ)	0.45
Quiescent current at input voltage min. (µA)	-
Quiescent current at input voltage max. (µA)	1800
Output discharge (yes / no)	No
Reverse blocking (yes / no)	Yes
Continuous current (A)	100
Package type	PowerPAK® MLP66-40L
Package size (W, L, H) (mm)	6.0 x 6.0 x 0.75
Status code	1
Product type	OR-ing switch
Applications	Redundant power supply, server, data center, cloud computing

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