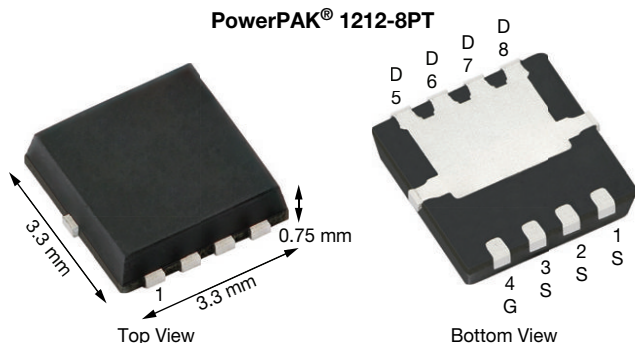


N-Channel 40 V (D-S) MOSFET



PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0074
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0096
Q_g typ. (nC)	14.2
I_D (A)	65
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 1212-8PT
Lead (Pb)-free and halogen-free	Si7116BDN-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	40	V	
Gate-source voltage	V_{GS}	± 20		
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	65	A	
	$T_C = 70$ °C	52		
	$T_A = 25$ °C	18.4 ^{b, c}		
	$T_A = 70$ °C	14.7 ^{b, c}		
Pulsed drain current ($t = 100$ μ s)	I_{DM}	100		
Continuous source-drain diode current	$T_C = 25$ °C	57		
	$T_A = 25$ °C	4.5 ^{b, c}		
Single pulse avalanche current	$L = 0.1$ mH	30		
Single pulse avalanche energy	E_{AS}	45	mJ	
Maximum power dissipation	$T_C = 25$ °C	62.5	W	
	$T_C = 70$ °C	40		
	$T_A = 25$ °C	5 ^{b, c}		
	$T_A = 70$ °C	3.2 ^{b, c}		
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) ^c		260		

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^b	$t \leq 10$ s	R_{thJA}	20	25	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.4	2.0	

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 60 °C/W

FEATURES

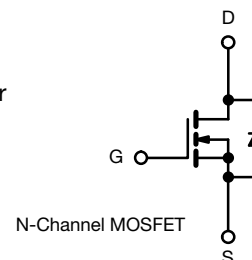
- TrenchFET® Gen IV power MOSFET
- Very low Q_g and Q_{oss} reduce power loss and improve efficiency
- Optimized Q_g , Q_{gd} , and Q_{gd}/Q_{gs} ratio reduces switching related power loss
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- Synchronous buck converter
- High power density DC/DC
- Load switching



N-Channel MOSFET



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	40	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	52	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J		-	1.1	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5	-	2.5	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 16 A	-	0.0060	0.0074	Ω
		V _{GS} = 4.5 V, I _D = 15 A	-	0.0075	0.0096	
Forward transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 25 A	-	80	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	-	1915	-	pF
Output capacitance	C _{oss}		-	230	-	
Reverse transfer capacitance	C _{rss}		-	95	-	
C _{rss} /C _{iss} ratio			-	0.050	0.100	
Total gate charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 16 A	-	31.4	48	nC
		V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 16 A	-	14.2	22	
Q _{gs}	-		6.7	-		
Q _{gd}	-		5.1	-		
Q _{oss}	-	7.1	-			
Gate resistance	R _g	V _{DS} = 20 V, V _{GS} = 0 V	-	7.1	-	Ω
Turn-on delay time	t _{d(on)}	f = 1 MHz	0.2	1.1	2.2	
Rise time	t _r	V _{DD} = 20 V, R _L = 2 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	10	20	
Turn-off delay time	t _{d(off)}		-	5	10	
Fall time	t _f		-	25	50	
Turn-on delay time	t _{d(on)}		-	5	10	
Rise time	t _r	V _{DD} = 20 V, R _L = 2 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	25	50	
Turn-off delay time	t _{d(off)}		-	45	90	
Fall time	t _f		-	22	45	
Fall time	t _f		-	7	15	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	52	A
Pulse diode forward current (t _p = 100 μs)	I _{SM}		-	-	100	
Body diode voltage	V _{SD}	I _S = 5 A	-	0.76	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 5 A, di/dt = 100 A/μs, T _J = 25 °C	-	20	40	ns
Body diode reverse recovery charge	Q _{rr}		-	16	35	nC
Reverse recovery fall time	t _a		-	12	-	ns
Reverse recovery rise time	t _b		-	8	-	

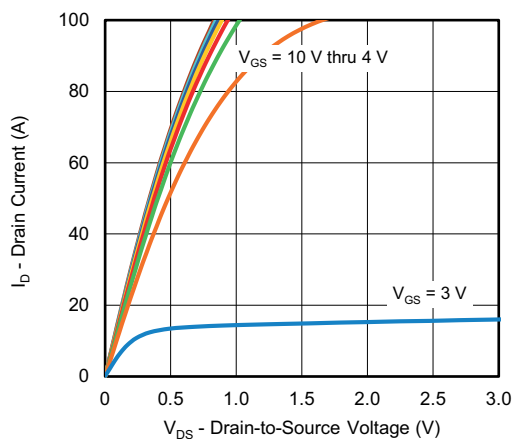
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

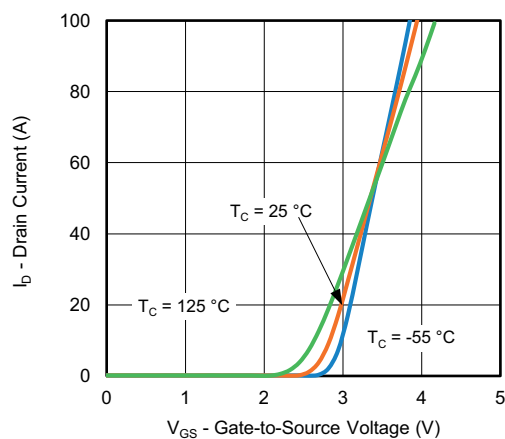
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



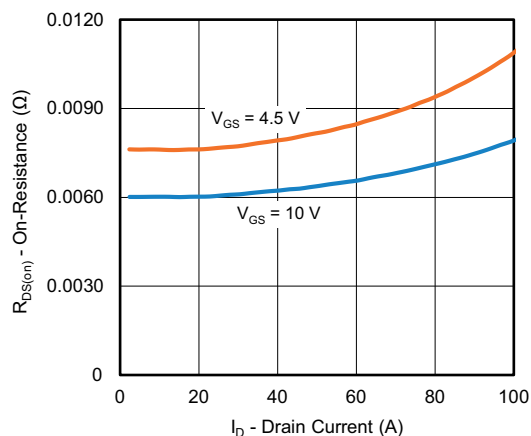
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



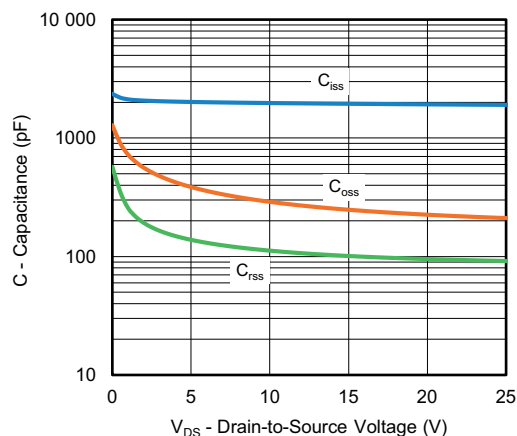
Output Characteristics



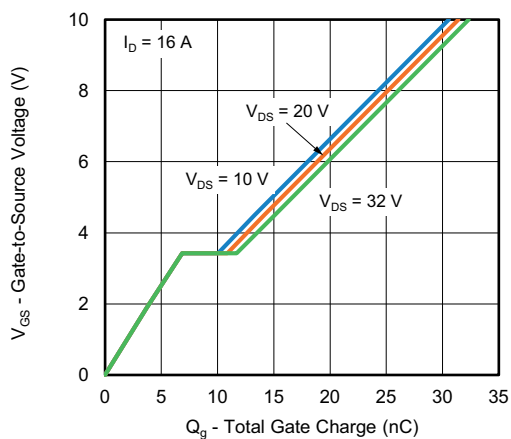
Transfer Characteristics



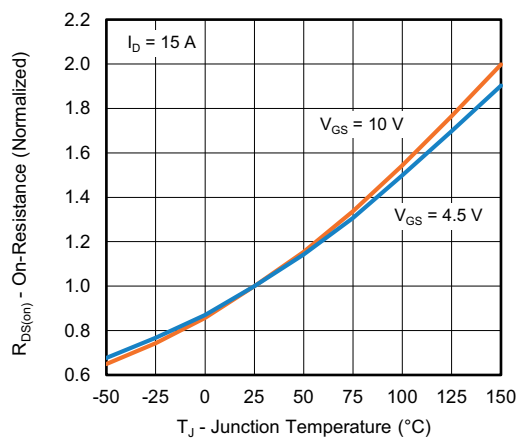
On-Resistance vs. Drain Current



Capacitance



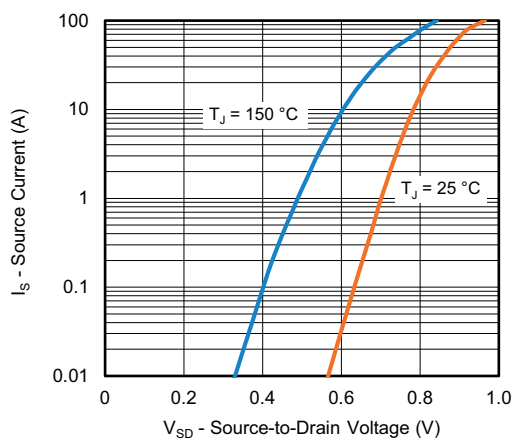
Gate Charge



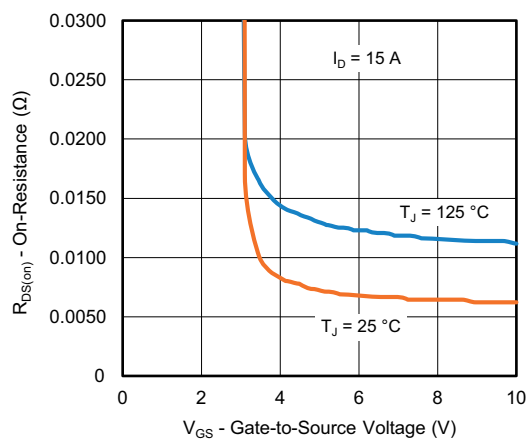
On-Resistance vs. Junction Temperature



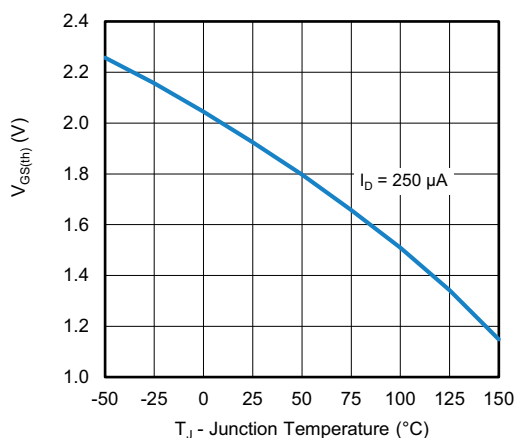
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



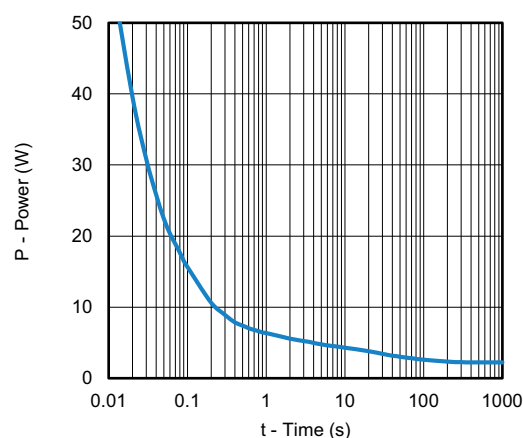
Source-Drain Diode Forward Voltage



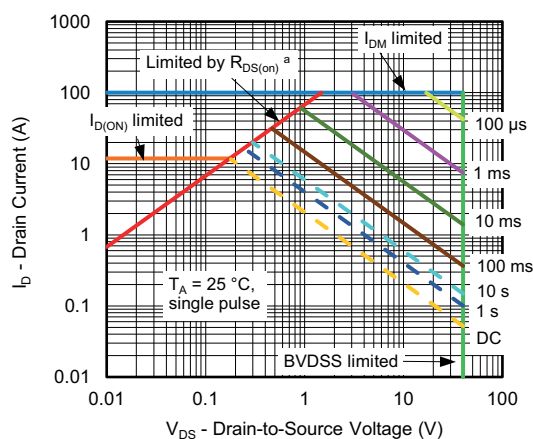
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



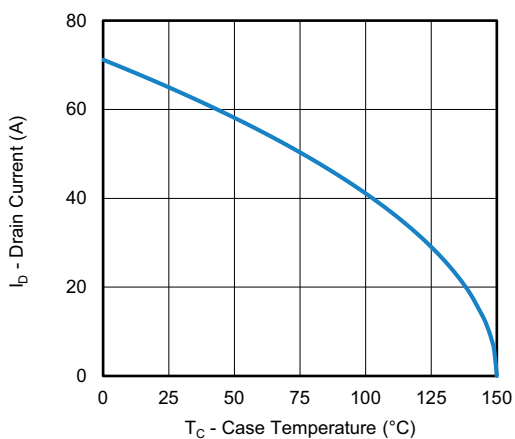
Safe Operating Area

Note

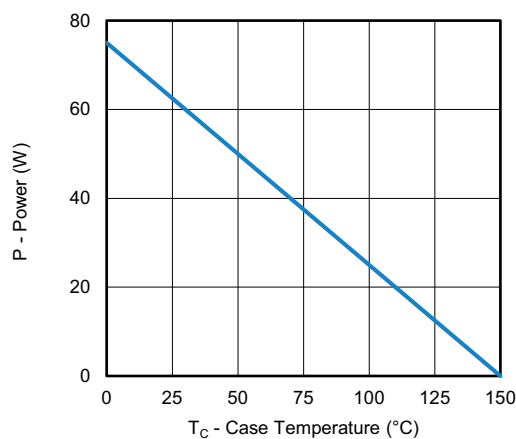
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



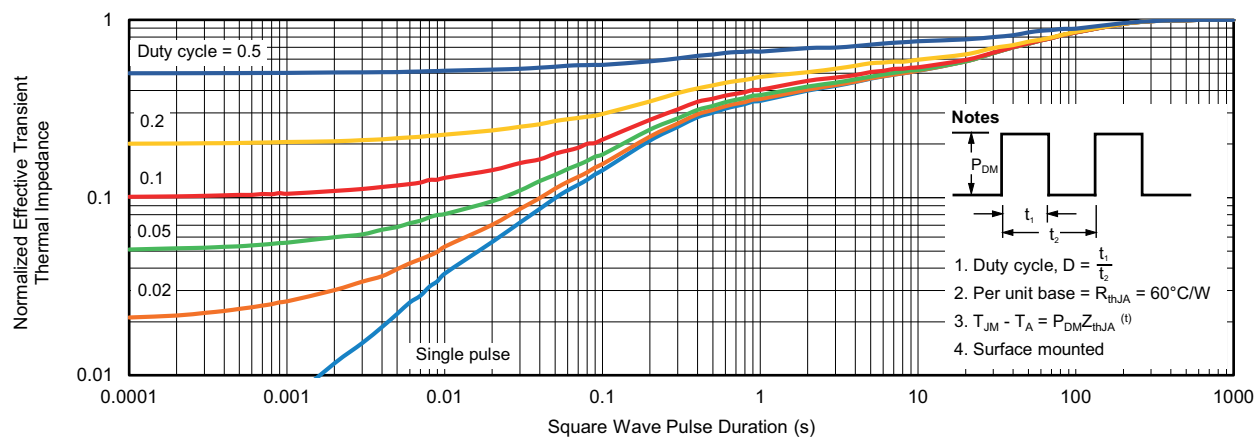
Power, Junction-to-Ambient

Note

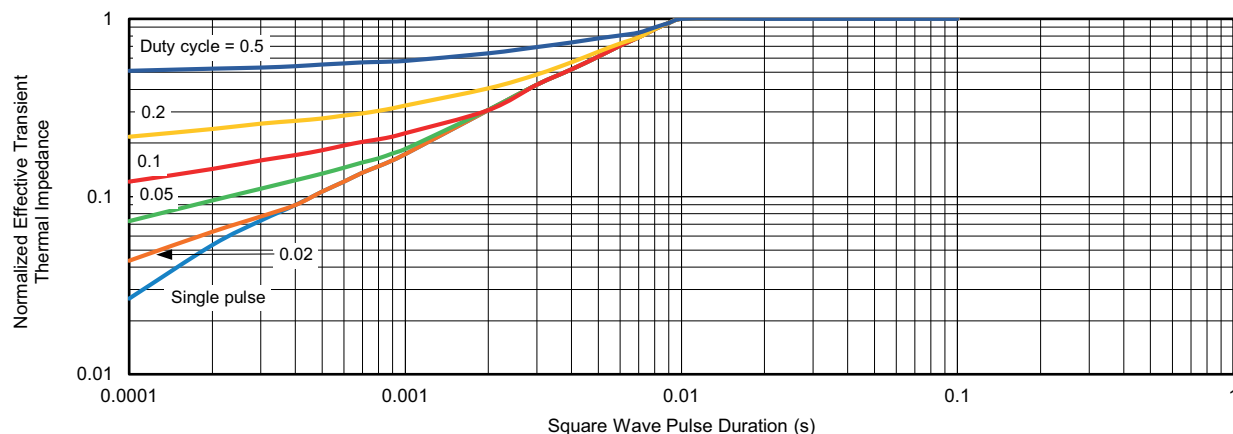
- b. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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