N- and P-Channel 100 V (D-S) MOSFET

DESCRIPTION

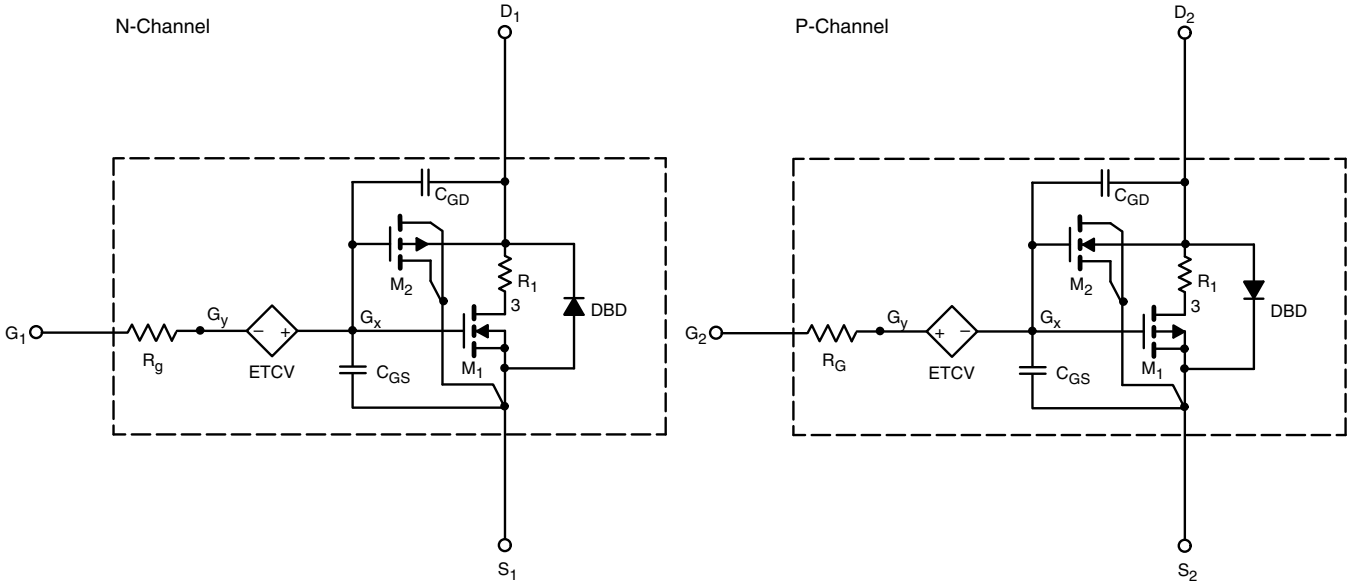
The attached SPICE model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N- and P-Channel Vertical DMOS
- Macro Model (Sub-circuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	2	-	V
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	2	-	
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 2 A	N-Ch	0.045	0.047	Ω
		V_{GS} = -10 V, I_D = -2 A	P-Ch	0.150	0.150	
		V_{GS} = 4.5 V, I_D = 1.5 A	N-Ch	0.060	0.059	
		V_{GS} = -4.5 V, I_D = -1 A	P-Ch	0.170	0.165	
Forward Transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 2 A	N-Ch	9	9	S
		V_{DS} = -15 V, I_D = -2 A	P-Ch	7	9.3	
Diode Forward Voltage [a]	V_{SD}	I_S = 3.6 A, V_{GS} = 0 V	N-Ch	0.83	0.83	V
		I_S = -4 A, V_{GS} = 0 V	P-Ch	-0.83	-0.80	
Dynamic [b]						
Input Capacitance	C_{iss}	N-Channel V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz P-Channel V_{DS} = -50 V, V_{GS} = 0 V, f = 1 MHz	N-Ch	408	360	pF
			P-Ch	1270	1150	
Output Capacitance	C_{oss}		N-Ch	129	130	
			P-Ch	64	65	
Reverse Transfer Capacitance	C_{rss}		N-Ch	19	20	
			P-Ch	40	40	
Total Gate Charge	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 4.5 A	N-Ch	6.8	7.5	nC
		V_{DS} = -50 V, V_{GS} = -10 V, I_D = -5 A	P-Ch	20	24	
		N-Channel V_{DS} = 50 V, V_{GS} = 4.5 V, I_D = 4.5 A P-Channel V_{DS} = -50 V, V_{GS} = -4.5 V, I_D = -5 A	N-Ch	4	4	
			P-Ch	10	11.6	
Gate-Source Charge	Q_{gs}		N-Ch	1.2	1.2	
			P-Ch	3.8	3.8	
Gate-Drain Charge	Q_{gd}		N-Ch	2	2	
			P-Ch	5	5	

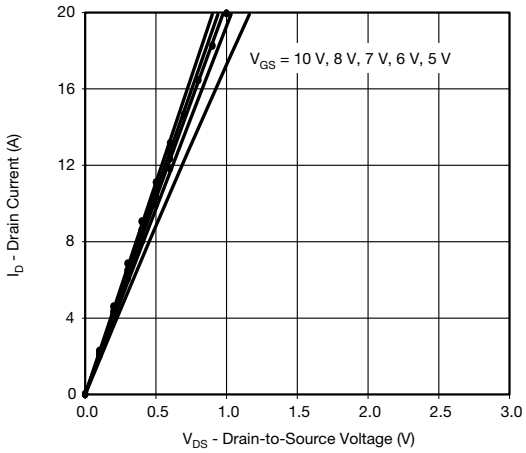
Notes

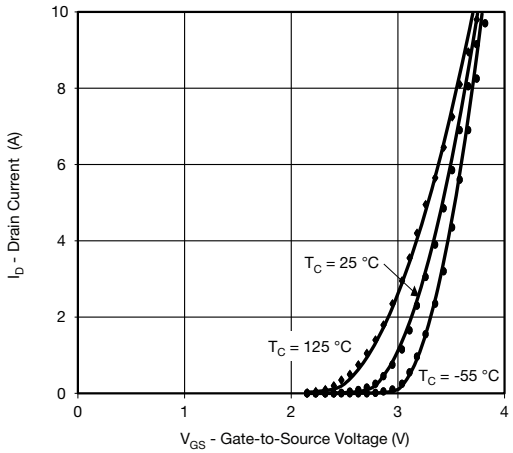
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

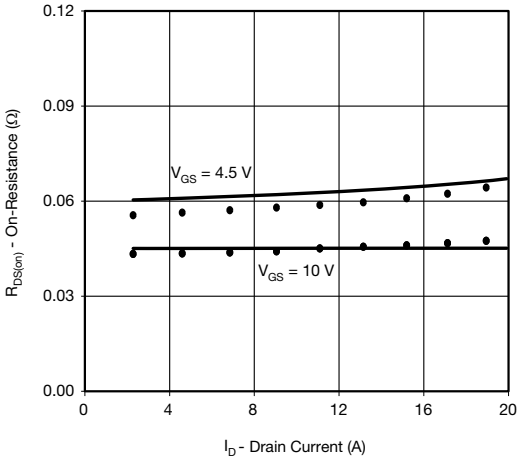
b. Guaranteed by design, not subject to production testing.

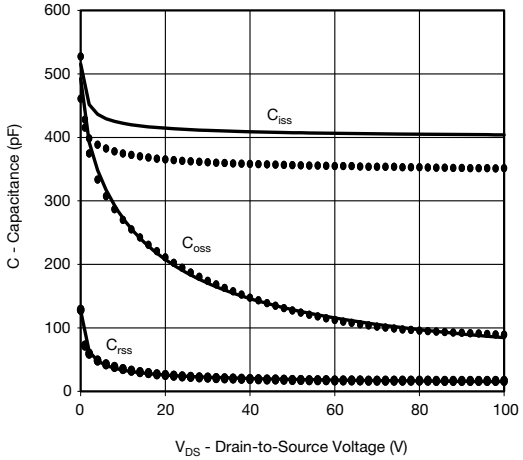
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

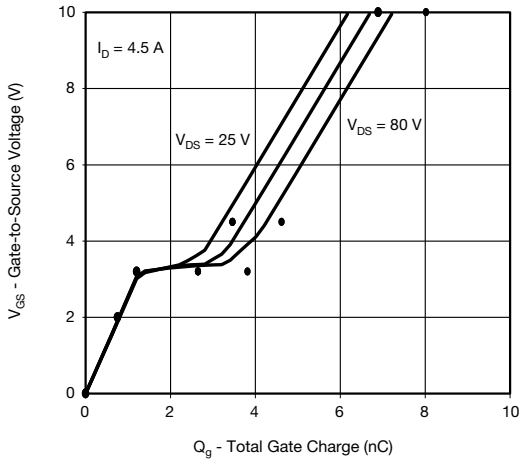
N-Channel MOSFET

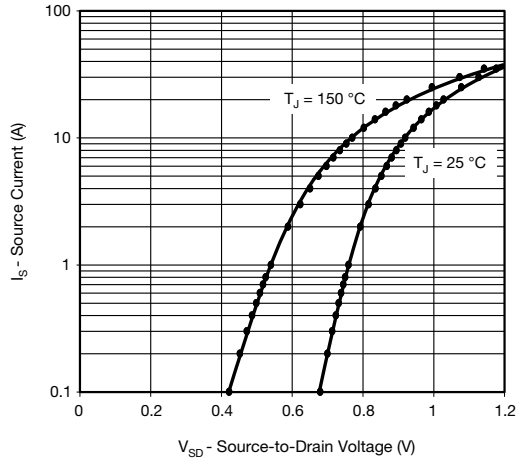










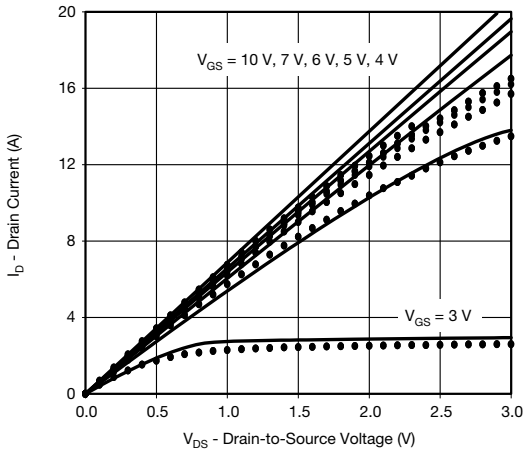


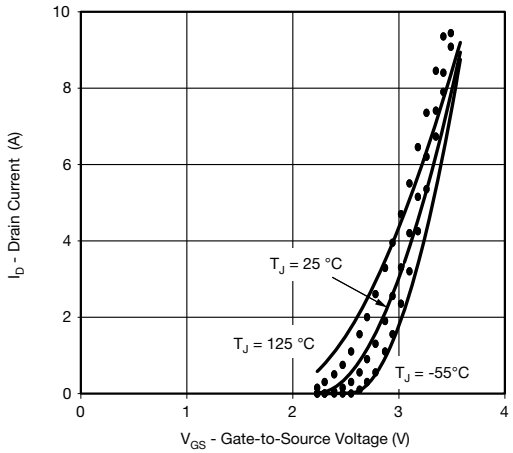
Note

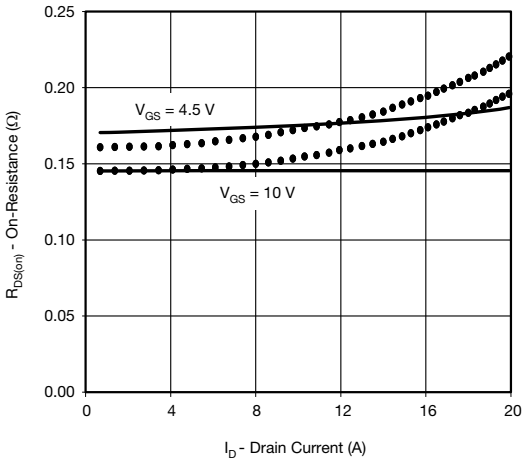
- Dots and squares represent measured data.

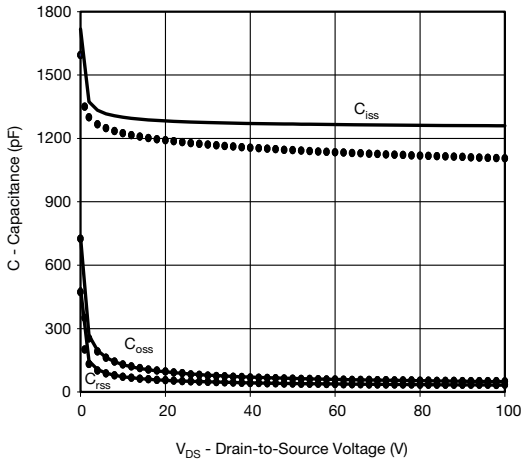
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

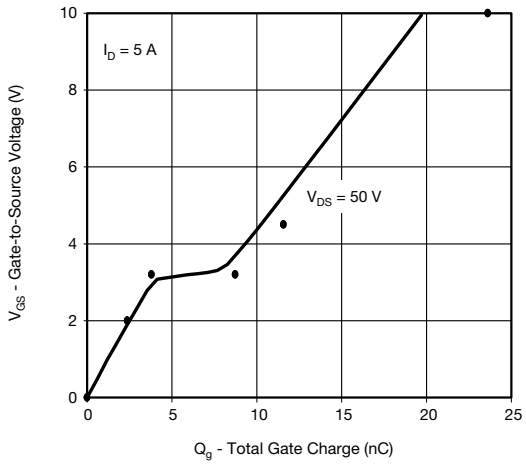
P-Channel MOSFET

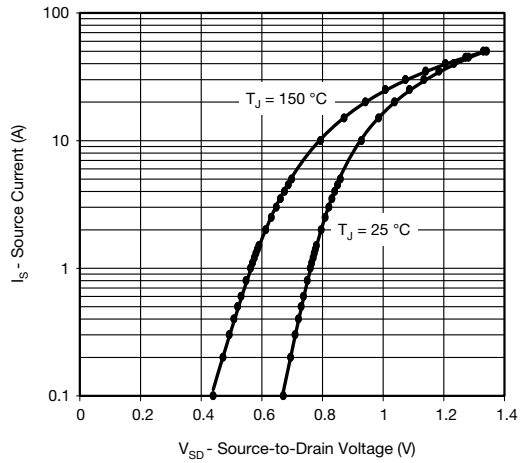












Note

- Dots and squares represent measured data.

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