

## Dual N-Channel 30 V (D-S) MOSFET

### DESCRIPTION

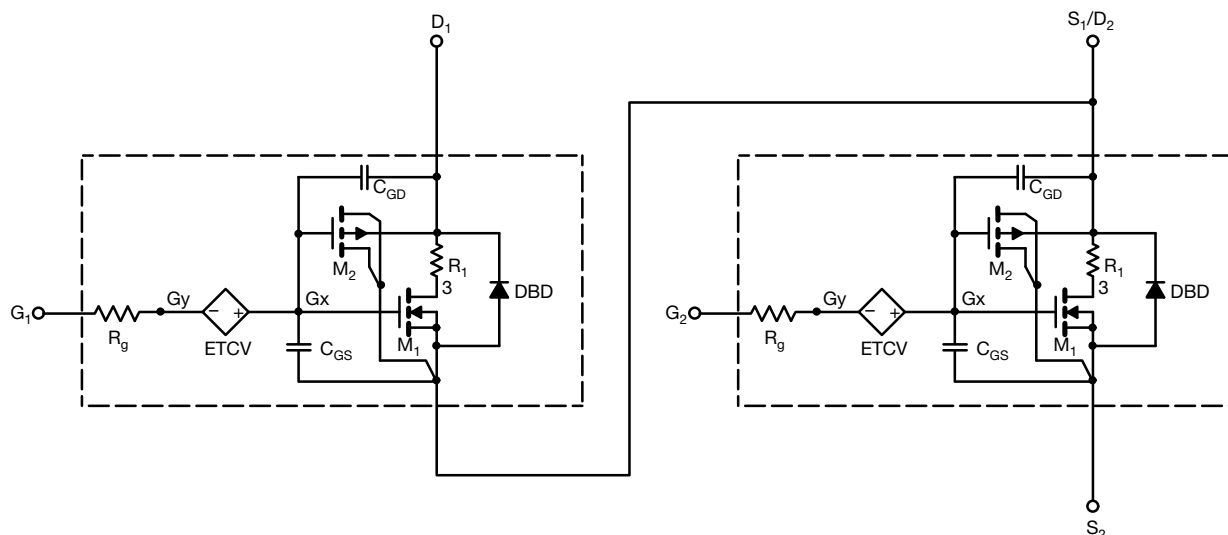
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATE D DATA		MEASURED DATA	UNIT
Static						
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	Ch-1	1.8	-	V
			Ch-2	1.5	-	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	Ch-1	0.0230	0.0230	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 14.4 A	Ch-2	0.0083	0.0084	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A	Ch-1	0.0320	0.0300	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 13 A	Ch-2	0.0100	0.0111	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 A	Ch-1	19	17	S
		V <sub>DS</sub> = 10 V, I <sub>D</sub> = 14.4 A	Ch-2	40	37	
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 5 A, V <sub>GS</sub> = 0 V	Ch-1	0.85	0.87	V
		I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V	Ch-2	0.82	0.80	
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	N-Channel V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz  P-Channel V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	Ch-1	335	325	pF
Output Capacitance	C <sub>oss</sub>		Ch-2	660	650	
			Ch-1	67	66	
Reverse Transfer Capacitance	C <sub>rss</sub>		Ch-2	243	236	
			Ch-1	34	33	
			Ch-2	20	20	
Total Gate Charge	Q <sub>g</sub>	Channel 1 V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A	Ch-1	6	6.6	nC
		Channel 2 V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 14.4 A	Ch-2	10	10	
		Channel 1 V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A	Ch-1	3	3.2	
			Ch-2	4.5	4.5	
Gate-Source Charge	Q <sub>gs</sub>		Ch-1	1.2	1	
			Ch-2	2.1	2.1	
Gate-Drain Charge	Q <sub>gd</sub>	Channel 2 V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 14.4 A	Ch-1	1.6	1.2	
			Ch-2	0.7	0.7	

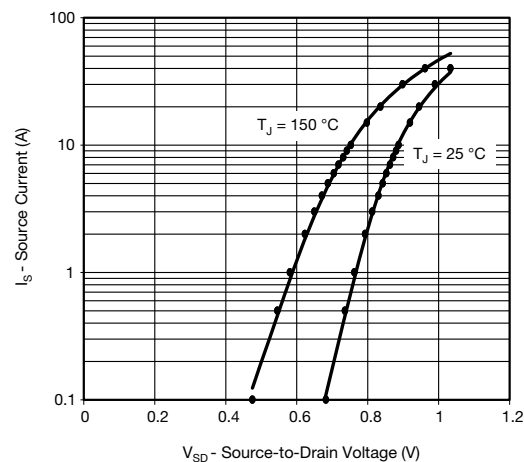
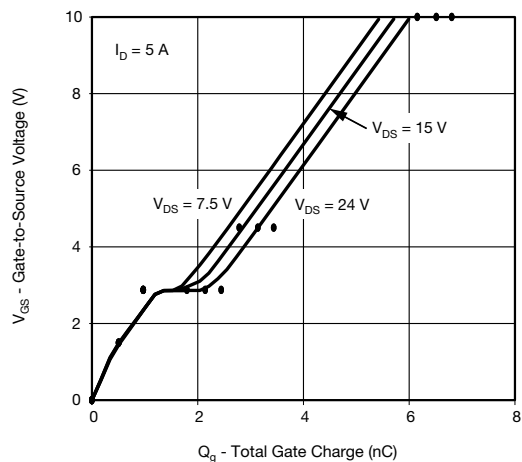
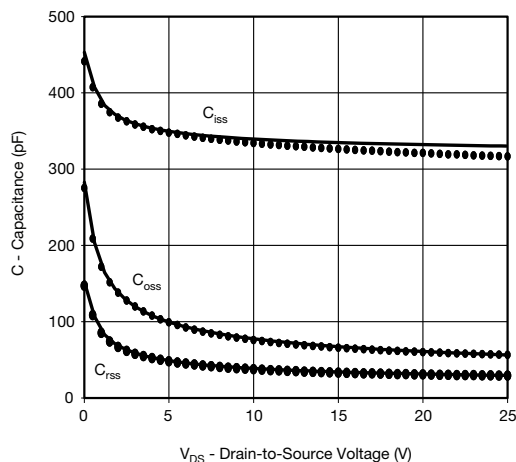
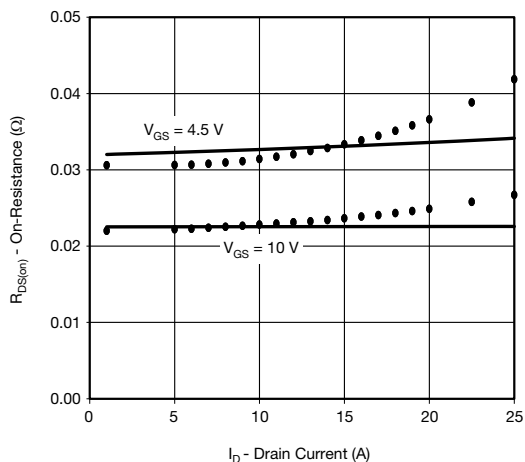
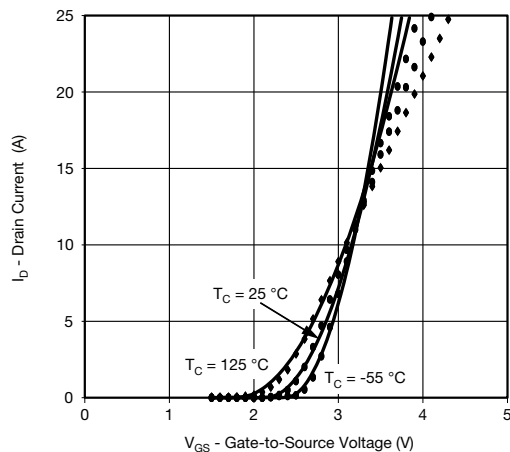
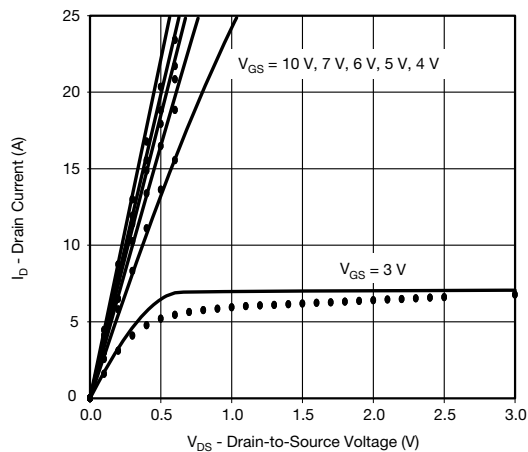
**Notes**

- a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\ \%$   
b. Guaranteed by design, not subject to production testing



## COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25^\circ\text{C}$ , unless otherwise noted

### N-Channel 1 MOSFET



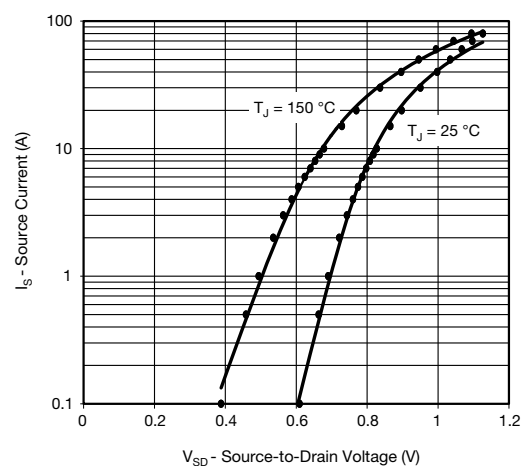
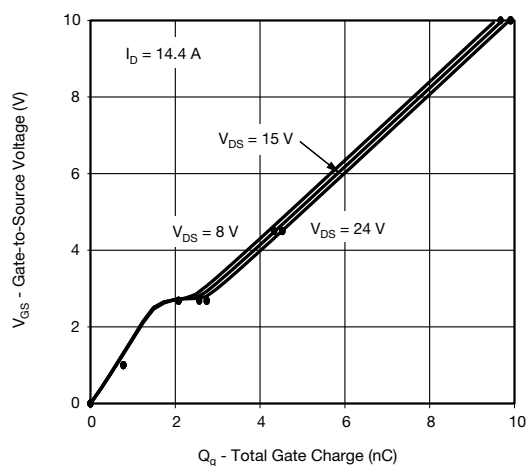
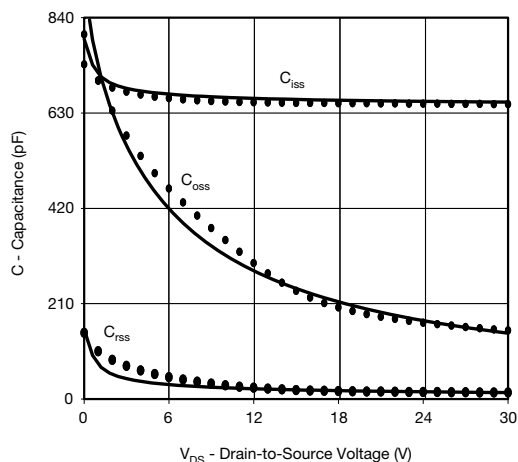
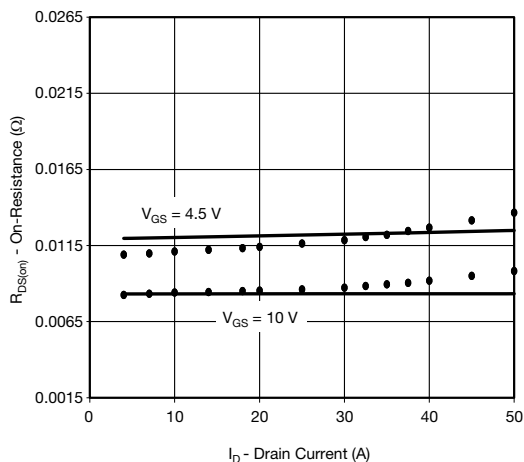
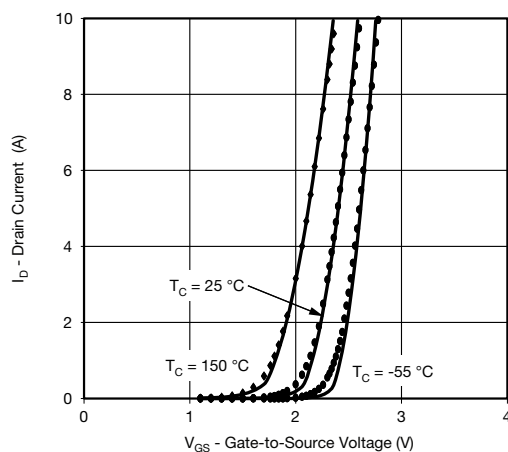
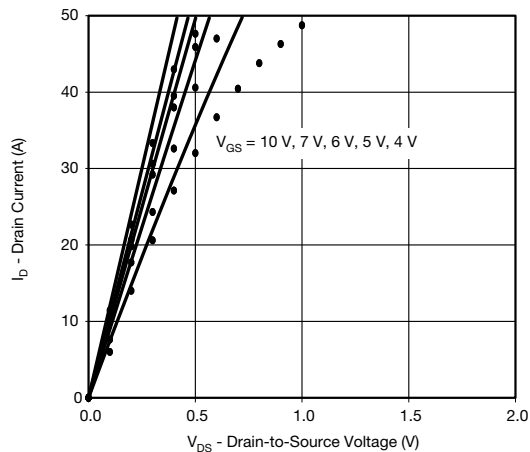
#### Note

- Dots and squares represent measured data



## COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25^\circ\text{C}$ , unless otherwise noted

### N-Channel 2 MOSFET



#### Note

- Dots and squares represent measured data

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