Measurement and Comparison of Thermal Properties of D²PAK and PowerPAK® 8 x 8L Packages

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INTRODUCTION

As a result of the continuing miniaturization of electronic power circuits, heat dissipation has come to play an increasingly important role. The following text relates the thermal properties of various MOSFET packages to circuit board space requirements. This is intended to allow users to better assess the suitability of MOSFETs with regard to applications requiring circuit footprints that are subject to size restrictions. Tests are performed on two MOSFETs joined to create a series connection in order to facilitate the transfer of the results obtained to real-life application scenarios, e.g. inverter output stages.

THEORETICAL OVERVIEW

The conventional approach to thermal characterization of FETs is to quote the thermal resistance R_{th} between the active semiconductor junction and the case R_{thJC} or the ambient medium to which heat is dissipated R_{thJA}. The thermal resistance expresses the temperature difference ΔT required to dissipate a power output P from the component. These figures define the thermal performance of the component in question but do not provide any definitive indication as to which component is most effective in dissipating heat in respect to the circuit board surface area used. In order to perform a quantitative assessment of this aspect, the heat transfer coefficient h_{JA} is considered with the unit W/(m²K). This expresses the heat transfer at a given temperature differential in relation to the footprint of the component under review. The higher the value, the greater the heat transfer given the same temperature differential and footprint. This renders this parameter a basis for decision making, in particular in selecting components for electronic circuits with limited available space and predefined heatsinks.

EXPERIMENTAL SETUP

Exemplary values for R_{thJA} and h_{JA} will be specified, and the results for the D²PAK (SQM60030) and PowerPAK® 8 x 8L (SQJQ480E) will be compared. For this purpose, two n-channel MOSFETs were joined to create a series connection in the manner illustrated in Fig. 1. The two copper surfaces on either side, as shown in Fig. 3 with a surface of approx. 3180 mm², were coated in solder resist and attached to FR4. This equates to a cooling surface area of approx. 1590 mm², or approx. 2.46 in² per MOSFET. However, as the circuit boards were tested lying against a smooth surface with poor heat-conducting properties, the active cooling surface areas must be presumed to be 795 mm², or 1.23 in² per MOSFET. The solder surfaces of the circuit boards are designed in such a way as to allow both packages to be tested on identical circuit boards. This guarantees a precise comparison of cooling surfaces. During the tests, the circuit boards were laid on a level surface. As there is no active ventilation, it must be presumed that all heat is dissipated through natural convection.

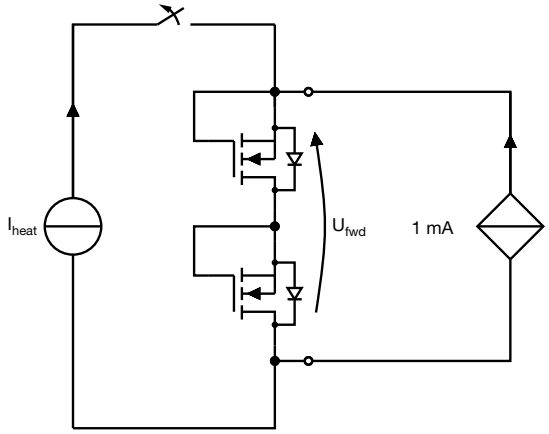

Fig. 1 - Basic Circuit to Measure Junction Temperature of a Series Connection.

The determination of the junction temperature utilizes the fact that the forward voltage of the body diode has a characteristic temperature correlation. With the aid of a current constant I_{meas}, it is possible to derive a value that corresponds to the junction temperature. In order to determine the appropriate conversion factors, the forward voltage of the body diodes U_{fwd} (T_J) is recorded at predefined steady-state temperatures $T_A = T_J$. During the determination of the temperature correlation of the diode voltage and during measurements, the ambient temperature T_A is recorded using a type K thermocouple. This results in the values listed in Table 1. The thermal power loss is achieved by applying a constant current I_{heat} to the series

APPLICATION NOTE

Measurement and Comparison of Thermal Properties of D²PAK and PowerPAK® 8 x 8L Packages

connection in the direction of the flow of the body diodes. The heat dissipated in the series connection P_{diss} is calculated using the parameters of the system at equilibrium, i.e. $P_{diss} = U_{fwd} \times I_{heat}$. If the heating current is suddenly switched off and the voltage drop U_{fwd} at the body diodes caused by measuring current I_{meas} = 1 mA is instantaneously recorded, a value is obtained that can be converted into a junction temperature T_J through linear extrapolation of data from Table 1. The same values apply to both MOSFET cases.

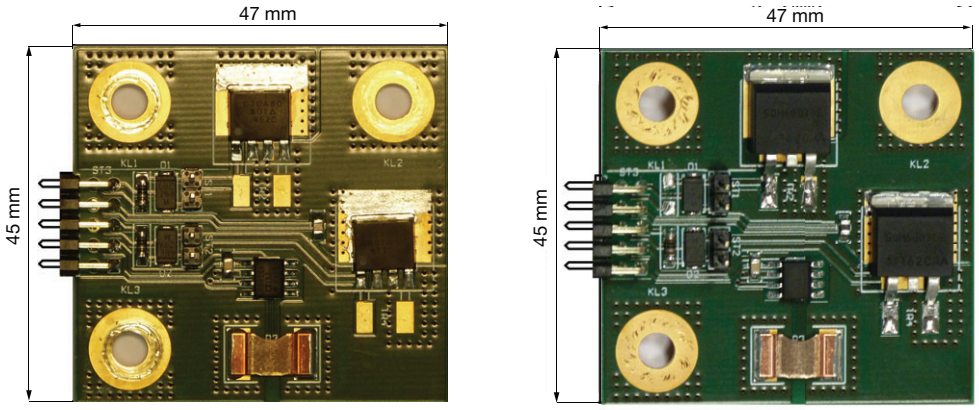

Fig. 2 - Circuit Board Used for Thermal Characterization.
The Circuit Boards Can be Optionally Populated With Either D²PAK or PowerPAK 8 x 8L Packages.

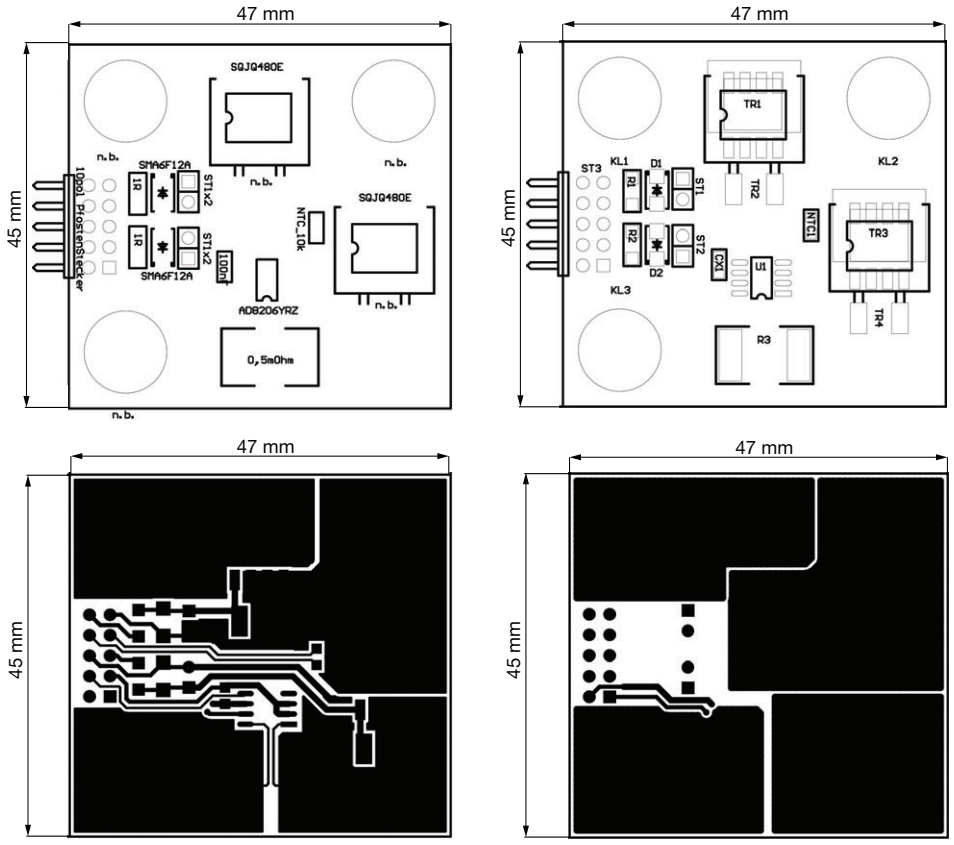

Fig. 3 - Copper Surfaces of Circuit Board.
The Cooling Surface Area Available for Each MOSFET is approx. 1590 mm², or approx. 2.46 in² per MOSFET.

APPLICATION NOTE

Measurement and Comparison of Thermal Properties of D²PAK and PowerPAK® 8 x 8L Packages

TABLE 1			
	20.2 °C	75 °C	123 °C
D²PAK	0.987 V	0.736 V	0.48 V
PPAK 8 x 8L	0.992 V	0.741 V	0.474 V
T_C of bridge	-	-4.6 mV/K	-4.9 mV/K

Note

- Temperature correlation of forward voltage at a current of 1 mA

MEASUREMENT RESULTS

When measuring the interrelationship between the junction temperature T_J and the thermal dissipation loss P_{diss}, Table 4 and Table 5 provide composite values. In the case of the circuit board under review (cf. Fig. 2 and Fig. 3), a mean value for the thermal resistance R_{th} for a series connection consisting of two n-channel MOSFETs was calculated to be R_{th} = 16.6 K/W for the SQM60030 in the D²PAK package and R_{th} = 20.6 K/W for the SQJQ480E in the PowerPAK 8 x 8L package. The values obtained correlate well with the values quoted in the relevant datasheets. A comparisons of the two is shown in Table 2. In order to enable a comparison of thermal properties, the heat transfer coefficient is calculated as described above. The results are summarized in Table 3.

CONCLUSION

A comparison of the thermal behavior of the D²PAK and PowerPAK 8 x 8L packages reveals that under equal peripheral conditions (junction temperature, ambient temperature, heatsink design), the thermal transition resistance R_{thJA} of the PowerPAK 8 x 8L package is slightly higher than that of the D²PAK package. However on closer scrutiny, it becomes apparent that this is chiefly a result of the size. A comparison with the circuit board surface used clearly highlights the advantages of the PowerPAK 8 x 8L. Compared with the D²PAK, the PowerPAK 8 x 8L enables heat dissipation loss densities higher by an order of 2. Therefore it is ideally suited to miniaturized circuits.

TABLE 2				
	DATASHEET		MEASUREMENT	
	R_{th} LIMIT	A	R_{th}	A
D²PAK	40 K/W	1 in²	33 K/W	1.23 in²
PPAK 8 x 8L	50 K/W	1 in²	41 K/W	1.23 in²

Note

- Datasheet entries and recorded values per single FET. Please notice the difference in the active cooling surface area A

TABLE 3			
	R_{thJA}	A	h_{JA}
D²PAK	16.6 K/W	344 mm²	0.18 mW/(K mm²)
PPAK 8 x 8L	20.6 K/W	130 mm²	0.38 mW/(K mm²)

Note

- Comparison of heat transfer coefficient h_{JA} using the components footprint area A [2]

TABLE 4					
I_{heat} (A)	P_{diss} (W)	T_A (°C)	U_{fwd} (V)	T_J (°C)	R_{th} (K/W)
1	1.26	21	0.98	43.5	17.8
2	2.48	21	0.78	65.2	17.8
3	3.63	20.7	0.70	95.1	16
4	4.68	20.5	0.62	78.8	15.9
5	5.70	20.7	0.54	111.4	15.9
6	6.66	20.5	0.46	127.8	16.1

Note

- Measurements on series connection consisting of two SQM60030

TABLE 5					
I_{heat} (A)	P_{diss} (W)	T_A (°C)	U_{fwd} (V)	T_J (°C)	R_{th} (K/W)
1	1.24	20.2	0.85	51.1	24.9
2	2.42	20	0.76	70.6	20.9
3	3.51	18	0.64	92	20.9
4	4.52	20.5	0.57	106.3	19
5	5.45	20.5	0.48	124.7	19.1
6	6.36	20.5	0.41	139	18.6

Note

- Measurements on series connection consisting of two SQJQ480E

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REFERENCES

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