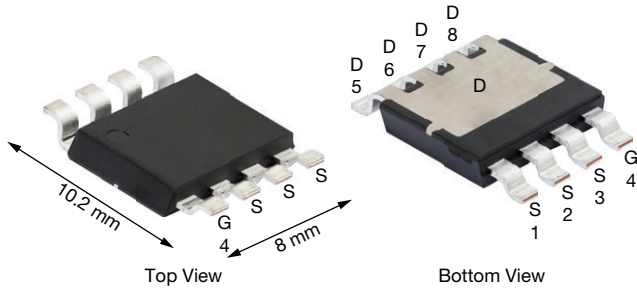
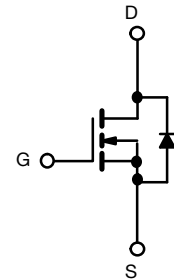


# Automotive N-Channel 40 V (D-S) 175 °C MOSFET

**PowerPAK® 8 x 8LR**

**FEATURES**

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 %  $R_g$  and UIS tested
- Thin 1.6 mm package
- Very low thermal resistance
- Material categorization:  
for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

 AUTOMOTIVE  
GRADE

**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**


N-Channel MOSFET

**PRODUCT SUMMARY**

$V_{DS}$ (V)	40
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.0009
$I_D$ (A)	575
Configuration	Single

**ORDERING INFORMATION**

Package	PowerPAK 8 x 8LR
Lead (Pb)-free and halogen-free	SQJQ144AER (for detailed order number please see <a href="http://www.vishay.com/doc?79776">www.vishay.com/doc?79776</a> )

**ABSOLUTE MAXIMUM RATINGS** ( $T_C = 25$  °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	40	V
Gate-source voltage	$V_{GS}$	$\pm 20$	
Continuous drain current	$I_D$	$T_C = 25$ °C	575
		$T_C = 125$ °C	330
Continuous source current (diode conduction)	$I_S$	545	A
Pulsed drain current <sup>a</sup>	$I_{DM}$	1800	
Single pulse avalanche current	$I_{AS}$	60	mJ
Single pulse avalanche energy			
Maximum power dissipation	$P_D$	$T_C = 25$ °C	600
		$T_C = 125$ °C	200
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>c</sup>		260	

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	$R_{thJA}$	44	°C/W
Junction-to-case (drain)			

**Notes**

- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %
- When mounted on 1" square PCB (FR4 material)
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



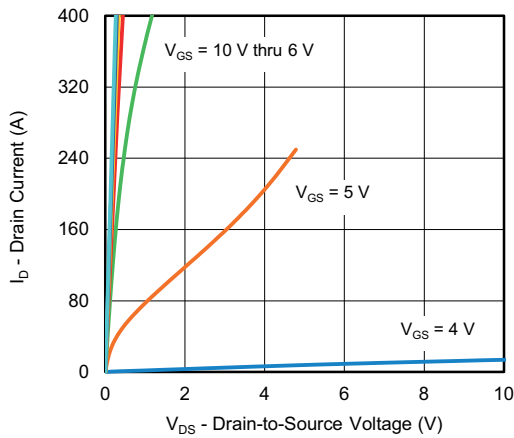
<b>SPECIFICATIONS</b> ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$		40	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2	3	3.5	
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	150	
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	100	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}$	-	0.0007	0.0009	$\Omega$
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.0015	
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.0019	
Forward transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 60\text{ A}$		-	160	-	S
<b>Dynamic <sup>b</sup></b>							
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	-	7220	9020	$\text{pF}$
Output capacitance	$C_{oss}$			-	2290	2860	
Reverse transfer capacitance	$C_{rss}$			-	175	220	
Total gate charge <sup>c</sup>	$Q_g$	$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 30\text{ A}$	-	116	145	$\text{nC}$
Gate-source charge <sup>c</sup>	$Q_{gs}$			-	36	-	
Gate-drain charge <sup>c</sup>	$Q_{gd}$			-	25	-	
Gate resistance	$R_g$	$f = 1\text{ MHz}$		0.9	1.6	2.6	$\Omega$
Turn-on delay time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 0.66\text{ }\Omega$ $I_D \cong 30\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		-	17	27	$\text{ns}$
Rise time <sup>c</sup>	$t_r$			-	27	41	
Turn-off delay time <sup>c</sup>	$t_{d(off)}$			-	41	62	
Fall time <sup>c</sup>	$t_f$			-	18	27	
<b>Source-Drain Diode Ratings and Characteristics <sup>b</sup></b>							
Reverse recovery time	$t_{rr}$	$V_{DD} = 32\text{ V}, I_{FM} = 15\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}$		-	66	-	ns
Reverse recovery charge	$Q_{rr}$			-	94	-	nC
Reverse recovery current	$I_{RM}$			-	-	-3.6	A
Pulsed current <sup>a</sup>	$I_{SM}$			-	-	1600	A
Forward voltage	$V_{SD}$	$I_F = 50\text{ A}, V_{GS} = 0$		-	0.8	1.1	V

**Notes**

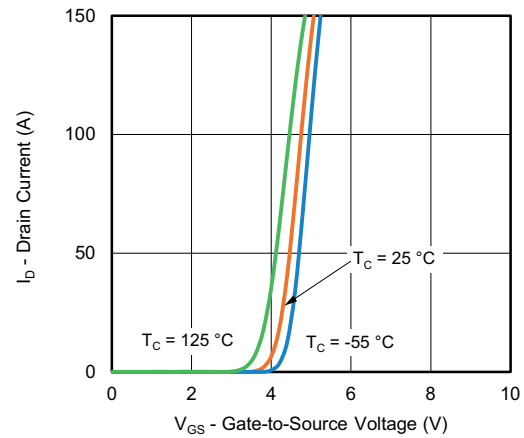
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\text{ }\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

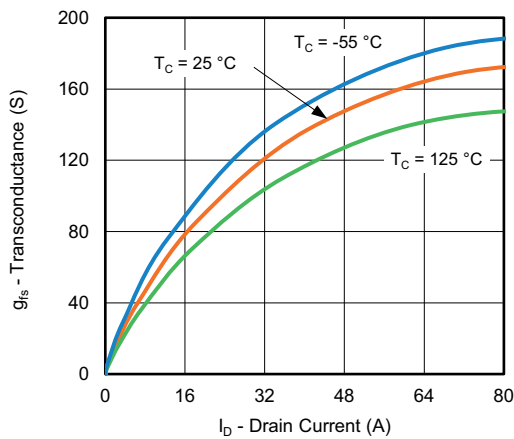
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



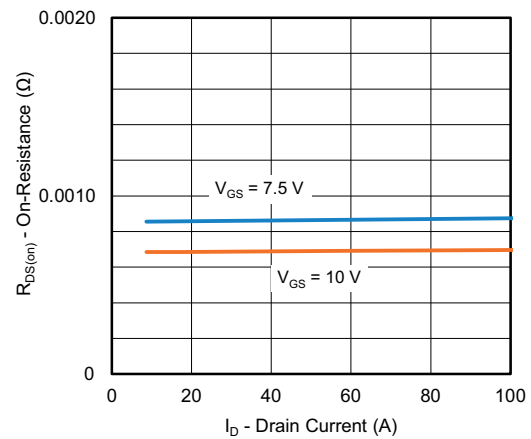
**Output Characteristics**



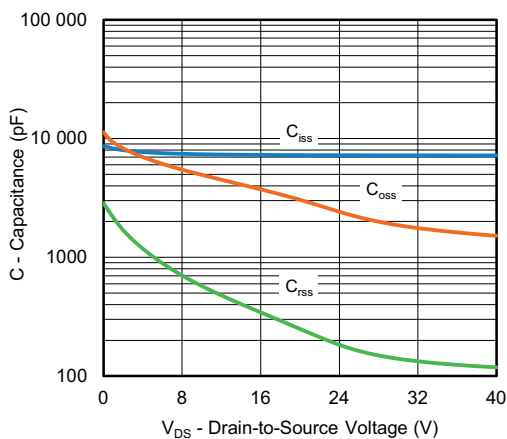
**Transfer Characteristics**



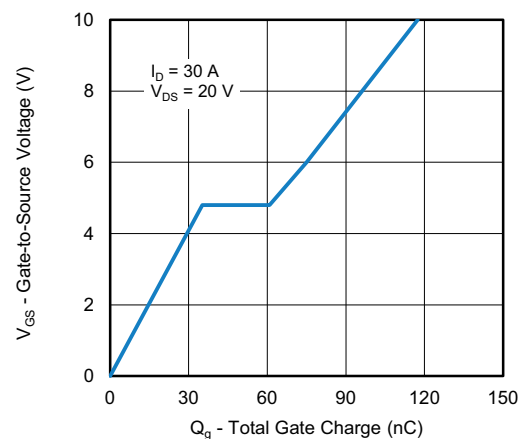
**Transconductance**



**On-Resistance vs. Drain Current**



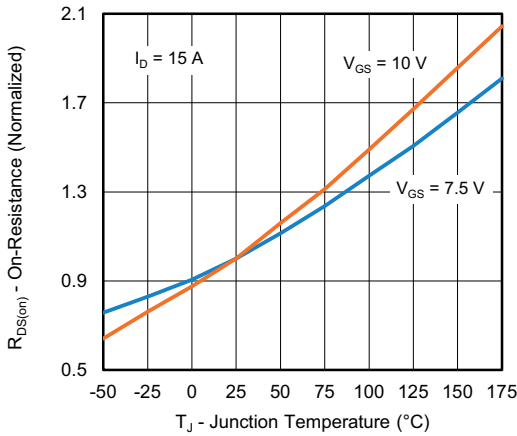
**Capacitance**



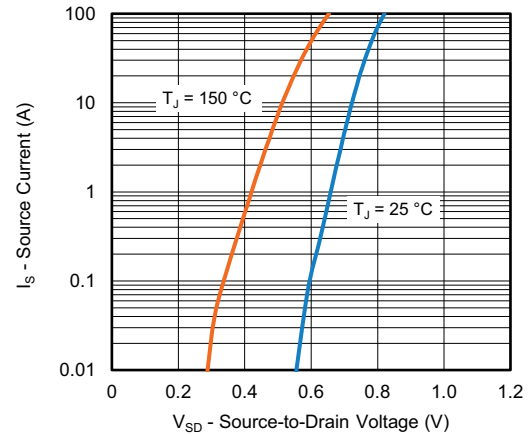
**Gate Charge**



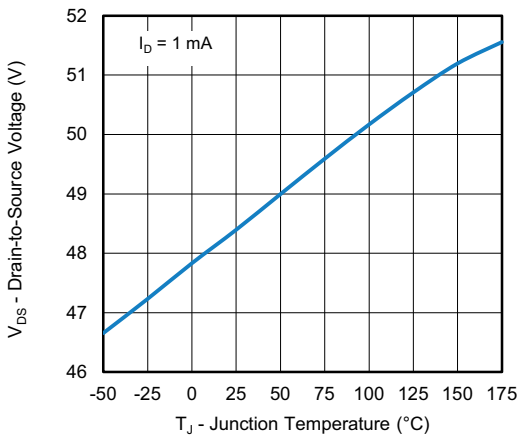
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



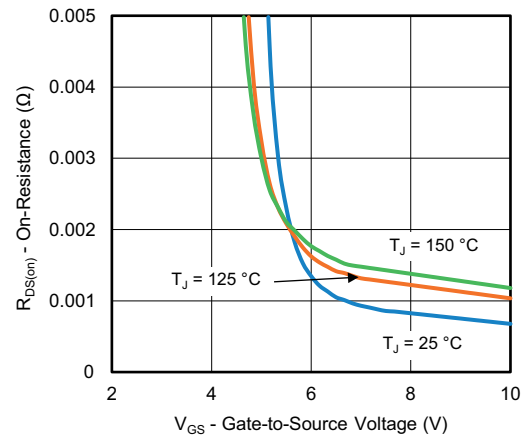
**On-Resistance vs. Junction Temperature**



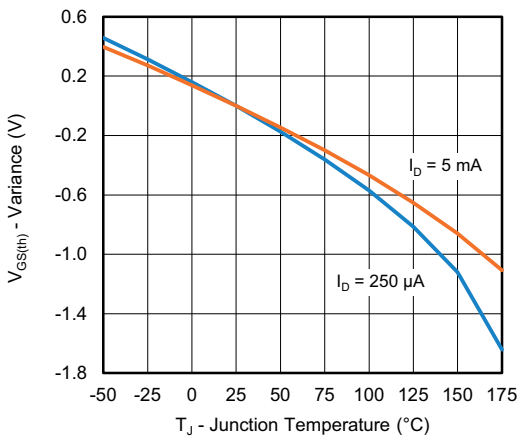
**Source Drain Diode Forward Voltage**



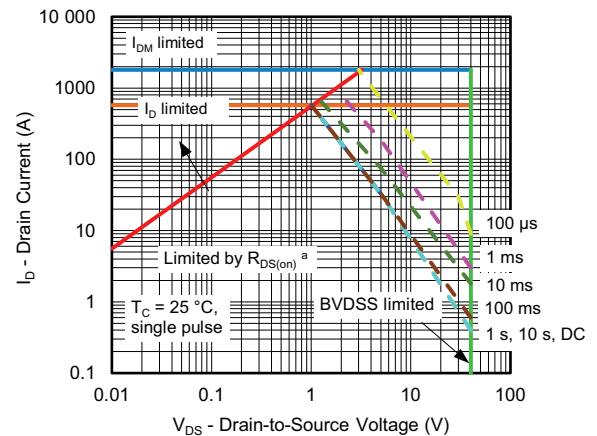
**Drain Source Breakdown vs. Junction Temperature**



**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



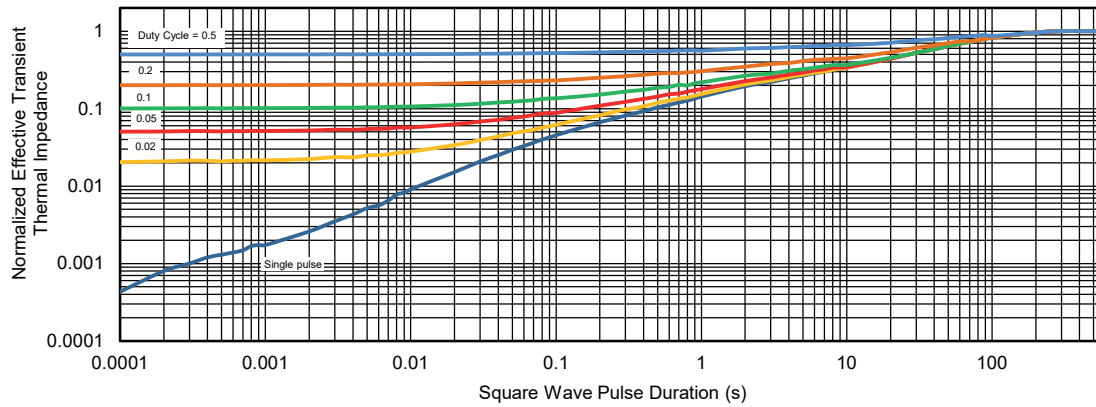
**Safe Operating Area**

**Note**

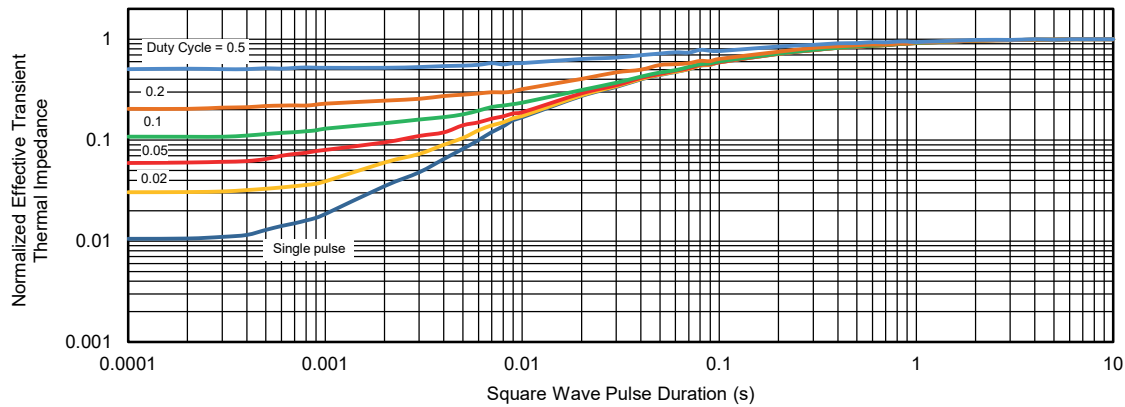
- a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



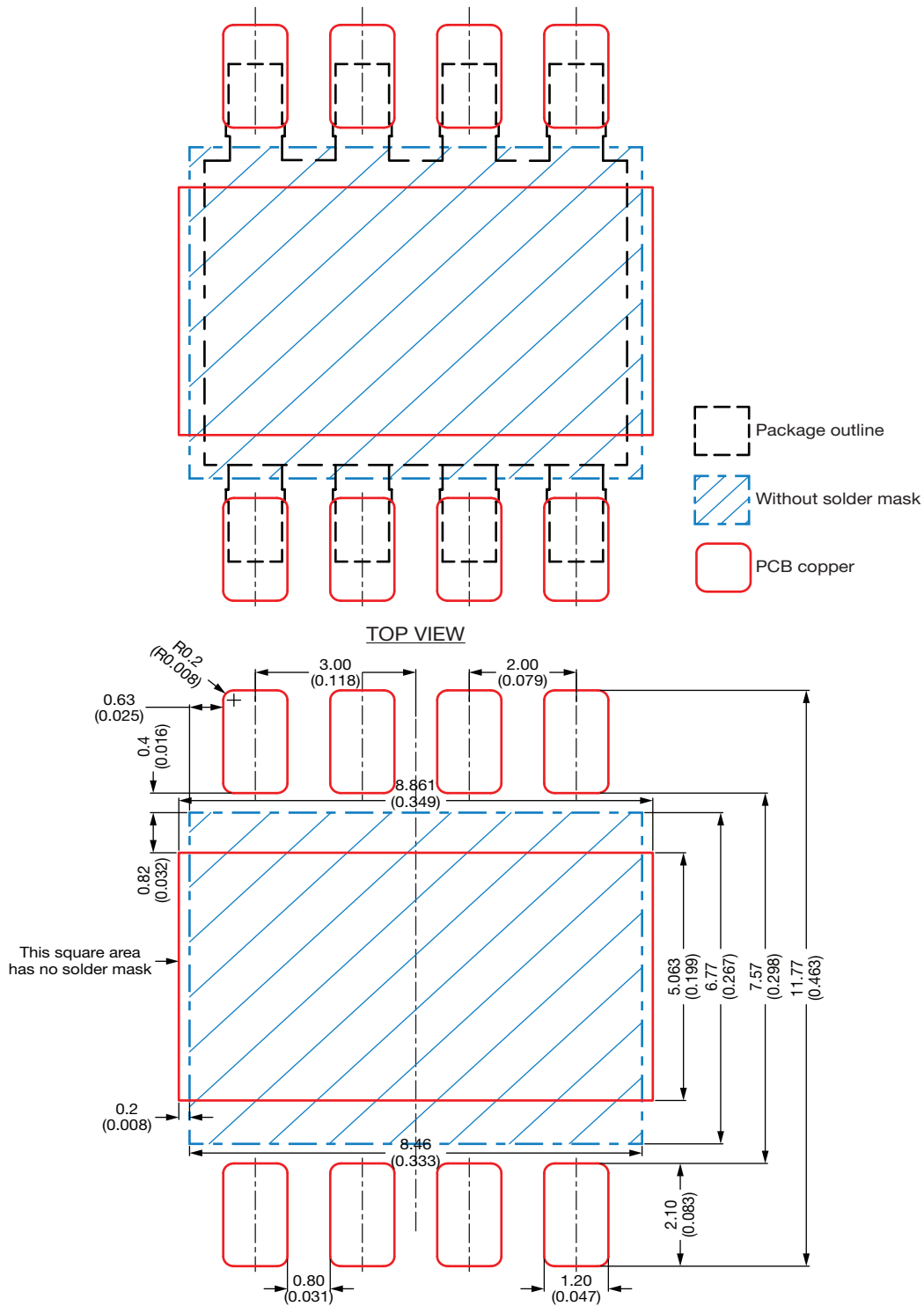
**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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**Recommended Land Pattern PowerPAK® 8 x 8LR**



**Notes**

- This land pattern is for reference
- Proposed stencil thickness 200 µm
- All dimensions are in millimeter (inches)

ECN: C23-0461-Rev. B, 17-Apr-2023  
 DWG: 3002



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