

N-Channel 25 V (D-S) MOSFET

DESCRIPTION

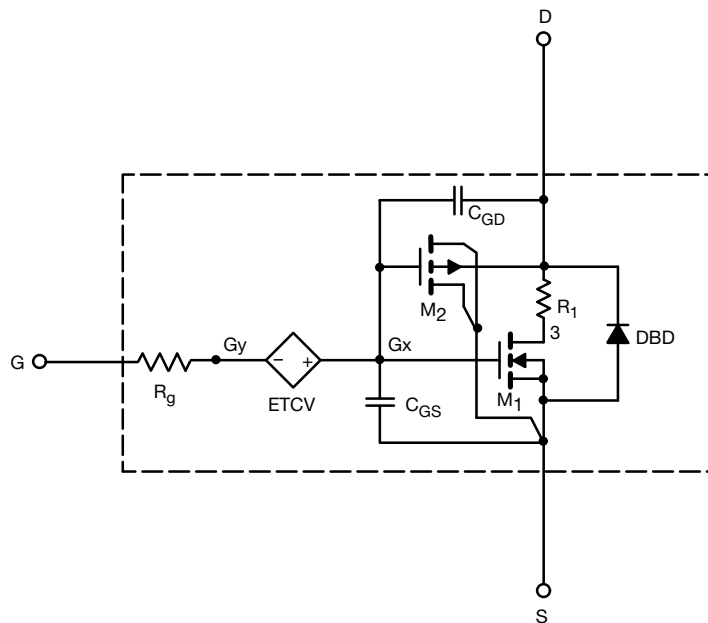
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over -55 °C to +125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



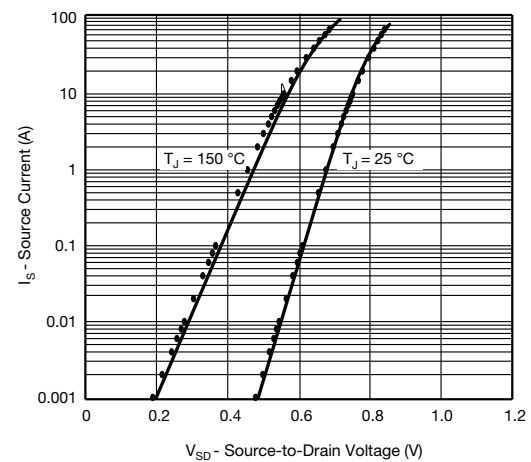
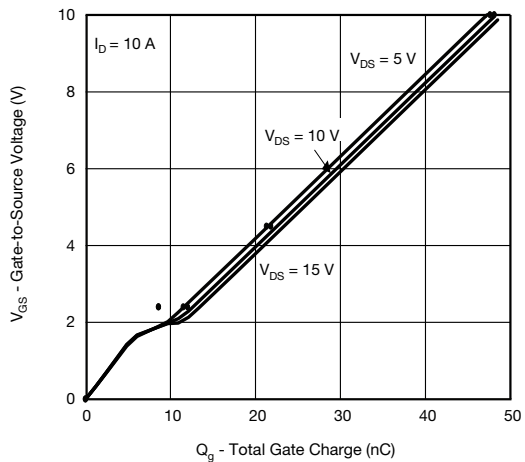
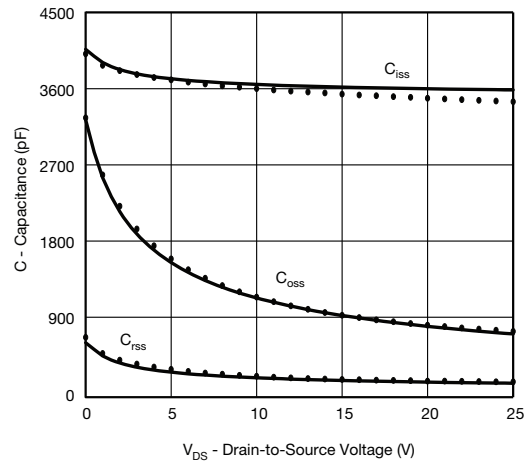
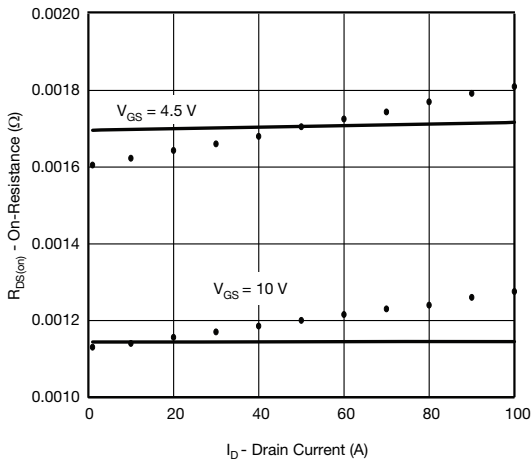
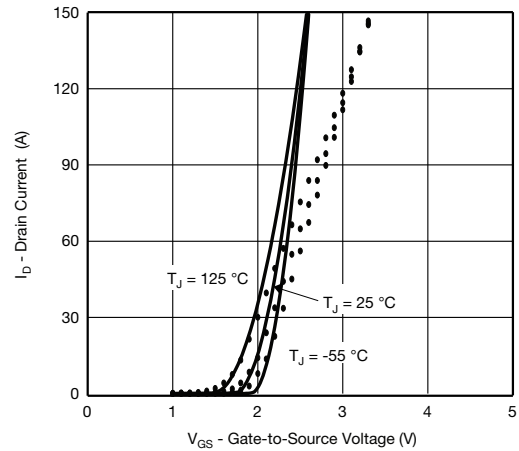
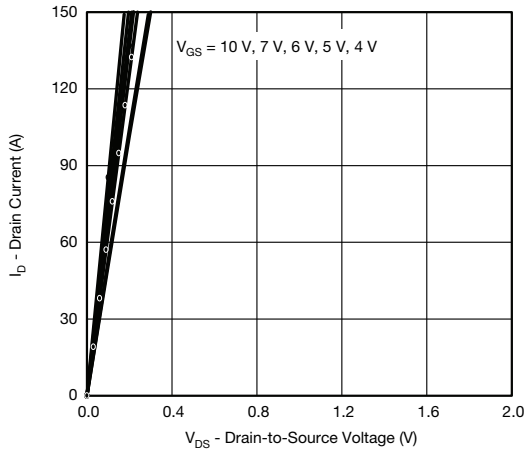
| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | |
|---|---------------------|--|----------------|---------------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS | SIMULATED DATA | MEASURED DATA | UNIT |
| Static | | | | | |
| Gate-Source Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | 1.4 | - | V |
| Drain-Source On-State Resistance ^a | R _{DS(on)} | V _{GS} = 10 V, I _D = 15 A | 0.00114 | 0.00115 | Ω |
| | | V _{GS} = 4.5 V, I _D = 10 A | 0.00169 | 0.00160 | |
| Forward Transconductance ^a | g _{fs} | V _{DS} = 10 V, I _D = 15 A | 118 | 95 | S |
| Diode Forward Voltage | V _{SD} | I _S = 5 A | 0.73 | 0.73 | V |
| Dynamic ^b | | | | | |
| Input Capacitance | C _{iss} | V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz | 3650 | 3640 | pF |
| Output Capacitance | C _{oss} | | 1130 | 1155 | |
| Reverse Transfer Capacitance | C _{rss} | | 186 | 200 | |
| Total Gate Charge | Q _g | V _{DS} = 10 V, V _{GS} = 10 V, I _D = 10 A | 48.4 | 48.1 | nC |
| | | V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 10 A | 22 | 21.8 | |
| Gate-Source Charge | Q _{gs} | | 8.6 | 8.6 | |
| Gate-Drain Charge | Q _{gd} | | 3.4 | 3.4 | |

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data.

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