



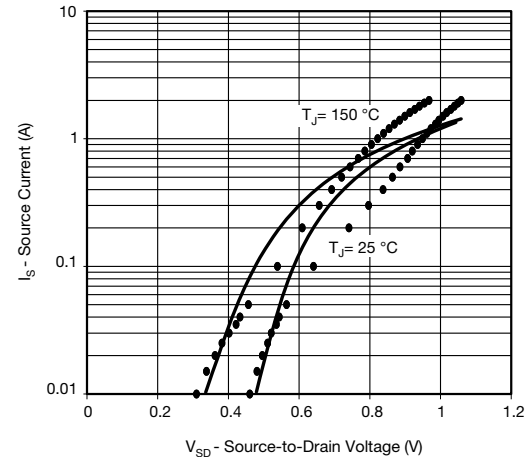
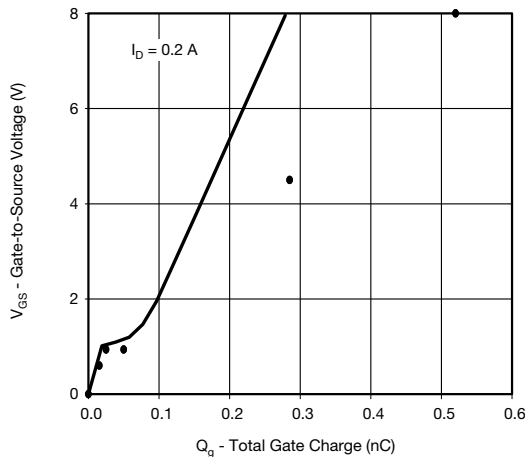
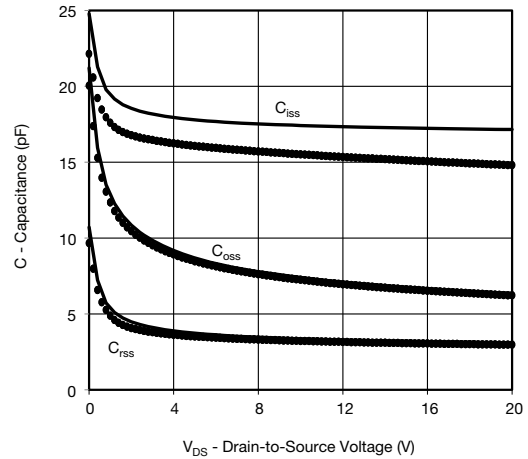
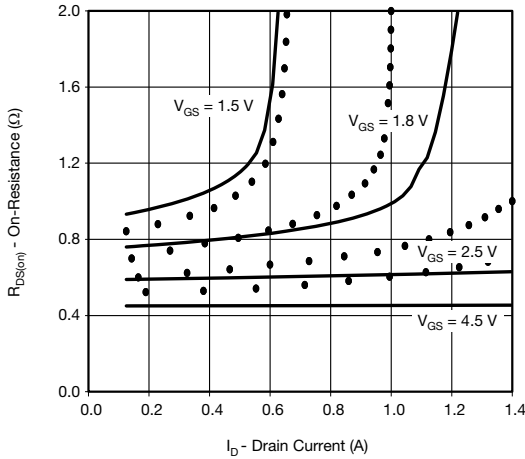
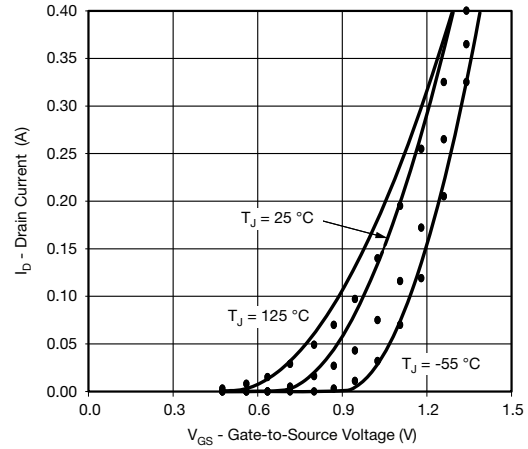
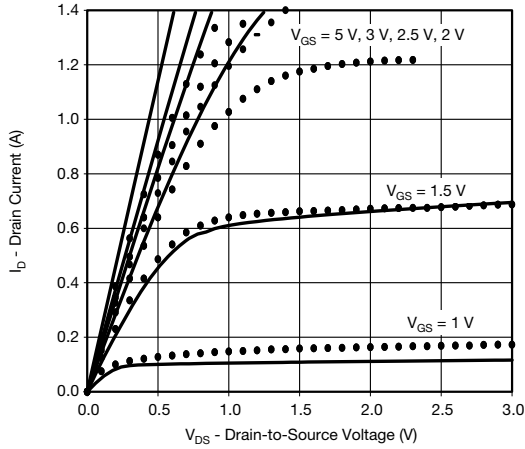
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.62	-	V
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 0.2\ \text{A}$	0.50	0.57	Ω
		$V_{GS} = 2.5\ \text{V}, I_D = 0.1\ \text{A}$	0.59	0.67	
		$V_{GS} = 1.8\ \text{V}, I_D = 0.02\ \text{A}$	0.80	0.80	
		$V_{GS} = 1.5\ \text{V}, I_D = 0.01\ \text{A}$	0.90	0.90	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\ \text{V}, I_D = 0.2\ \text{A}$	1	1.2	S
Diode Forward Voltage	V_{SD}	$I_S = 0.2\ \text{A}$	0.7	0.8	V
Dynamic ^b					
Input Capacitance	C_{iss}	$V_{DS} = 10\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$	17	16	pF
Output Capacitance	C_{oss}		7.4	7.5	
Reverse Transfer Capacitance	C_{rss}		3.4	3.5	
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}, V_{GS} = 8\ \text{V}, I_D = 0.2\ \text{A}$	0.29	0.52	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = 10\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 0.2\ \text{A}$	0.17	0.29	
Gate-Drain Charge	Q_{gd}		0.03	0.03	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\ \%$.
b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data.

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