Automotive Dual N-Channel 100 V (D-S) 175 °C MOSFET

DESCRIPTION

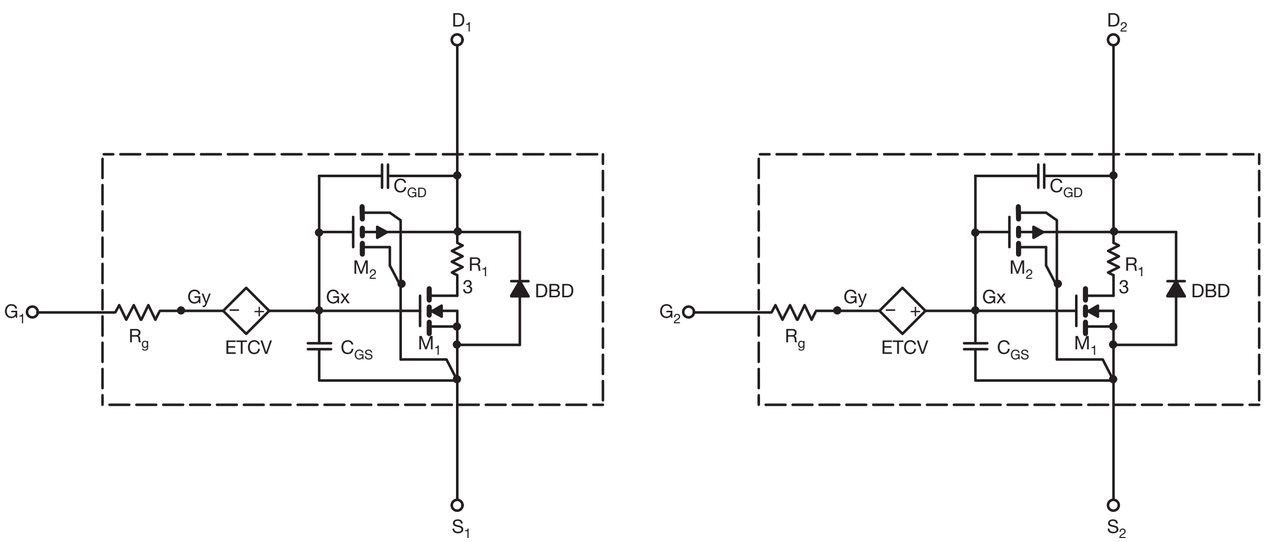
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over -55 °C to +125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits

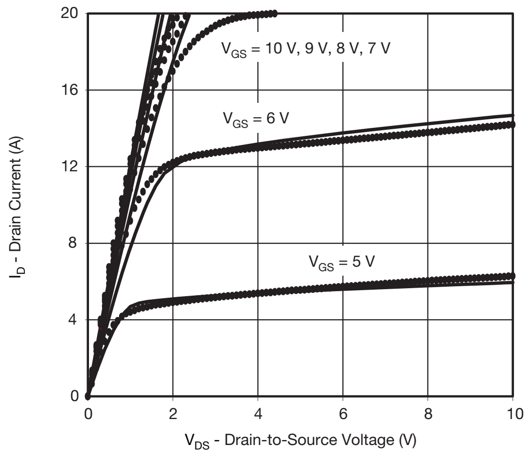
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	2	2	V
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 4 A	0.0766	0.0765	Ω
		V_{GS} = 4.5 V, I_D = 3 A	0.1070	0.0967	
Forward transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 4 A	7.6	8.6	S
Diode forward voltage	V_{SD}	I_F = 4 A	0.87	0.88	V
Dynamic [b]					
Input capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	223	212	pF
Output capacitance	C_{oss}		119	118	
Reverse transfer capacitance	C_{rss}		16	15	
Total gate charge	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 3 A	4.5	4.7	nC
Gate-source charge	Q_{gs}		0.8	0.8	
Gate-drain charge	Q_{gd}		1.3	1.3	

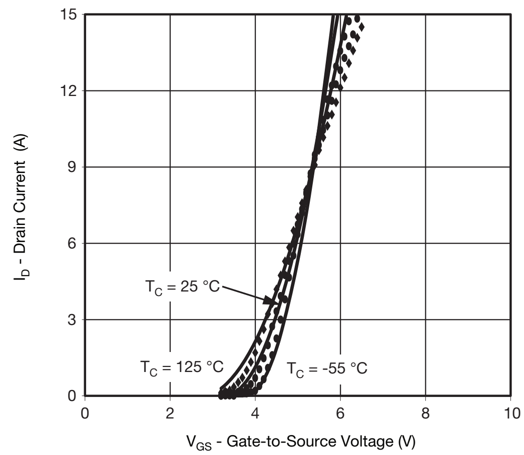
Notes

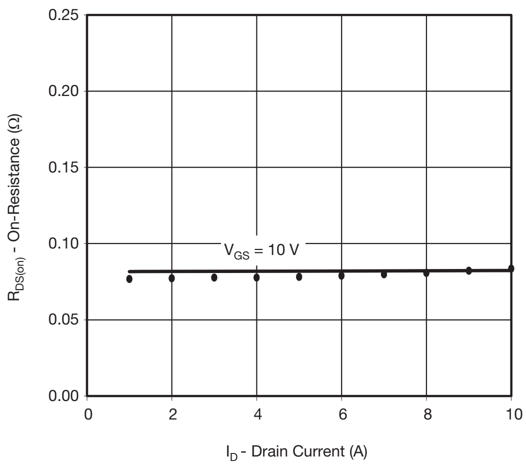
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

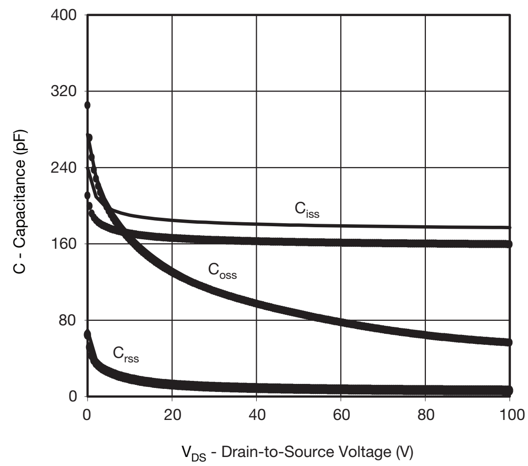
b. Guaranteed by design, not subject to production testing

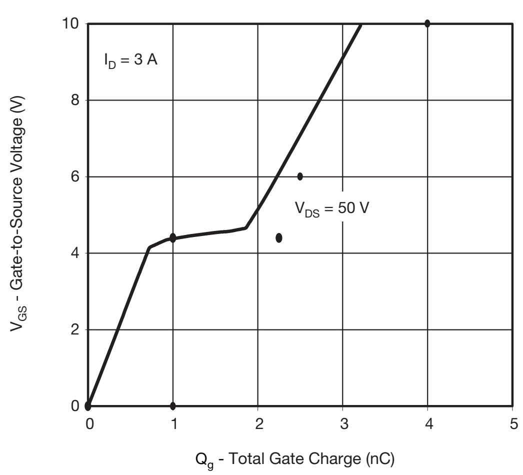
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

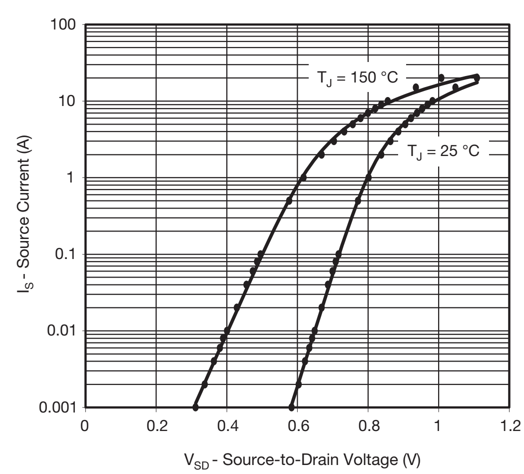












Note

- Dots and squares represent measured data

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