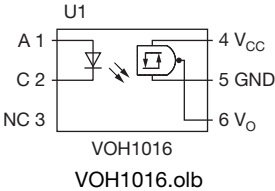# Optocoupler VOH1016,
High Speed Optocoupler, 1 MBd, Schmitt Trigger

DESCRIPTION

This device VOH1016A is an industry standard optocoupler with a high efficient LED as input and an integrated photo detector as output. The detector incorporates a Schmitt trigger stage to improve noise immunity.

The PSpice models have been written from device characterization data and were tested with simulation program OrCAD16.6.

The symbol and model files as well as the netlist are in the symbol library file VOH1016.olb, model library file VOH1016.lib, and netlist file VOH1016.txt respectively for this model.

This document is intended as a guideline of simulating with provided model and does not constitute as commercial product, neither a substitute to datasheet.

PART	MODEL DESCRIPTION	SYMBOL FILE	MODEL FILE
VOH1016	High Speed Optocoupler	 VOH1016.olb	VOH1016.lib

RECOMMENDED USE OF THE MODEL

• This model is designed only for use at 25 °C and should be used as is.

• This model has been created and tested with OrCAD version 16.6.

• The olb file (symbol) is not down-compatible. Users of the earlier versions need to create the symbols on their platform and associate with relative PSpice model data.

NETLIST OF MODEL

Following list shows the netlist of the model:

```
* Library of High Speed Optocoupler VOH1016
* Copyright VISHAY, Inc. 2018 All Rights Reserved.
**
**
.SUBCKT VOH1016 A C NC VCC GND VO
dD1  A 6  DEMIT
vV1  6  C  DC 0
wW1  VCC 7  vV1  I_SW1
rR3  GND 7  10K
xU2  7 VO $G_DPWR $G_DGND BUF
```

```
R4        0 NC 1MEG
C1        0 NC 1u
.MODEL DEMIT   D
+ IS=1.8e-021 N=1.02e+000 RS=-8.406e-002
+ BV=3.000e+000 IBV=0.5e-006  XTI=4
+ EG=1.52436 CJO=18E-12 VJ=0.75 M=0.5 FC=0.5
.MODEL I_SW1 ISWITCH (Roff=1e6 Ron=1 IT=0.68m IH=0.12m TD=70ns)
.ENDS VOH1016
*$
*************************************************************
***----------------------------------------------------------------------
**  1 INPUT BUFFER
**
.SUBCKT BUF  I0  O  optional: DPWR=$G_DPWR DGND=$G_DGND
U1 BUF DPWR  DGND I0  O
+  D_PLD_GATE IO_PLD
.ENDS
*$
***----------------------------------------------------------------------
.MODEL D_PLD_GATE  UGATE
*$
.MODEL D_PLD_TGATE  UTGATE
*$
.MODEL D_PLD_EFF  UEFF
*$
.MODEL D_PLD_GFF  UGFF
*$
.MODEL IO_PLD  UIO
*$
**=================================================================*
* Note:                                   *
* Altough models can be a useful tool in evaluating device       *
* performance, they cannot model exact device performance        *
* under all conditions, nor are they intended to replace         *
* breadboarding for final verification!                          *
*                                 *
* Models provided by VISHAY Semiconductors GmbH are not          *
* as fully representing all of the specifications and operating  *
* characteristics of the semiconductor product to which the      *
* model relates.                                  *
* The models describe the characteristics of typical devices.    *
* In all cases, the current data sheet information for a given    *
* device is the final design guideline and the only actual       *
* performance specification.                          *
* VISHAY Semiconductors does not assume any liability arising     *
* from the model use. VISHAY Semiconductors reserves the right to  *
* change models without prior notice.                         *
**=================================================================*
```

SIMULATED PARAMETERS (T_{amb} = 25 °C, unless otherwise specified)				
PARAMETER	TEST CONDITION	SYMBOL	SIMULATION DATA	UNIT
INPUT				
Forward voltage	I_F = 4 mA	V_F	1.11	V
OUTPUT				
Turn-on threshold current	V_{CC} = 5 V, R_L = 280 Ω	I_{FT}	0.75	mA
SWITCHING CHARACTERISTICS				
Propagation delay time to high output level	R_L= 280 Ω, V_{CC} = 5 V, I_F = 4 mA	t_{PLH}	0.75	μs
Propagation delay time to low output level		t_{PHL}	0.75	

EXAMPLE SIMULATION PLOTS USING OrCAD
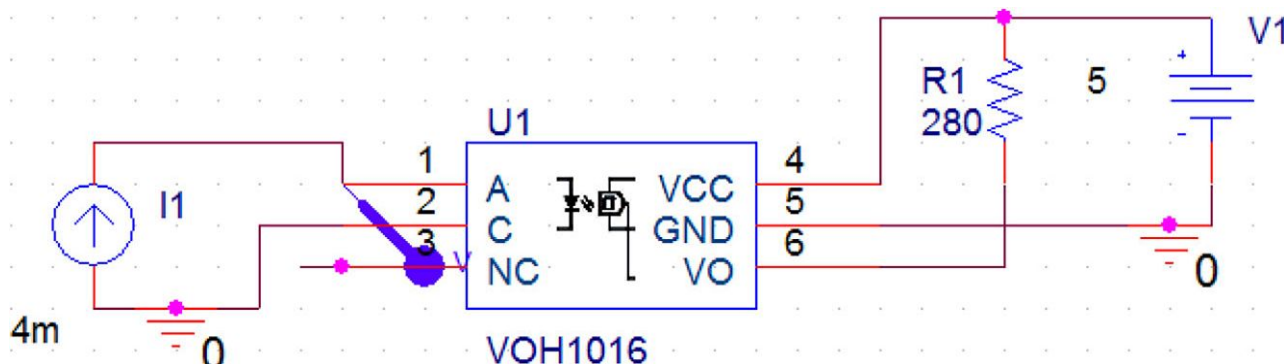
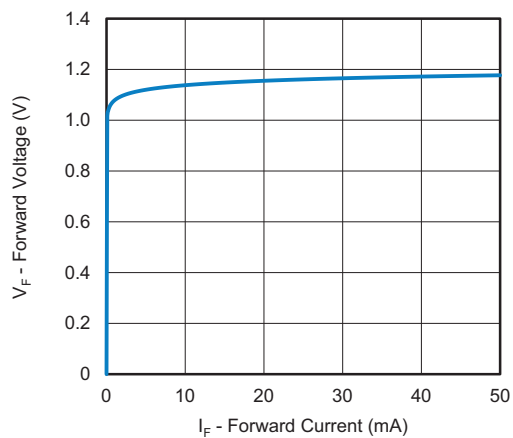Fig. 1 - Simulation Setup for V_F vs. I_F Curve
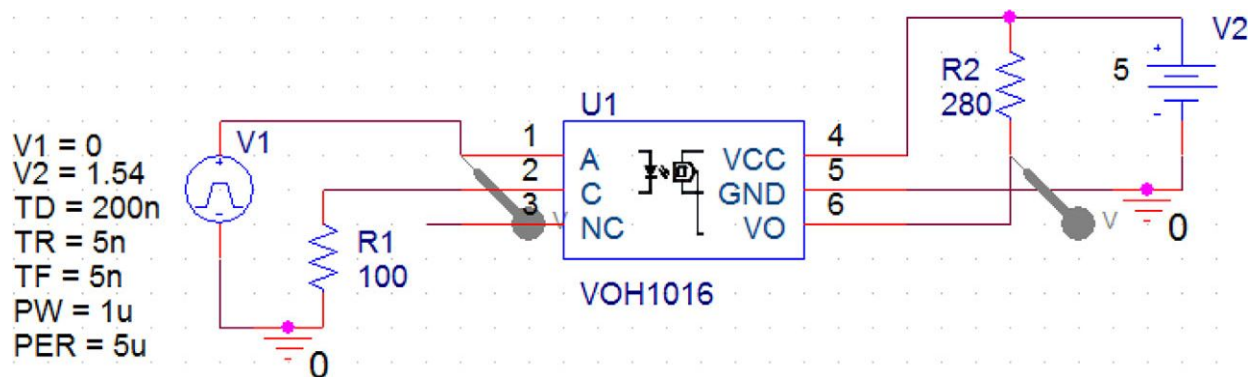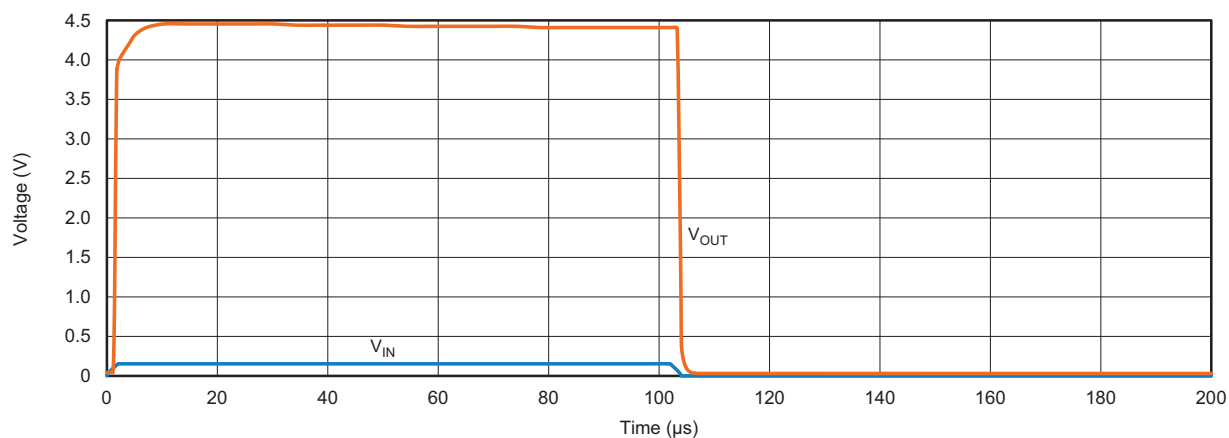

Fig. 2 - Forward Current vs. Forward Voltage

Fig. 3 - Timing Simulation Setup

Fig. 4 - Timing Simulation Output