Circuit Description of the IR Receiver Modules

All Vishay IR receivers have the same circuit architecture. The functional block diagram of the Vishay TSOP IR receiver modules can be seen in Fig. 1. The infrared signal generates an equivalent photo current in the photo PIN diode. The DC part of the signal is blocked in the bias circuit and the AC part is passed to a trans impedance amplifier followed by an automatic gain-control amplifier and an integrated band pass filter. A comparator, an integrator and a Schmitt Trigger stage perform the final signal conditioning. The blocks “Automatic Gain Control” and “Automatic Threshold Control” dynamically control the operating points as well as the threshold levels required to suppress noise from disturbance sources. The digital output signal has an active low polarity and consists of an envelope signal of the incoming optical burst, without the carrier frequency.

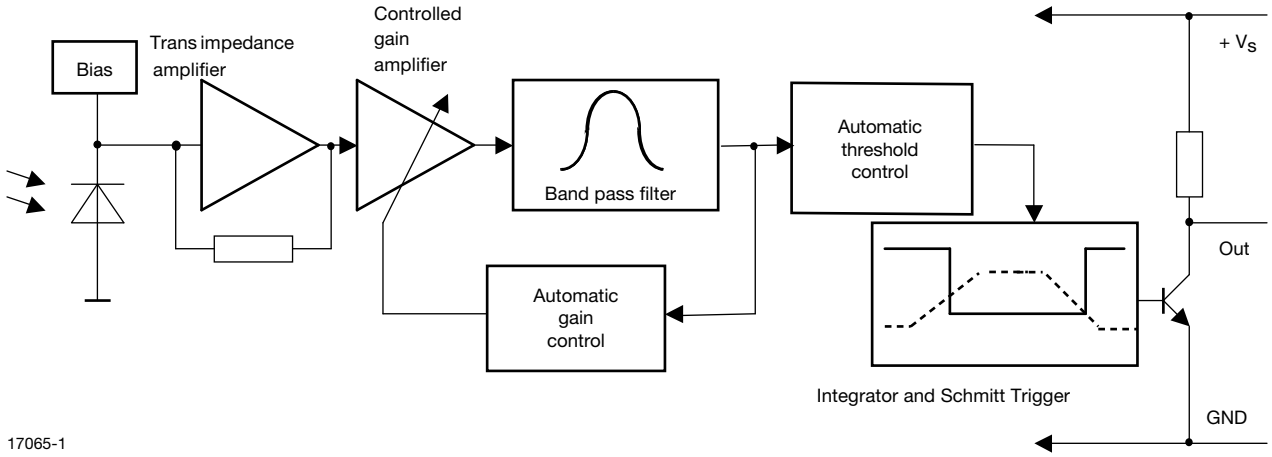

Fig. 1 - Simplified Block Diagram of TSOP IR Receivers

TRANS IMPEDANCE AMPLIFIER

The Bias block provides the necessary bias voltage for the detector diode and also separates the DC and low frequency components from the useful signal by providing a low impedance path to ground. The AC signals are passed unhindered to the trans impedance amplifier.

The currents at the signal frequency are converted by the trans impedance amplifier to a voltage at the input of the Controlled Gain Amplifier.

CONTROLLED GAIN AMPLIFIER

Most of the gain in the system is generated in the controlled gain amplifier, whereby the degree of amplification is controlled by the automatic gain control (AGC) block.

BAND PASS FILTER

The band pass filter is an important system block, required to obtain good performance in disturbed or noisy ambients. The filter attenuates noise coming from various disturbance sources.

The following band pass center frequencies are available: 30 kHz, 33 kHz, 36 kHz, 38 kHz, 40 kHz, and 56 kHz. These are the carrier frequencies for the most common data formats of IR remote controls.

The duty cycle of the carrier frequency can be between 50 % and 5 %. A remote control system using a Vishay IR receiver is more efficient regarding battery power consumption on the emitter side if the carrier duty cycle is low. This is shown in the following example:

- Carrier duty cycle 50 %, peak current of emitter I_F = 50 mA, the resulting transmission distance is 30 m
- Carrier duty cycle 10 %, peak current of emitter I_F = 200 mA, the resulting transmission distance is 32 m

AUTOMATIC GAIN CONTROL (AGC)

The AGC stage ensures that the receiver module is insensitive to disturbance signals. It adapts the system sensitivity to the existing noise or disturbance level by changing the gain of the amplifier. In dark ambient, the AGC also sets the gain to the most sensitive value at which there are no longer any random output pulses. The time constant of the AGC was chosen to be sufficiently large enough to avoid a decrease in sensitivity during normal transmission. The AGC does not react to the useful signal but reduces the sensitivity in case of disturbances. Hence the AGC has to distinguish between useful and disturbance signals. To achieve this, the AGC needs to distinguish between these good and bad signals. The characteristics used to destinguish the signals are different for the various IR receiver series from Vishay. The criteria used are mainly burst length and envelope duty cycle, except for the AGC 6 of TSOP9... series which uses repetitive gap times in the data stream (signal gap time, SGT).

Table 1 shows the maximum burst length limit for different AGC numbers and IC generations. If the maximum burst length is exceeded, additional idle times can prevent the receiver from suppressing the data signal. The highest burst rate which can be achieved with a specific AGC is given in the last line of Table 1. Please note, that AGC 6 in Cyllene 1 TSOP9... series receiver has no max. burst length limit, since this AGC searches for min. gap times of approx. 12 ms every 50 ms interval. These are usually the gap times between adjacent data words.

TABLE 1 - CONDITIONS OF THE AGC FOR DATA SIGNAL

	AGC 1	AGC 2	AGC 3	AGC 4	AGC 5	AGC 6
CYLLENE 1 (TSOP9...)						
Maximum burst length for high duty cycle	1.8ms	1.8 ms	0.5 ms	1 ms	1ms	SGT
Idle time needed for each burst longer than the max. burst length (above line)	1 x burst length	6 x burst length	6 x burst length	10 x burst length	> 20 ms	-
Maximum number of short bursts in 1 s	3000	1000	2500	1800	2500	-
CYLLENE 2A (TSOP1...)						
Maximum burst length for high duty cycle	1.8ms	1.9 ms	0.9 ms	1 ms	0.5 ms	1 ms
Idle time needed for each burst longer than the max. burst length (above line)	1 x burst length	6 x burst length	10 x burst length	10 x burst length	10 x burst length	10 x burst length
Maximum number of short bursts in 1 s	2100	750	2100	1300	2100	750
CYLLENE 2B (TSOP5...)						
Maximum burst length for high duty cycle	1.8ms	1.9 ms	1 ms	1 ms	0.5 ms	-
Idle time needed for each burst longer than the max. burst length (above line)	1 x burst length	3 x burst length	6 x burst length	10 x burst length	10 x burst length	-
Maximum number of short bursts in 1 s	2500	950	2500	1500	2500	-
CYLLENE 2C (TSOP3...)						
Maximum burst length for high duty cycle	1.8ms	1.8 ms	0.9 ms	0.9 ms	0.5 ms	-
Idle time needed for each burst longer than the max. burst length (above line)	2 x burst length	5 x burst length	9 x burst length	15 x burst length	25 x burst length	-
Maximum number of short bursts in 1 s	2000	1700	2000	1700	2000	-

AUTOMATIC THRESHOLD CONTROL (ATC)

After the band pass filter, the signal is evaluated by a comparator. In quiescent mode (no data signal present), there should be no output signal due to noise, i.e. the threshold of the comparator is set above the noise floor.

INTEGRATOR AND SCHMITT TRIGGER

The integrator is triggered when the signal reaches the above mentioned comparator threshold. Several consecutive cycles of the carrier signal at the comparator output are required before the integrator finally triggers the output.

The integration time necessary to control the output via the Schmitt Trigger is given in Table 2 for each of the IR receiver module series.

The integrator defines a minimum time for the burst length (integrator ramp up time) and a minimum time between the bursts (integrator ramp down time).

The integrator prevents the feed-through of short disturbances or spikes to the output. A long integrator ramp time can improve the signal to noise ratio significantly. The design of the integrator and Schmitt Trigger combination was optimised such that the output pulse width is close to the optical burst length at the input.

TABLE 2 - INTEGRATOR DATA OF THE VISHAY IR RECEIVER

	AGC 1	AGC 2	AGC 3	AGC 4	AGC 5	AGC 6
CYLLENE 1 (TSOP9...)						
Minimum burst length	6	16	6	10	6	10
Minimum gap between the bursts	6	16	8	12	8	13
CYLLENE 2A (TSOP1...)						
Minimum burst length	6	19	6	10	6	19
Minimum gap between the bursts	7	20	8	11	8	20
CYLLENE 2B (TSOP5...)						
Minimum burst length	6	10	6	10	6	-
Minimum gap between the bursts	6	10	7	10	7	-
CYLLENE 2C (TSOP3...)						
Minimum burst length	6	10	6	10	6	-
Minimum gap between the bursts	10	12	10	12	10	-

OUTPUT STAGE

As shown in Fig. 1, the digital output of the TSOP IR receiver modules is an open collector transistor with an internal pull up resistor. An additional external pull up resistor can optionally be used if more current is needed to drive the input of the decoding device or if a faster switching time is required. The logic low level will be below 0.2 V even at a sink current of 2 mA. The output can continuously drive a capacitance of up to 1 nF without risk of damaging the output stage.