VOxHx6x - 10 MBd High Speed Optocoupler

1. GENERAL

This document is intended as a guideline for simulating with the provided models and does not constitute a commercial product or a substitute for the datasheet.

1.1. Device Description

The VOxHx6x series of 10 MBd optocouplers utilizes a highly efficient input LED coupled to a high speed integrated photodetector logic gate with a strobable open drain output.

The VOxHx60A are single-channel devices which, depending on the version, provide an additional enable pin input. In contrast to this, the VOxHx63A are dual-channel versions without an enable pin.

The internal shield provides a guaranteed common mode transient immunity of 15 kV/µs.

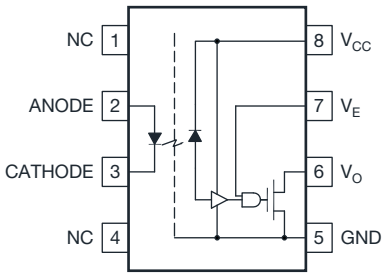


Fig. 1 - Pin Configuration of the VOH260, VOIH060, and VOWH260

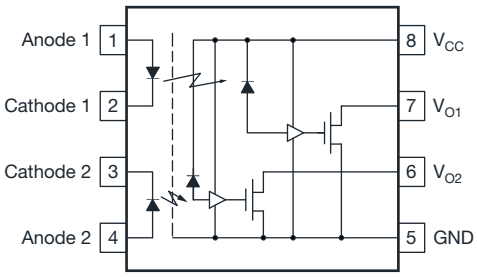


Fig. 2 - Pin Configuration of the VOH263 and VOIH063

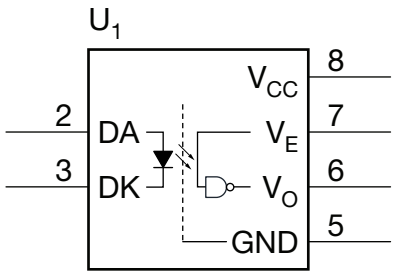
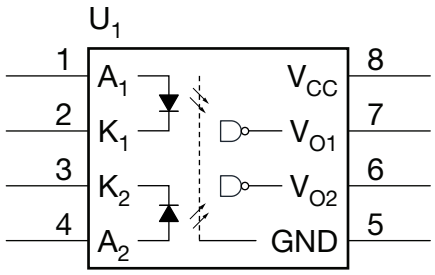
TRUTH TABLE (positive logic)		
LED	**ENABLE**	**OUTPUT**
On	H	L
Off	H	H
On	L	H
Off	L	H
On	Not connected / open	L
Off	Not connected / open	H

1.2. Available Models

Different SPICE models have been written for PSpice and LTspice® and were tested with the OrCAD PSpice 22.1 (2022-S007) and LTspice XVII (17.0.34.0) simulation programs. The simulation results were compared with the datasheet and device characterization data.

The symbol files are available in the symbol library file VOxHx6x_10MBd.olb for PSpice, or specific VOxHx6x.asy files for LTspice (e.g. VOH260.asy).

The model file is named identical VOxHx6x_10MBd.lib for PSpice and LTspice. However, the model files for PSpice and LTspice differ in content.

PART	MODEL DESCRIPTION	SYMBOL FILE	LIBRARY / SYMBOL FILES
VOH260 VOIH060 VOWH260	6-pin optocoupler in 8-pin package, 6-pin symbol, with enable pin and open drain output	 VOH260	PSpice: VOxHx6x_10MBd.lib, VOxHx6x_10MBd.olb LTspice: VOxHx6x_10MBd.lib, VOH260.asy, VOIH060.asy, VOWH260.asy
VOH263 VOIH063	8-pin dual optocoupler, with open drain output	 VOH263	PSpice: VOxHx6x_10MBd.lib, VOxHx6x_10MBd.olb LTspice: VOxHx6x_10MBd.lib, VOH263.asy, VOIH063.asy

1.3. Netlist of Model

The netlists between PSpice and LTspice differ due to incompatible elements of the two simulation programs.

The appropriate models can be downloaded using the links in the table.

1.4. Recommended Operating Conditions

This model is designed only for use at 25 °C and should be used as is.

The supply voltage V_{CC} in the simulation must be between 2.7 V and 5.5 V, otherwise the output level is continuously high (V_{CC}), Fig. 5.

2. SIMULATION RESULTS

The following tables and graphs show comparisons of simulation and measurement results to evaluate the performance and limits of the model.

2.1. Electrical Characteristics

SIMULATED ELECTRICAL PARAMETERS (T_{amb} = 25 °C, unless otherwise specified)							
PARAMETER	**TEST CONDITION**	**SYMBOL**	**DATASHEET**		**SIMULATION**		**UNIT**
			MIN.	**MAX.**	**PSpice**	**LTspice**	
INPUT							
Forward voltage	I_F = 10 mA	V_F	1.38	1.70	1.42	1.42	V
OUTPUT							
Low level output voltage	V_{CC} = 3.3 V, V_E = 2 V, I_F = 5 mA	V_{OL}	0.20	0.60	0.31	0.32	V
Low level output voltage	V_{CC} = 5.5 V, V_E = 2 V, I_F = 5 mA	V_{OL}	0.20	0.60	0.44	0.45	V

Note

- Simulated electrical characteristics compared to the datasheet values

2.2. DC Simulations

The following tables and graphs show simulation results in comparison to the corresponding datasheet values to evaluate the performance and limits of the model.

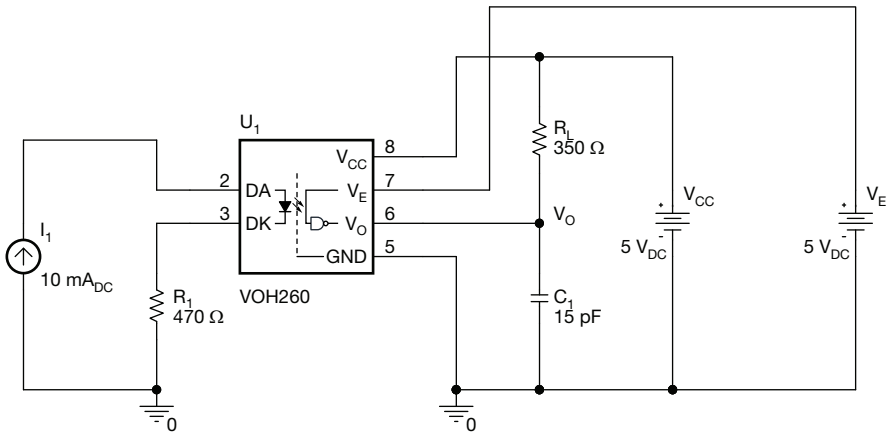


Fig. 3 - Simulation Schematic V_{CC}

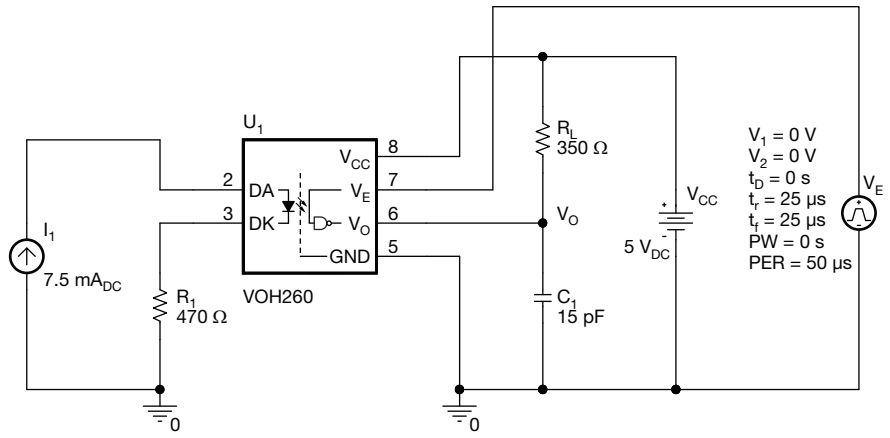


Fig. 4 - Simulation Schematic V_E

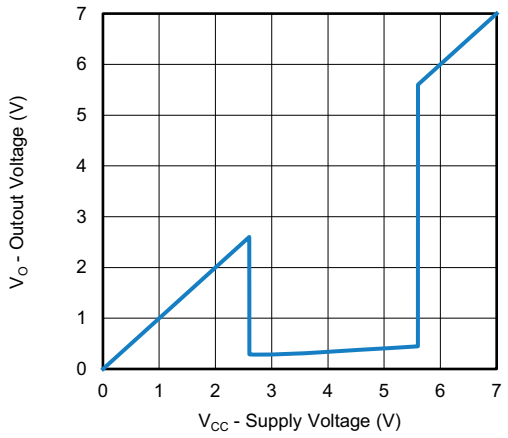


Fig. 5 - Output Voltage vs. Supply Voltage

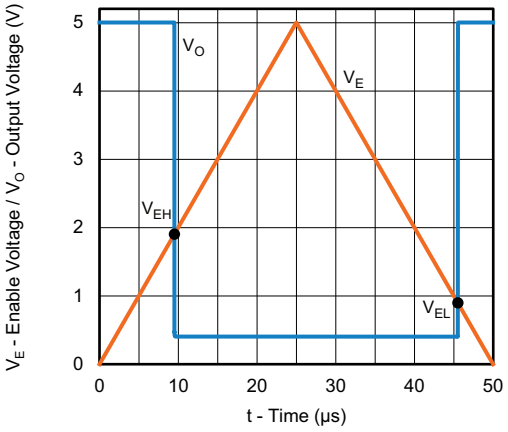


Fig. 6 - Enable Voltage / Output Voltage vs. Time
(only for VOxHx60 in 8-pin package)

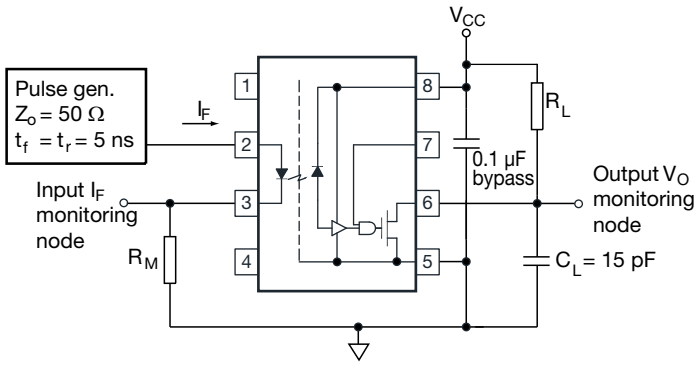
SIMULATED ELECTRICAL PARAMETERS (T_{amb} = 25 °C, unless otherwise specified)							
PARAMETER	**TEST CONDITION**	**SYMBOL**	**DATASHEET**		**SIMULATION**		**UNIT**
			MIN.	**MAX.**	**PSpice**	**LTspice**	
OUTPUT							
Low level enable voltage	V_{CC} = 5 V, I_F = 10 mA	V_{EL}	-	0.8	0.89	0.9	V
High level enable voltage		V_{EH}	2	-	1.9	1.91	V

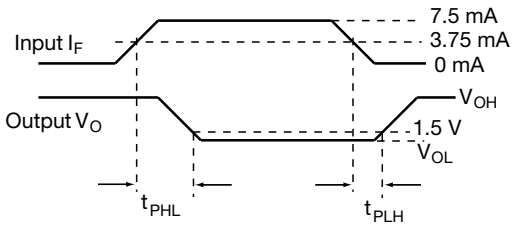
Note

- Simulated enable voltage levels compared to the datasheet values

2.3. Switching Characteristics

2.3.1. Propagation Delay Time





The probe and jig capacitances are included in C_L

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Fig. 7 - Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

SWITCHING CHARACTERISTICS (T_{amb} = -40 °C to +110 °C, 4.5 V ≤ V_{CC} ≤ 5.5 V, I_F = 7.5 mA, unless otherwise specified; typical values are at V_{CC} = 5.0 V, T_{amb} = 25 °C)						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Propagation delay time to high output level	R_L = 350 Ω, C_L = 15 pF, T_{amb} = 25 °C	t_{PLH}	25	50	90	ns
	R_L = 350 Ω, C_L = 15 pF	t_{PLH}	-	-	100	ns
Propagation delay time to low output level	R_L = 350 Ω, C_L = 15 pF, T_{amb} = 25 °C	t_{PHL}	25	40	90	ns
	R_L = 350 Ω, C_L = 15 pF	t_{PHL}	-	-	100	ns
Pulse width distortion	R_L = 350 Ω, C_L = 15 pF	$\|t_{PLH} - t_{PHL}\|$	-	10	-	ns
Propagation delay skew	R_L = 350 Ω, C_L = 15 pF	t_{PSK}	-	-	40	ns
Output rise time (10 % to 90 %)	R_L = 350 Ω, C_L = 15 pF	t_r	-	23	-	ns
Output fall time (90 % to 10 %)	R_L = 350 Ω, C_L = 15 pF	t_f	-	10	-	ns
Propagation delay time of enable from V_{EH} to V_{EL}	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	t_{ELH}	-	15	-	ns
Propagation delay time of enable from V_{EL} to V_{EH}	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	t_{EHL}	-	15	-	ns

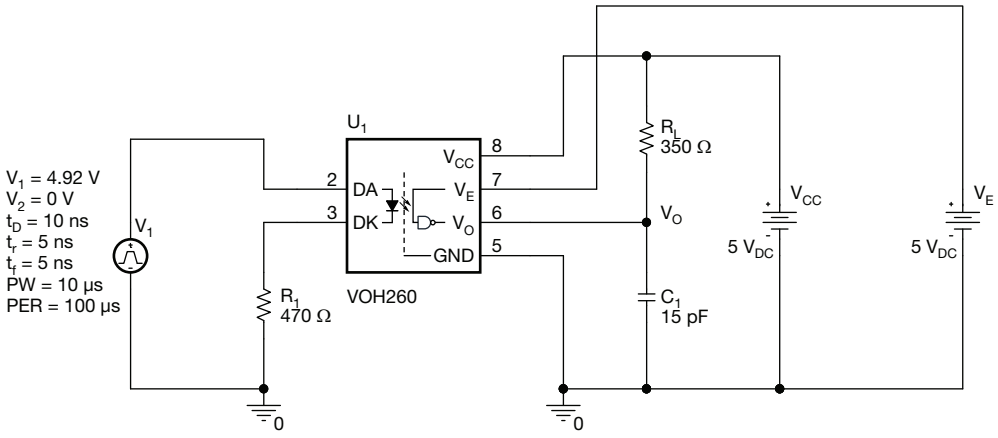


Fig. 8 - Timing Simulation Setup (V_{CC} = 5 V, I_F = 7.5 mA)

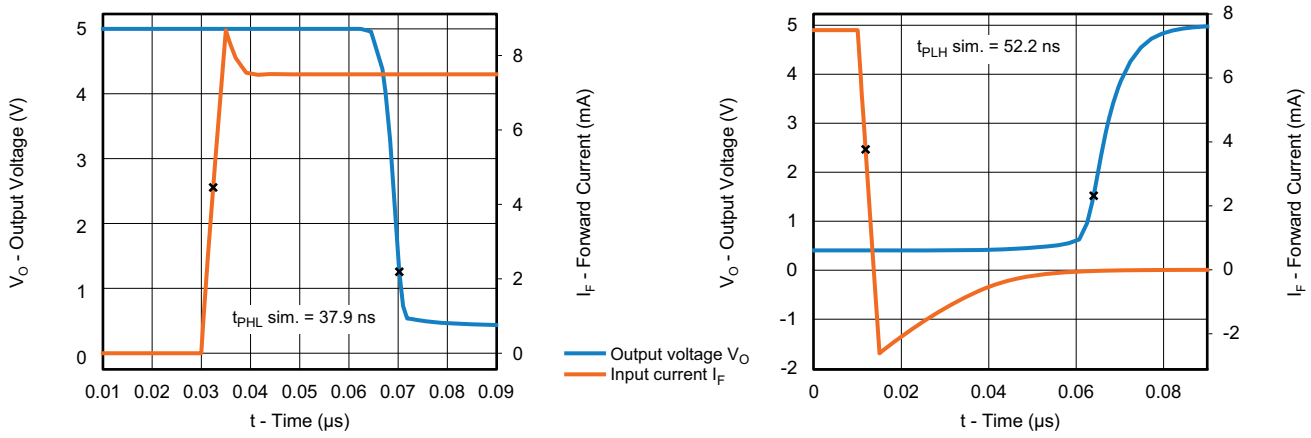


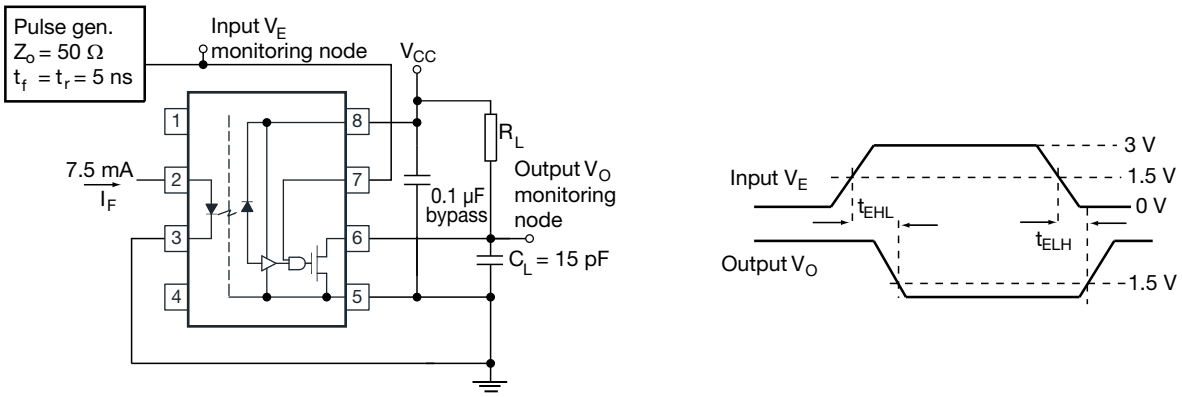
Fig. 9 - Timing Simulation Output Data for t_P

SIMULATED SWITCHING PARAMETERS (T_{amb} = 25 °C, unless otherwise specified)							
PARAMETER	**TEST CONDITION** R_L = 350 Ω, C_L = 15 pF	**SYMBOL**	**DATASHEET**		**SIMULATION**		**UNIT**
			TYP.	**MAX.**	**PSpice**	**LTspice**	
Turn-on time	V_{CC} = 3.3 V, I_F = 7.5 mA	t_{PHL}	40	90	48.8	56.4	ns
Turn-off time		t_{PLH}	50	90	38.0	41.0	ns
Turn-on time	V_{CC} = 5 V, I_F = 7.5 mA	t_{PHL}	40	90	37.9	41.2	ns
Turn-off time		t_{PLH}	50	90	52.2	51.8	ns

Note

- Timing simulation results for t_P in comparison to datasheet

2.3.2. Propagation Delay Time of Enable Input



The probe and jig capacitances are included in C_L

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Fig. 10 - Test Circuit for t_{EHL} and t_{ELH}

SWITCHING CHARACTERISTICS (T_{amb} = -40 °C to +110 °C, 4.5 V ≤ V_{CC} ≤ 5.5 V, I_F = 7.5 mA, unless otherwise specified; typical values are at V_{CC} = 5.0 V, T_{amb} = 25 °C)						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Propagation delay time to high output level	R_L = 350 Ω, C_L = 15 pF, T_{amb} = 25 °C	t_{PLH}	25	50	90	ns
	R_L = 350 Ω, C_L = 15 pF	t_{PLH}	-	-	100	ns
Propagation delay time to low output level	R_L = 350 Ω, C_L = 15 pF, T_{amb} = 25 °C	t_{PHL}	25	40	90	ns
	R_L = 350 Ω, C_L = 15 pF	t_{PHL}	-	-	100	ns
Pulse width distortion	R_L = 350 Ω, C_L = 15 pF	$\lvert t_{PLH} - t_{PHL} \rvert$	-	10	-	ns
Propagation delay skew	R_L = 350 Ω, C_L = 15 pF	t_{PSK}	-	-	40	ns
Output rise time (10 % to 90 %)	R_L = 350 Ω, C_L = 15 pF	t_r	-	23	-	ns
Output fall time (90 % to 10 %)	R_L = 350 Ω, C_L = 15 pF	t_f	-	10	-	ns
Propagation delay time of enable from V_{EH} to V_{EL}	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	t_{ELH}	-	15	-	ns
Propagation delay time of enable from V_{EL} to V_{EH}	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	t_{EHL}	-	15	-	ns

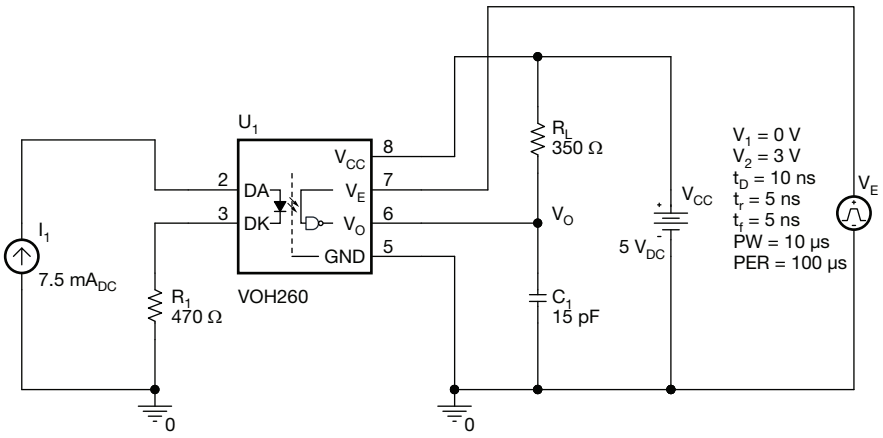

Fig. 11 - Timing Simulation Setup for t_E
(V_{CC} = 5 V, I_F = 7.5 mA)

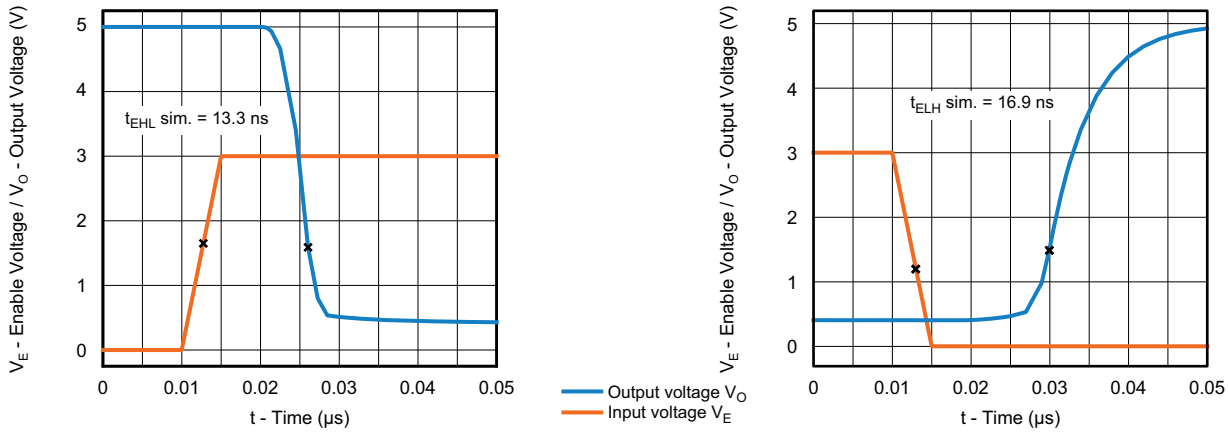

Fig. 12 - Timing Simulation Output Data for t_E

SIMULATED SWITCHING PARAMETERS (T_{amb} = 25 °C, unless otherwise specified)							
PARAMETER	**TEST CONDITION** R_L = 350 Ω, C_L = 15 pF	**SYMBOL**	**DATASHEET**		**SIMULATION**		**UNIT**
			TYP.	**MAX.**	**PSpice**	**LTspice**	
Turn-on time	V_{CC} = 3.3 V, V_{EL} = 0 V, V_{EH} = 3 V, I_F = 7.5 mA	t_{EHL}	15	-	28.0	29.8	ns
Turn-off time		t_{ELH}	15	-	19.9	12.5	ns
Turn-on time	V_{CC} = 5 V, V_{EL} = 0 V, V_{EH} = 3 V, I_F = 7.5 mA	t_{EHL}	15	-	13.3	15.5	ns
Turn-off time		t_{ELH}	15	-	16.9	14.2	ns

Note

- Timing simulation results for t_E in comparison to datasheet