Proximity Sensor With VCSEL in Ultra Thin Small Package, I²C Interface

FEATURES

- Package type: transparent mold with isolation wall
- Dimensions (L x W x H in mm): 1.6 x 1.0 x 0.35
- Integrated modules: vertical-cavity surface-emitting laser (VCSEL) and a proximity sensor (PS)
- Support both 1.2 V and 1.8 V I²C I / O with 1.8 V supply voltage
- I²C interface up to 1 MHz (fast mode plus)
- Present on I³C bus (spike filter implemented)
- Low power consumption with 5 µA idle current
- A small package allows a design with a small window size
- Smart dual I²C slave address in one package
- Immunity to red glow (940 nm VCSEL)
- Programmable I_{VCSEL} sink current
- Intelligent cancellation to reduce cross talk phenomenon
- Smart persistence scheme to reduce measurement response time
- Interrupt functionality
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

e4

RoHS COMPLIANT

HALOGEN FREE GREEN (5-2008)

LINKS TO ADDITIONAL RESOURCES

3D Models

Application Notes

DESCRIPTION

The VCNL36829UM is a fully integrated proximity sensor. It combines a vertical-cavity surface-emitting laser (VCSEL), photodiode, and application-specific integrated circuit (ASIC) within a ultra thin small package. The VCNL36829UM has been developed for proximity detection applications that offers quite some advanced features including dual slave address, low power consumption, smallest volume package design with isolation wall for the best signal to noise ratio performance with the flexible of mechanical design. In addition, given the typical rated supply voltage of 1.8 V to reduce power consumption, the sensor is intended for battery-powered applications.

APPLICATIONS

- True wireless stereo (TWS) earbuds
- VR / AR headsets and smart glasses
- Smart wearables / IOT devices
- Touchless button / dispensing

PRODUCT SUMMARY

PART NUMBER	OPERATING RANGE (mm)	OPERATING VOLTAGE RANGE (V)	I²C BUS VOLTAGE RANGE (V)	MAX. VCSEL DRIVING CURRENT (mA)	ADC RESOLUTION PROXIMITY / AMBIENT LIGHT
VCNL36829UM	50	1.65 to 2.00	1.08 to 3.6	18	16 bit / -

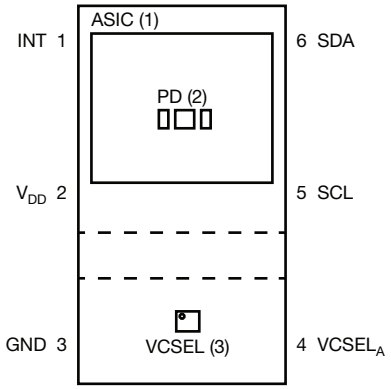
ORDERING INFORMATION

ORDERING CODE	PACKAGING	VOLUME (1)	REMARKS
VCNL36829UM	Tape and reel	MOQ: 5000 pcs, 5000 pcs/reel	1.6 mm x 1.0 mm x 0.35 mm

Note

(1) MOQ: minimum order quantity

PIN DEFINITION



PIN DESCRIPTION			
PIN NUMBER	**PIN NAME**	**TYPE**	**DESCRIPTION**
1	INT	O (open drain)	Interrupt
2	V_{DD}	I	Supply voltage
3	GND	I	Ground
4	$VCSEL_A$	I	VCSEL anode
5	SCL (1)	I / O (open drain)	I^2C serial clock
6	SDA (1)	I / O (open drain)	I^2C serial data

Note

(1) Pin 5 (SCL) and pin 6 (SDA) can be swapped to change the slave address from 0x60 to 0x51; please refer to Table 1

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)					
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**MAX.**	**UNIT**
Supply voltage		V_{DD}	0	2	V
Ambient temperature range		T_{amb}	-40	+85	°C
Storage temperature range		T_{stg}	-40	+100	°C

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
ASIC						
Supply voltage		V_{DD}	1.65	1.80	2.00	V
Supply current (1)	Shutdown state; light condition = dark; V_{DD} = 1.8 V	I_{DD}	-	1	-	µA
	Idle state (2); V_{DD} = 1.8 V		-	5	-	
	Active state (2); V_{DD} = 1.8 V		-	310	-	
I^2C supply voltage		$V_{PULL\ UP}$	1.08	1.8	3.6	V
I^2C signal input, logic high	V_{DD} = 1.8 V	V_{IH}	0.9	-	-	V
I^2C signal input, logic low	V_{DD} = 1.8 V	V_{IL}	-	-	0.45	V
VCSEL						
Supply voltage of the VCSEL (3)		V_{VCSEL}	2.8	-	3.6	V
Forward voltage	I_F = 9 mA	V_F	-	2	-	V
Forward current		I_F	8	-	18	mA
Angle of half intensity	FWHM	φ	-	± 4.5	-	°
Peak wavelength	I_F = 9 mA	λ_p	930	940	955	nm
Spectral bandwidth	I_F = 9 mA	Δλ	-	3	-	nm
PHOTODIODE						
Angle of half sensitivity		φ	-	± 60	-	°
Peak sensitivity wavelength		λ_p	-	850	-	nm

Notes

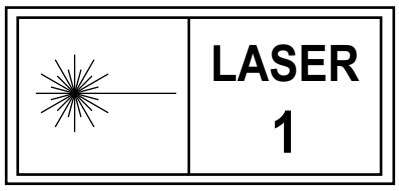
(1) Actual current consumption depends on the register settings. Please refer to the application note on the current consumption

(2) Excluding VCSEL driving current

(3) V_{VCSEL} should at least match the minimum required supply voltage for the VCSEL $V_{VCSEL, min}$. Please refer to the $V_{VCSEL, min}$ table

$V_{VCSEL, MIN.}$						
PS_CURRENT (I_F)	8 mA	10 mA	12 mA	14 mA	16 mA	18 mA
$V_{VCSEL, min.}$	2.80 V	2.90 V	3.00 V	3.08 V	3.16 V	3.22 V
$V_{VCSEL, max.}$	3.6 V					

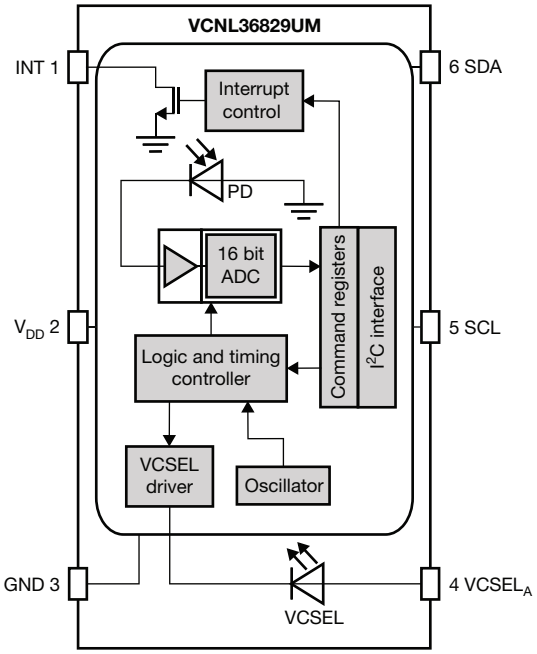
LASER CLASS



Note

- Product specification with IEC / EN 60825-1:2014 compliance and above label

BLOCK DIAGRAM



I²C BUS TIMING CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
Clock frequency	$f_{(I2CCLK)}$	10	100	10	400	kHz
Bus free time between start and stop condition	$t_{(BUF)}$	4.7	-	1.3	-	µs
Hold time after (repeated) start condition; after this period, the first clock is generated	$t_{(HDSTA)}$	4.0	-	0.6	-	µs
Repeated start condition setup time	$t_{(SUSTA)}$	4.7	-	0.6	-	µs
Stop condition setup time	$t_{(SUSTO)}$	4.0	-	0.6	-	µs
Data hold time	$t_{(HDDAT)}$	0	3450	0	900	ns
Data setup time	$t_{(SUDAT)}$	250	-	100	-	ns
I²C clock (SCL) low period	$t_{(LOW)}$	4.7	-	1.3	-	µs
I²C clock (SCL) high period	$t_{(HIGH)}$	4.0	-	0.6	-	µs
Clock / data fall time	$t_{(f)}$	-	300	-	300	ns
Clock / data rise time	$t_{(r)}$	-	1000	-	300	ns

Note

- Data based on standard I²C protocol requirement, not tested in production

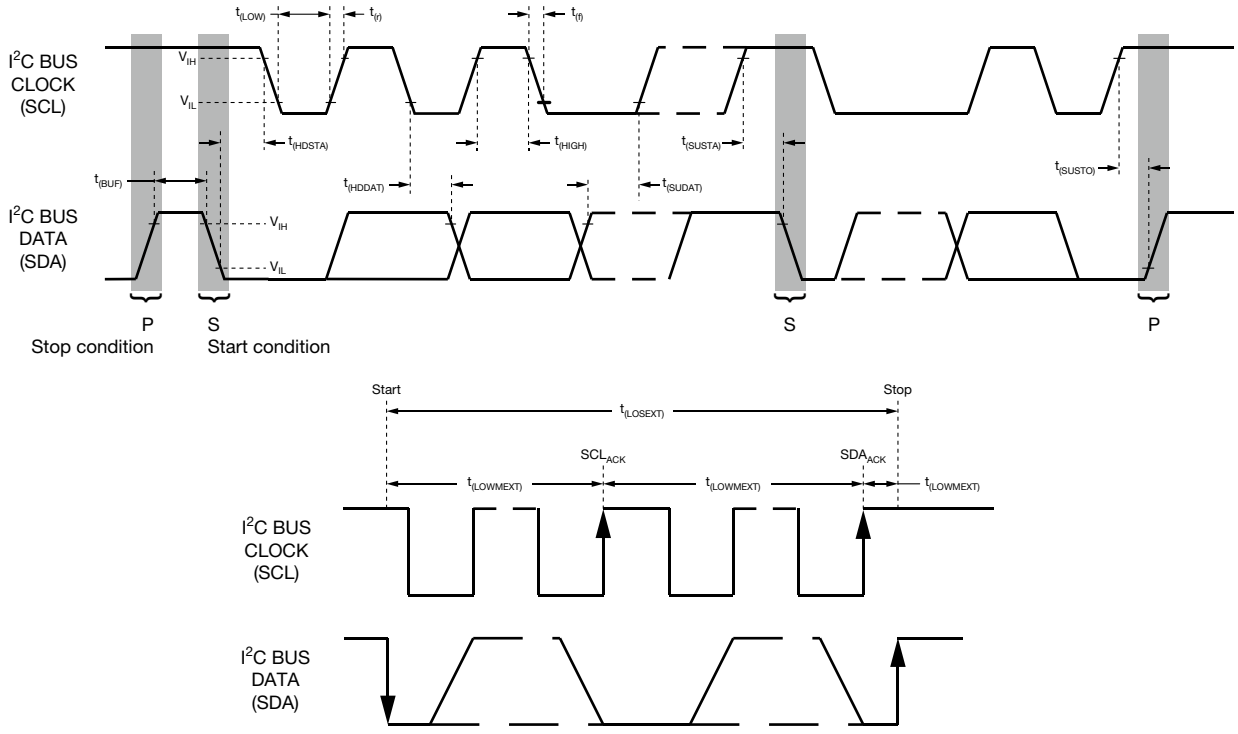


Fig. 1 - I²C Bus Timing Diagram

PARAMETER TIMING INFORMATION

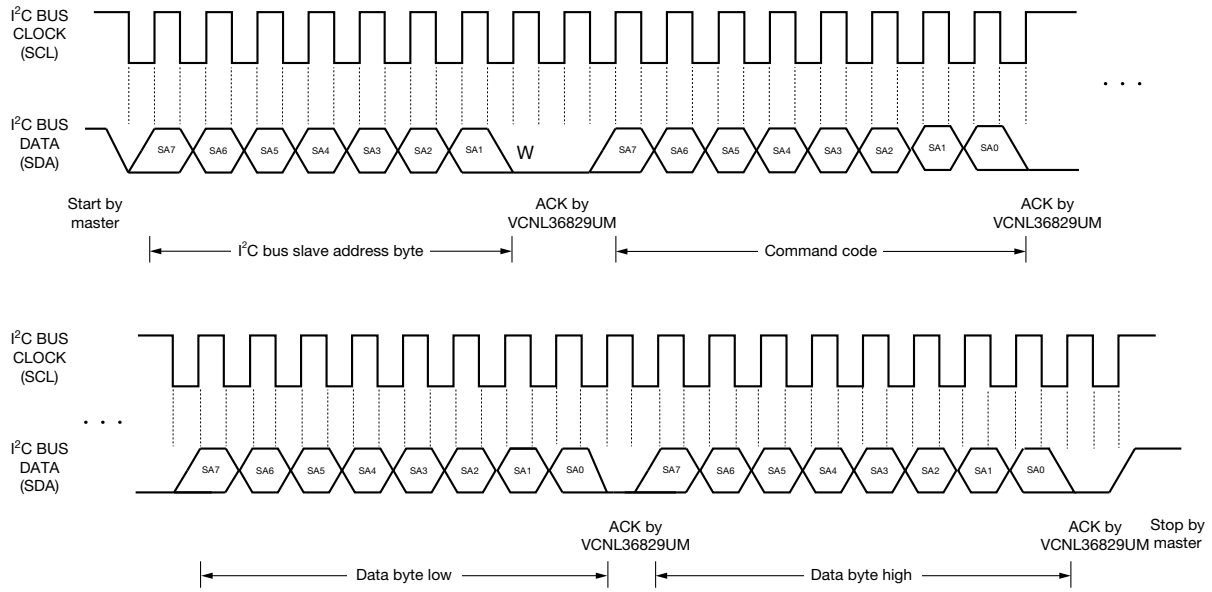


Fig. 2 - I²C Bus Timing for Sending Word Command Format

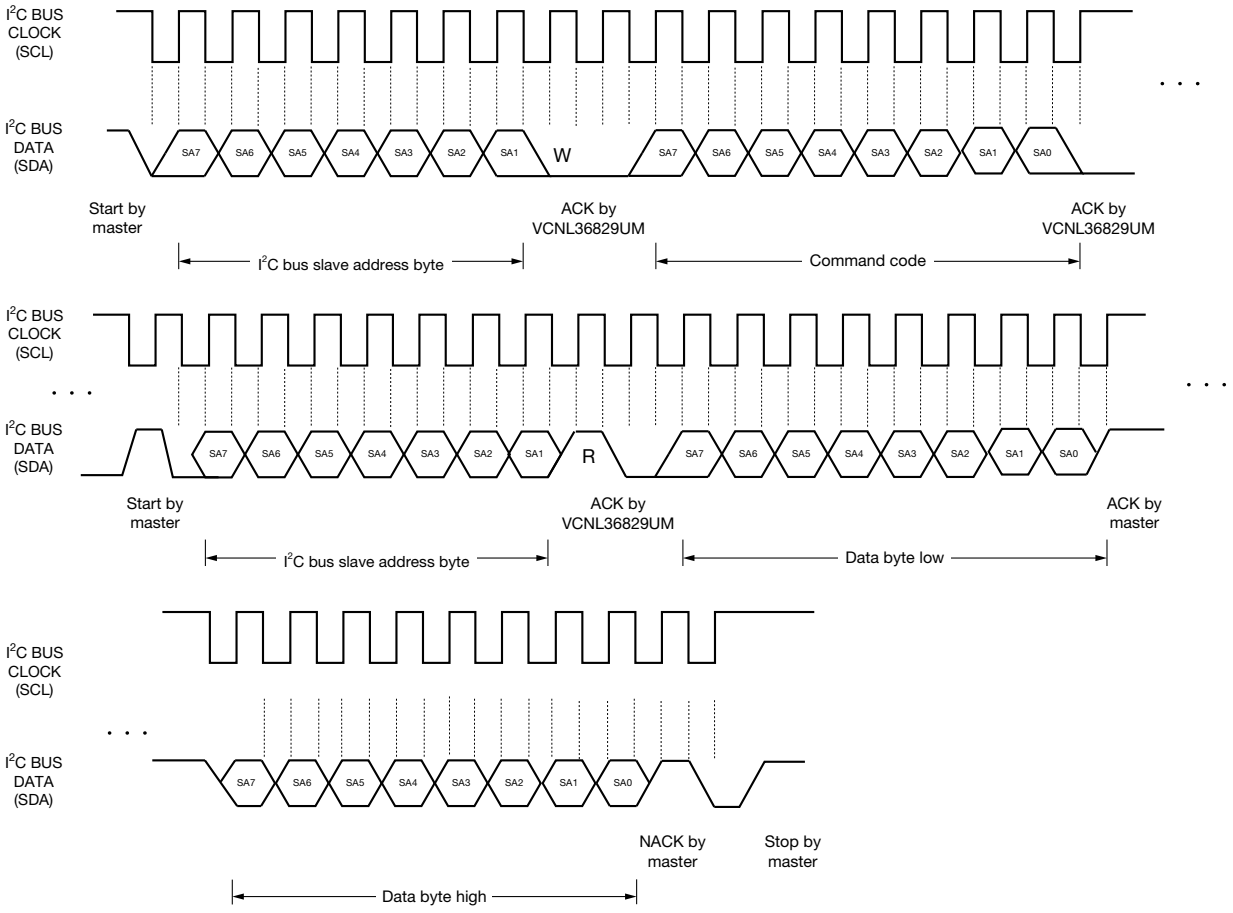


Fig. 3 - I²C Bus Timing for Receiving Word Command Format

TYPICAL PERFORMANCE CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

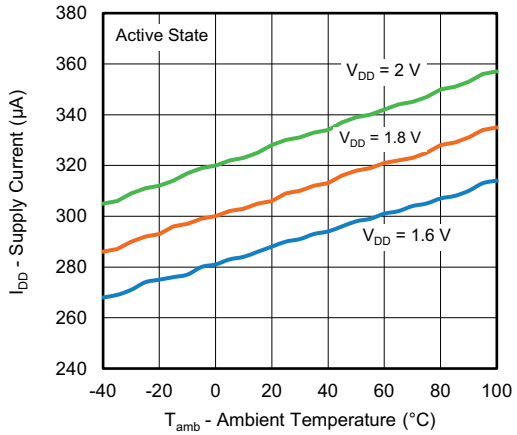


Fig. 4 - Supply Current vs. Ambient Temperature

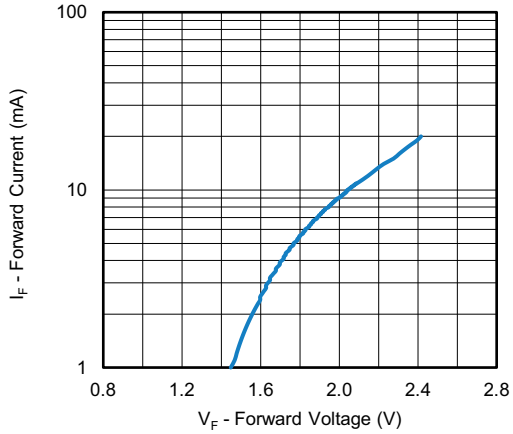


Fig. 5 - Forward Current vs. Forward Voltage of the VCSEL

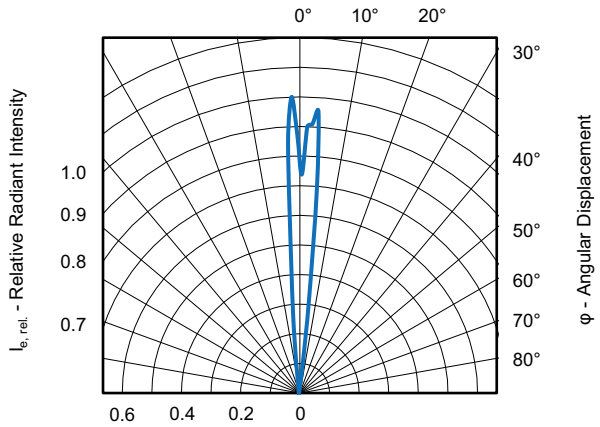


Fig. 6 - Relative Radiant Intensity vs.
Angular Displacement of the VCSEL

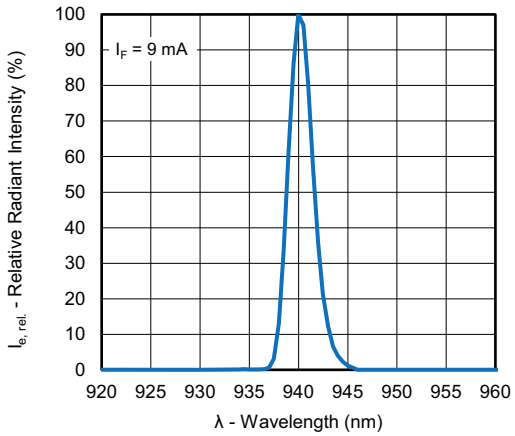


Fig. 7 - Relative Radiant Intensity vs. Wavelength of the VCSEL

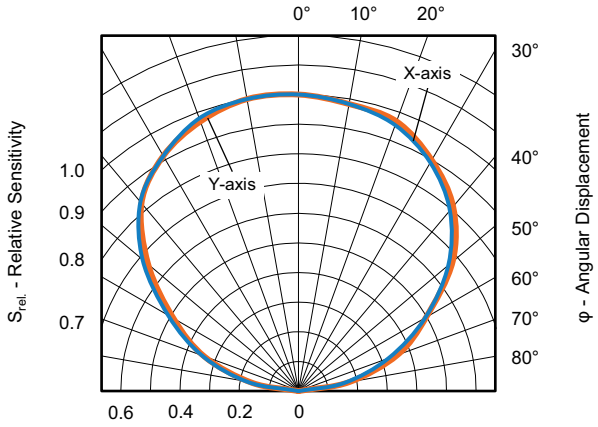


Fig. 8 - Relative Sensitivity vs.
Angular Displacement of the Photodiode

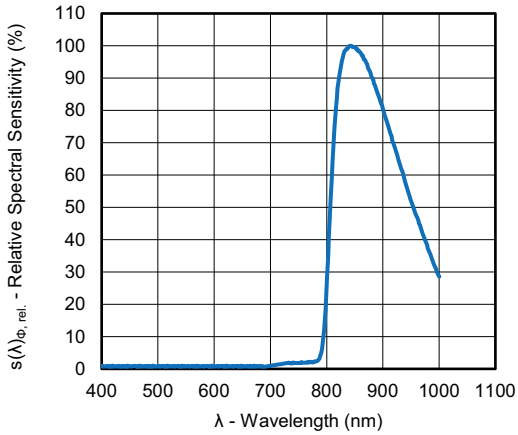


Fig. 9 - Relative Spectral Sensitivity vs.
Wavelength of the Photodiode

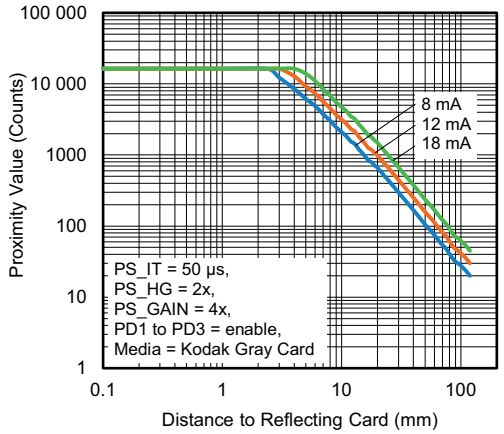


Fig. 10 - Proximity Value vs. Distance (IT = 2T)

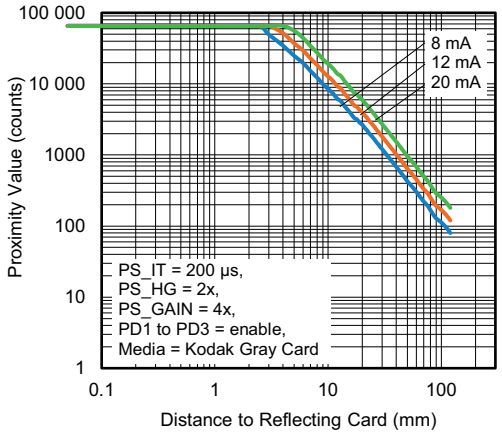


Fig. 11 - Proximity Value vs. Distance (IT = 8T)

APPLICATION INFORMATION

Slave Address Selection

The VCNL36829UM supports a smart dual slave address where the designer can change the slave address by swapping the SCL and SDA pins, as shown in Table 1.

TABLE 1 - SLAVE ADDRESS TABLE

PIN 5	PIN 6	7 BIT SLAVE ADDRESS	8 BIT SLAVE ADDRESS (WRITE)	8 BIT SLAVE ADDRESS (READ)
SCL	SDA	0x60	0xC0	0xC1
SDA	SCL	0x51	0xA2	0xA3

A smart dual slave address provides the flexibility for the designer to connect two devices from two different slave addresses on the same I^2C bus. Besides that, the two slave address options allow designers to select a different slave address if one is used by the other slave devices on the same I^2C bus in a single device application.

To ensure more stable slave address recognition, especially in systems with higher noise levels, it is recommended to follow a specific power-on sequence: apply power to the I^2C bus first, followed by V_{DD}. This sequence helps the IC determine the correct slave address more reliably in noisy environments.

Application Circuit With a Single Device - Slave Address 0x60

Fig. 12 shows an application circuit example with a single device. As described in Table 1, when pins 5 and 6 are connected to the clock and data signal from the microcontroller, as shown in Fig. 12, they will then be configured as an SCL pin and SDA pin, respectively. The 7 bit slave address option of 0x60 will be automatically selected.

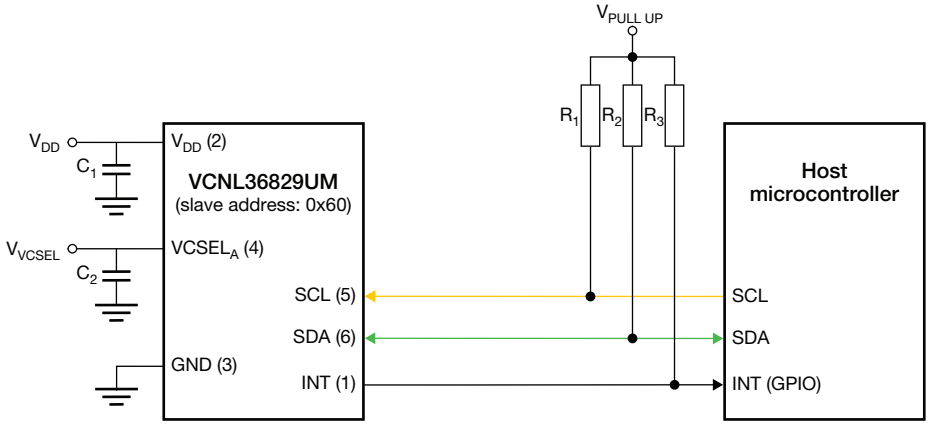


Fig. 12 - Application Circuit Example for a Single VCNL36829UM - Slave Address 0x60

Application Circuit With a Single Device - Slave Address 0x51

On the other hand, when pins 5 and 6 are connected to the data and clock signal from the microcontroller, as shown in Fig. 13, they will then be configured as an SDA pin and SCL pin, respectively. The 7 bit slave address option of 0x51 will be automatically selected.

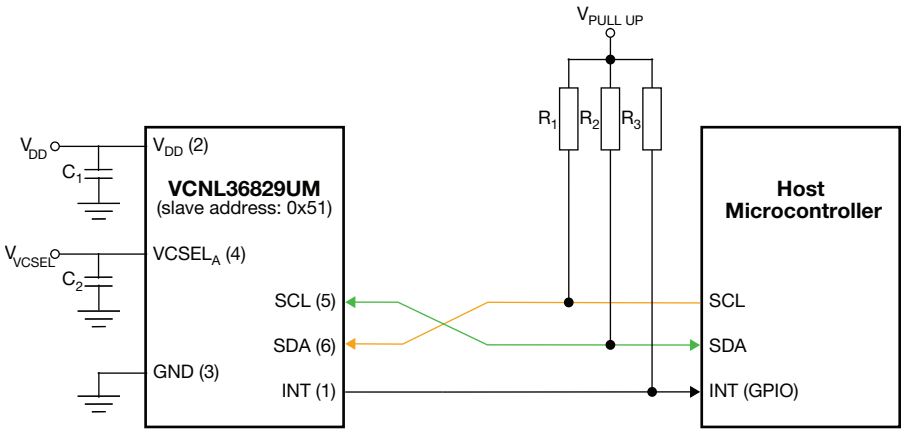


Fig. 13 - Application Circuit Example for a Single VCNL36829UM - Slave Address 0x51

Table 2 shows the required values and the explanation for the individual application circuit parameters.

TABLE 2 - APPLICATION CIRCUIT PARAMETERS

CIRCUIT PARAMETER	VALUE	DESCRIPTION
V_{DD}	1.65 V to 2.00 V	A stable power supply such as a low dropout regulator or a switching regulator is required; the power supply isolation can be further improved with a decoupling capacitor C_1
V_{VCSEL}	2.80 V to 3.60 V	A stable power supply such as a low dropout regulator or a switching regulator that can supply an adequate amount of power (max. VCSEL pulse driving current of 18 mA) is required; the power supply isolation can be further improved with a decoupling capacitor C_2; the minimum voltage depends on the selected driving current of the VCSEL; please refer to Table $V_{VCSEL,\ min.}$ for reference
$V_{PULL\ UP}$	1.2 V to 3.6 V	A stable power supply such as a low dropout regulator or a switching regulator is required; a voltage level shifter is required if the I^2C bus voltage from the microcontroller is higher than 3.6 V
C_1 - C_4	100 nF to 1 µF	Decoupling capacitors are recommended to reduce the noise in the supply voltage
R_1 - R_2	2.2 kΩ to 4.7 kΩ	Pull-up resistors within the range of 2.2 kΩ to 4.7 kΩ are recommended; any increase in bus capacitance or resistance will increase the logic high transition time
R_3	4.7 kΩ to 22 kΩ	Pull-up resistor within the range of 4.7 kΩ to 22 kΩ is recommended

Application Circuit With a Smart Dual Slave Address

Fig. 14 shows an application circuit example with a smart dual slave address. By swapping the SCL and SDA pins of the second device, as shown in Table 1, the designer can change the 7 bit slave address of the VCNL36829UM. This provides the flexibility for the designer to connect two devices from two different slave addresses on the same I²C bus.

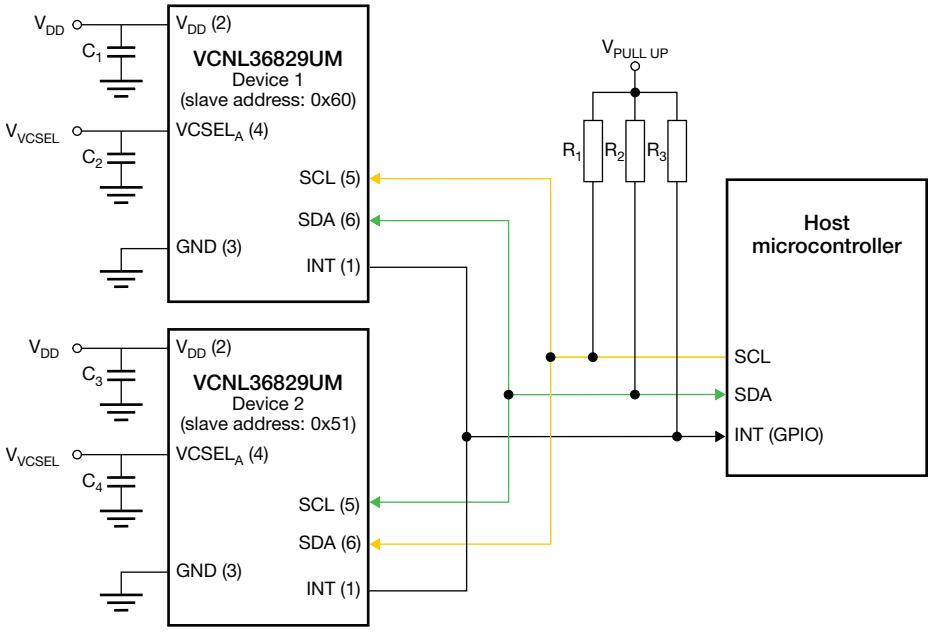


Fig. 14 - Application Circuit Example for Two VCNL36829UMs - Smart Dual Slave Address

I²C Write and Read Protocol

The communication with the VCNL36829UM can be performed via I²C. The I²C write and read protocol when communicating with the proximity sensor is shown in Fig. 15.

Fig. 15 - I²C Write and Read Protocol

It is imperative that only the restart condition for the I²C read is implemented instead of the stop and restart condition.

Function Description

TABLE 3 - COMMAND CODE AND REGISTER DESCRIPTION

COMMAND CODE	DATA BYTE LOW / HIGH	REGISTER NAME	DEFAULT VALUE	FUNCTION	ACCESS
0x00	L	PS_CONF1_L	0x00	Internal calibration setting	Write and read
				Active force mode trigger setting	
				Switch the sensor on / off	
	H	PS_CONF1_H	0x01	Interrupt setting	
				Persistence setting	
				Shutdown setting	
0x01	L	PS_CONF2_L	0x00	Wait time setting	
	H	PS_CONF2_H	0x00	Integration time setting	
0x02	L	PS_CONF3_L	0x00	VCSEL driving current setting	
	H	PS_CONF3_H	0x00	High gain setting	
0x03	L	PS_CONF4_L	0x00	Reserved	
	H	PS_CONF4_H	0x00	Sunlight cancellation setting	
0x04	L	PS_THDL_L	0x00	Low threshold interrupt value setting (low byte)	
	H	PS_THDL_H	0x00	Low threshold interrupt value setting (high byte)	
0x05	L	PS_THDH_L	0x00	High threshold interrupt value setting (low byte)	
	H	PS_THDH_H	0x00	High threshold interrupt value setting (high byte)	
0x06	L	PS_CANC_L	0x00	Offset count cancellation value setting (low byte)	
	H	PS_CANC_H	0x00	Offset count cancellation value setting (high byte)	
0x08	L	PS_CONF5_L	0x00	Reserved (must be set to 0xA0)	
	H	PS_CONF5_H	0x00	Reserved	
0xF8	L	PS_DATA_L	0x00	Proximity output data (low byte)	Read only
	H	PS_DATA_H	0x00	Proximity output data (high byte)	
0xF9	L	Reserved	0x00 to 0xFF	Reserved	
	H	INT_FLAG	0x00	PS interrupt flag	
0xFA	L	VCNL36829UM_ID_L	0x29	Device ID	
	H	VCNL36829UM_ID_H	0x00 / 0x10	Device ID [1] Slave address: 0x60; ID = 0x00 Slave address: 0x51; ID = 0x10	

Notes

- All of the reserved registers are used for internal test. These values must be kept constant.

(1) The default ID depends on the connection of the SCL and SDA pins on the VCNL36829UM with the SCL and SDA pins on the host MCU. If pins 5 and 6 on the VCNL36829UM are connected to the SCL and SDA pins on the host, the default value will be 0x00. On the other hand, if pins 5 and 6 on the VCNL36829UM are connected to the SDA and SCL pins on the host, the default value will be 0x10. Please refer to Fig. 13.

Command Register Format

TABLE 4 - REGISTER NAME: PS_CONF1_L							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PS_CAL	Reserved	PS_TRIG	PS_MODE	Reserved			PS_ON
COMMAND CODE					**0x00**		
Bit Name		**Function**		**Bit**	**Value**	**Description**	
PS_CAL		Enable / disable the internal calibration		7	0x0 (0b0)	Disable (default)	
					0x1 (0b1)	Enable	
Reserved		Reserved		6	0x0 (0b0)	Should be kept default	
PS_TRIG		Set the active force mode trigger; This bit will be reset to 0 after the measurement cycle		5	0x0 (0b0)	Off (default)	
					0x1 (0b1)	Trigger	
PS_MODE		Set the measurement mode of the sensor		4	0x0 (0b0)	Auto Mode (default)	
					0x1 (0b1)	Active force mode	
Reserved		Reserved		3:1	0x0 (0b000)	Should be kept default	
PS_ON		Switch the sensor on / off		0	0x0 (0b0)	Turn off the sensor (shutdown) (default)	
					0x1 (0b1)	Turn on the sensor	

TABLE 5 - REGISTER NAME: PS_CONF1_H							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PS_INT		PS_PERS		PS_SMART_PERS	PS_SP_INT	PS_START_INT	PS_SD
COMMAND CODE					**0x00**		
Bit Name		**Function**		**Bit**	**Value**	**Description**	
PS_INT		Set the interrupt mode setting		15 : 14	0x0 (0b00)	Interrupt disable (default)	
					0x1 (0b01)	Logic High/Low mode	
					0x2 (0b10)	First high	
					0x3 (0b11)	Trigger by each high/low threshold event	
PS_PERS		Set the amount of consecutive threshold crossing events necessary to trigger interrupt		13 : 12	0x0 (0b00)	1 time (default)	
					0x1 (0b01)	2 times	
					0x2 (0b10)	3 times	
					0x3 (0b11)	4 times	
PS_SMART_PERS		Enable / disable the smart persistence setting when the interrupt event is triggered		11	0x0 (0b0)	Disable (default)	
					0x1 (0b1)	Enable	
PS_SP_INT		Enable / disable the sunlight protection mode interrupt setting		10	0x0 (0b0)	Disable (default)	
					0x1 (0b1)	Enable	
PS_START_INT		After PS_SD disable, PS 1st detection Interrupt enable setting		9	0x0 (0b0)	Disable (default)	
					0x1 (0b1)	Enable	
PS_SD		PS shutdown setting		8	0x0 (0b0)	Disable	
					0x1 (0b1)	Enable (default)	

TABLE 6 - REGISTER NAME: PS_CONF2_L							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PS_WAIT							
COMMAND CODE					**0x01**		
Bit Name		Function		**Bit**	**Value**	**Description**	
PS_WAIT		PS wait time after PS detection		7 : 0	0 to 254	2.5 ms x (PS_WAIT + 1)	

TABLE 7 - REGISTER NAME: PS_CONF2_H							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved				PS_IT			
COMMAND CODE					**0x01**		
Bit Name		**Function**		**Bit**	**Value**	**Description**	
Reserved		Reserved		15 : 12	0x0 (0b0000)	Should be kept default	
PS_IT		Set the integration time for one measurement		11 : 8	0x0 (0b0000)	12.5 µs (default)	
					1 to 15	25 µs x PS_IT	

TABLE 8 - REGISTER NAME: PS_CONF3_L							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				PS_CURRENT_EN	PS_CURRENT		
COMMAND CODE					**0x02**		
Bit Name		**Function**		**Bit**	**Value**	**Description**	
Reserved		Reserved		7 : 4	0x0 (0b0000)	Should be kept default	
PS_CURRENT_EN		VCSEL driver enable setting		3	0x0 (0b0)	Disable (default)	
					0x1 (0b1)	Enable	
PS_CURRENT		Set the VCSEL driving current		2 : 0	0x0 (0b000)	Reserved (default)	
					0x1 (0b001)	Reserved	
					0x2 (0b010)	8 mA	
					0x3 (0b011)	10 mA	
					0x4 (0b100)	12 mA	
					0x5 (0b101)	14 mA	
					0x6 (0b110)	16 mA	
					0x7 (0b111)	18 mA	

TABLE 9 - REGISTER NAME: PS_CONF3_H							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved	PS_HG	PS_GAIN		Reserved	PD3_EN	PD2_EN	PD1_EN
COMMAND CODE					**0x02**		
Bit Name		**Function**		**Bit**	**Value**	**Description**	
Reserved		Reserved		15	0x0 (0b0)	Should be kept default	
PS_HG		Set the gain of the ADC		14	0x0 (0b0)	x1 gain (default)	
					0x1 (0b1)	x2 gain	
PS_GAIN		Set the gain of the ADC		13 : 12	0x0 (0b00)	x4 gain (default)	
					0x1 (0b01)	x2 gain	
					0x2 (0b10)	x1 gain	
					0x3 (0b11)	Reserved	
Reserved		Reserved		11	0x0 (0b0)	Should be kept default	
PD3_EN		PD3 enable setting		10	0x0 (0b0)	Disable (default)	
					0x1 (0b1)	Enable	
PD2_EN		PD2 enable setting		9	0x0 (0b0)	Disable (default)	
					0x1 (0b1)	Enable	
PD1_EN		PD1 enable setting		8	0x0 (0b0)	Disable (default)	
					0x1 (0b1)	Enable	

TABLE 10 - REGISTER NAME: PS_CONF4_L							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							
COMMAND CODE					**0x03**		
Bit Name		**Function**		**Bit**	**Value**	**Description**	
Reserved		Reserved		7 : 0	0x0 (0b00000000)	Should be kept default	

TABLE 11 - REGISTER NAME: PS_CONF4_H							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved				PS_SC_LEVEL		PS_SC	Reserved
COMMAND CODE					**0x03**		
Bit Name		**Function**		**Bit**	**Value**	**Description**	
Reserved		Reserved		15 : 12	0xF (0b1111)	Should be kept default	
PS_SC_LEVEL		Sunlight cancellation level setting		11 : 10	0x0 (0b00)	Level 1 (default)	
					0x1 (0b01)	Level 2	
					0x2 (0b10)	Level 3	
					0x3 (0b11)	Level 4	
PS_SC		Enable / disable the sunlight cancellation		9	0x0 (0b0)	Disable (default)	
					0x1 (0b1)	Enable	
Reserved		Reserved		8	0x0 (0b0)	Should be kept default	

TABLE 12 - REGISTER NAME: PS_THDL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PS_THDL_L							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PS_THDL_H							
COMMAND CODE					**0x04**		
Bit Name		**Function**		**Bit**	**Value**	**Description**	
PS_THDL_L		Set the low threshold interrupt value		7 : 0	0 to 65 535	Low byte	
PS_THDL_H				15 : 8		High byte	

TABLE 13 - REGISTER NAME: PS_THDH							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PS_THDH_L							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PS_THDH_H							
COMMAND CODE					**0x05**		
Bit Name		**Function**		**Bit**	**Value**	**Description**	
PS_THDH_L		Set the high threshold interrupt value		7 : 0	0 to 65 535	Low byte	
PS_THDH_H				15 : 8		High byte	

TABLE 14 - REGISTER NAME: PS_CANC							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PS_CANC_L							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved				PS_CANC_H			
COMMAND CODE					**0x06**		
Bit Name		**Function**		**Bit**	**Value**	**Description**	
PS_CANC_L		Set the offset count cancellation value		7 : 0	0 to 4095	Low byte	
PS_CANC_H				11 : 8		High byte	
Reserved		Reserved		15 : 12	0x0 (0b0000)	Should be kept default	

TABLE 15 - REGISTER NAME: PS_CONF5							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved							
COMMAND CODE					**0x08**		
Bit Name		**Function**		**Bit**	**Value**	**Description**	
Reserved		Reserved		7 : 4	0x0 (0b0000)	Must be set to “0xA (0b1010)”	
Reserved		Reserved		3 : 0	0x0 (0b0000)	Should be kept default	
Reserved		Reserved		15 : 8	0x0 (0b00000000)	Should be kept default	

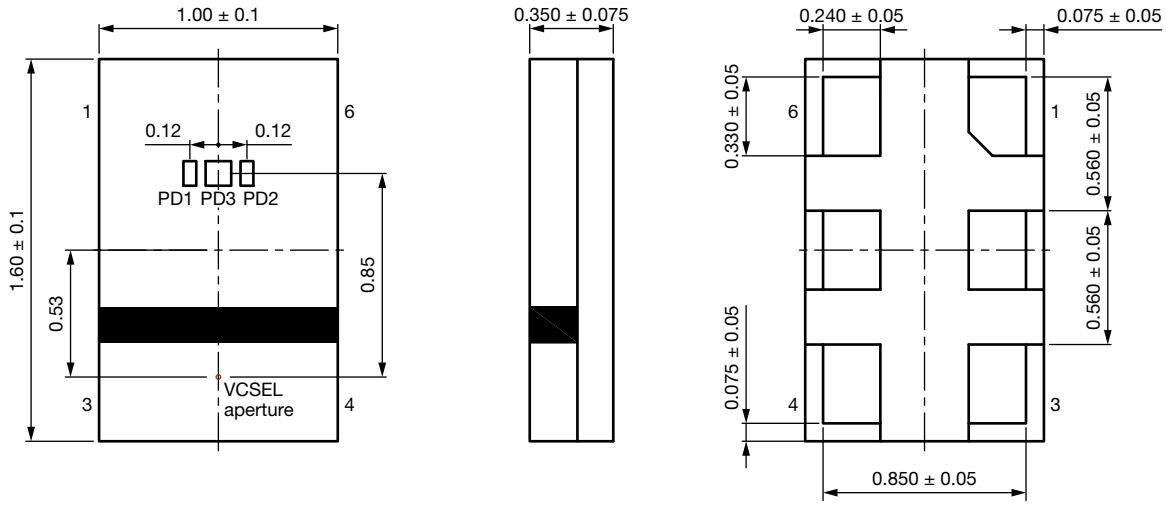
TABLE 16 - REGISTER NAME: PS_DATA							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PS_DATA_L							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PS_DATA_H							
COMMAND CODE					**0xF8**		
Bit Name		**Function**		**Bit**	**Value**	**Description**	
PS_DATA_L		Read the proximity output data		7 : 0	0 to 65 535	Low byte	
PS_DATA_H				15 : 8		High byte	

TABLE 17 - REGISTER NAME: INT_FLAG							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved				PS_START_FLAG	PS_SPFLAG	PS_IF_CLOSE	PS_IF_AWAY
COMMAND CODE					**0xF9**		
Bit Name		**Function**		**Bit**	**Value**	**Description**	
Reserved		Reserved		7 : 0	0x00 - 0xFF (0b00000000 - 0b11111111)	Should be kept default	
Reserved		Reserved		15 : 12	0x0 (0b0000)	Should be kept default	
PS_START_FALG		PS finish 1st detection after SD disable		11	0x0 (0b0)	No 1st detection flag	
					0x1 (0b1)	Finish 1st detection flag	
PS_SPFLAG		Read the sunlight protection mode interrupt event flag		10	0x0 (0b0)	No sunlight protection mode flag	
					0x1 (0b1)	Sunlight protection mode flag	
PS_IF_CLOSE		Read the high threshold crossing interrupt event flag		9	0x0 (0b0)	No high threshold crossing interrupt event flag	
					0x1 (0b1)	High threshold crossing interrupt event flag	
PS_IF_AWAY		Read the low threshold crossing interrupt event flag		8	0x0 (0b0)	No low threshold crossing interrupt event flag	
					0x1 (0b1)	Low threshold crossing interrupt event flag	

TABLE 18 - REGISTER NAME: VCNL36829UM_ID							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCNL36829UM_ID_L							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
VCNL36829UM_ID_H							

COMMAND CODE			0xFA	
Bit Name	**Function**	**Bit**	**Value**	**Description**
VCNL36829UM_ID_L	Read the device ID	7 : 0	0x29 (0b00101001)	Should be kept default
		15 : 8	0x00 (0b00000000)	Device with a slave address of 0x60
VCNL36829UM_ID_H			0x10 (0b00010000)	Device with a slave address of 0x51

PACKAGE INFORMATION in millimeters



1	INT	4	$VCSEL_A$
2	V_{DD}	5	SCL
3	GND	6	SDA

Fig. 16 - VCNL36829UM Package Dimensions

RECOMMENDED LAYOUT PAD INFORMATION in millimeters

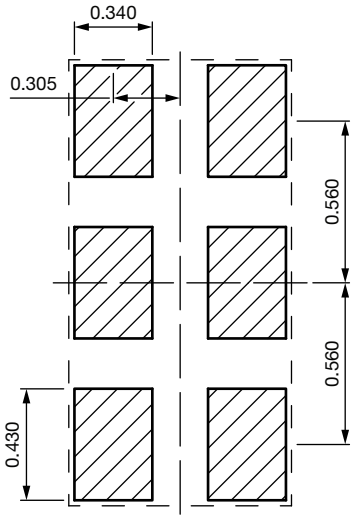


Fig. 17 - VCNL36829UM PCB Layout Footprint

RECOMMENDED INFRARED REFLOW

Soldering conditions which are based on J-STD-020C

IR REFLOW PROFILE CONDITION			
PARAMETER	**CONDITIONS**	**TEMPERATURE**	**TIME**
Peak temperature		260 °C + 5 °C / - 5 °C (max.: 265 °C)	10 s
Preheat temperature range and timing		150 °C to 200 °C	60 s to 180 s
Timing within 5 °C to peak temperature		-	10 s to 30 s
Timing maintained above temperature / time		217 °C	60 s to 150 s
Timing from 25 °C to peak temperature		-	8 min (max.)
Ramp-up rate		3 °C/s (max.)	-
Ramp-down rate		6 °C/s (max.)	-

Recommend normal solder reflow is 235 °C to 265 °C

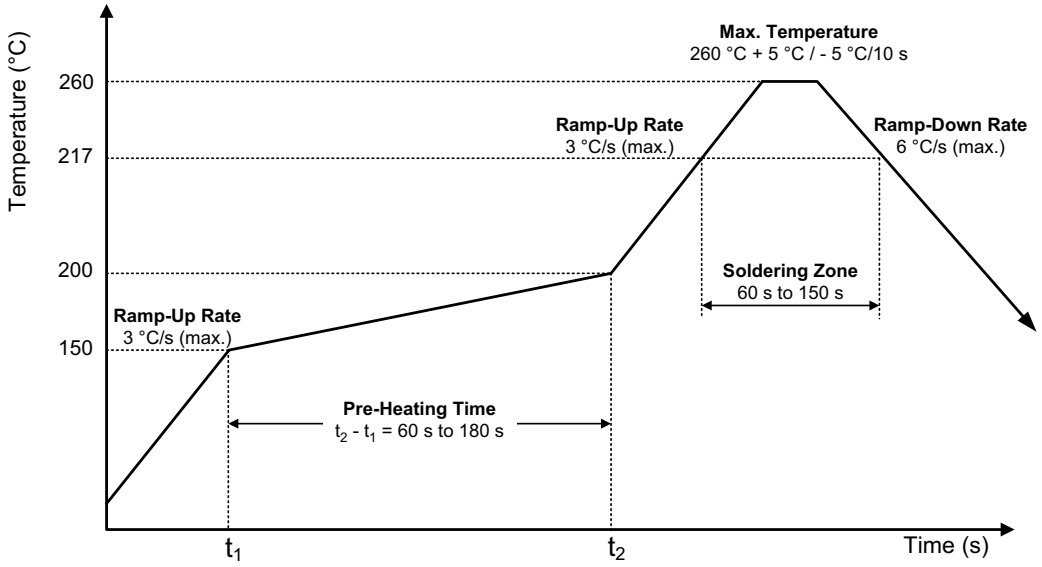
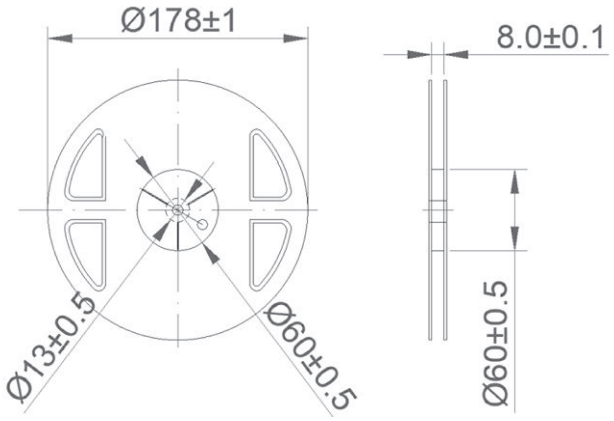
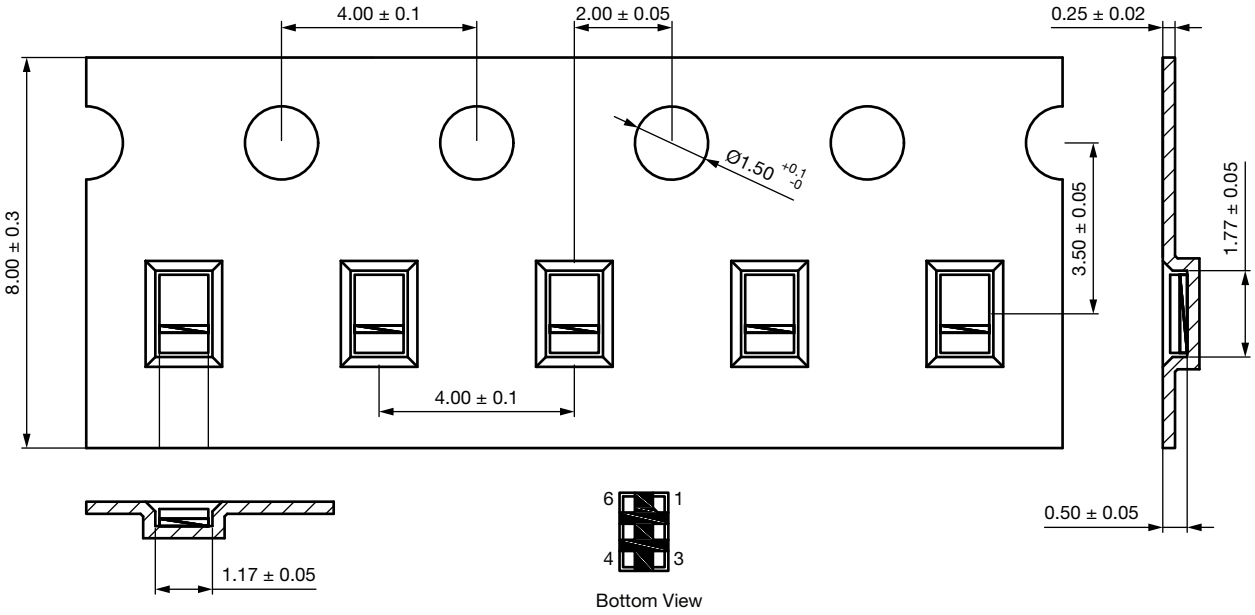


Fig. 18 - VCNL36829UM Solder Reflow Profile Chart

TAPE PACKAGING INFORMATION in millimeters





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