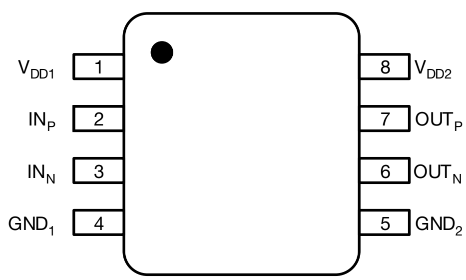
High Thermal Stability Isolation Amplifier



DESCRIPTION

The VIA0050DD is a high performance differential output isolated amplifier ideally suited for shunt based current sensing. The device is based on proprietary capacitive isolation technology and has a linear differential input signal range of ± 50 mV (± 64 mV full scale).

The device has a fixed gain of 41 and provides a differential analog output.

The low offset drift typ. 0.15 μV/°C and low gain drift typ. 15 ppm/°C ensures a good accuracy over the entire temperature range. The devices unmatched CMTI of 100 kV/μs allows accurate measurements in the noisy environment.

FEATURES

- Isolation test voltage: 5000 V_{RMS}
- ± 50 mV linear input voltage range
- Fixed gain: 41
- gain error and drift: ± 0.05 % typ., ± 15 ppm/°C typ.
- Low non-linearity and drift: ± 0.03 % max., ± 1 ppm/°C typ.
- SNR: 72 dB (typ., BW = 100 kHz)
- Wide bandwidth: 250 kHz
- High CMTI: 100 kV/μs min.
- Inbuilt common-mode overvoltage detection
- Operating temperature: -40 °C to + 125°C
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
e3
RoHS COMPLIANT
HALOGEN FREE
GREEN (5-2008)

LINKS TO ADDITIONAL RESOURCES

Product Page | Application Notes | 3D Models | SPICE Models | Ultra Librarian EDA / CAD | Design Tools | Infographics

APPLICATIONS

- Isolated current measurement in:
  - Motor control applications
  - Power supplies
  - Solar and wind energy storage systems
  - Charging stations and EV powertrain
  - Inverter and converters
- Battery management
- 48 V board net

Note

- For automotive qualification please contact our local sales.

AGENCY APPROVALS

- UL
- cUL
- DIN EN 60747-5-5 (VDE 0884-5)
- CQC

DEVICE INFORMATION		
PART NUMBER	PACKAGE	BODY SIZE
VIA0050DD	SOP-8 (300 mil)	5.85 mm x 7.50 mm

ORDERING INFORMATION							
PART NUMBER	ISOLATION RATING (kV)	LINEAR INPUT RANGE (mV)	MOISTURE SENSITIVITY LEVEL	TEMPERATURE (°C)	AUTOMOTIVE	PACKAGE TYPE	SPQ
VIA0050DD	5	-50 to +50	Level 3	-40 to +125	No	SOP-8 (300 mil)	1000

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)			
PARAMETER	**SYMBOL**	**VALUE**	**UNIT**
Power supply voltage	V_{DD1}, V_{DD2}	-0.3 to 6.5	V
Input voltage	IN_P, IN_N	GND_{1-6} to $V_{DD1+0.5}$	V
Output voltage	OUT_P, OUT_N	$GND_{2-0.5}$ to $V_{DD2+0.5}$	V
Output current per output pin	I_O	-10 to +10	mA
Operating temperature	T_{amb}	-40 to +125	°C
Junction temperature	T_j	-40 to +150	°C
Storage temperature	T_{stg}	-55 to +150	°C
Electrostatic discharge	HBM (1)	± 2000	V
	CDM (2)	± 1000	V

Notes

(1) Human body model (HBM), per AEC-Q100-002-RevD

(2) Charged device model (CDM), per AEC-Q100-011-RevB

FUNCTIONAL BLOCK DIAGRAM

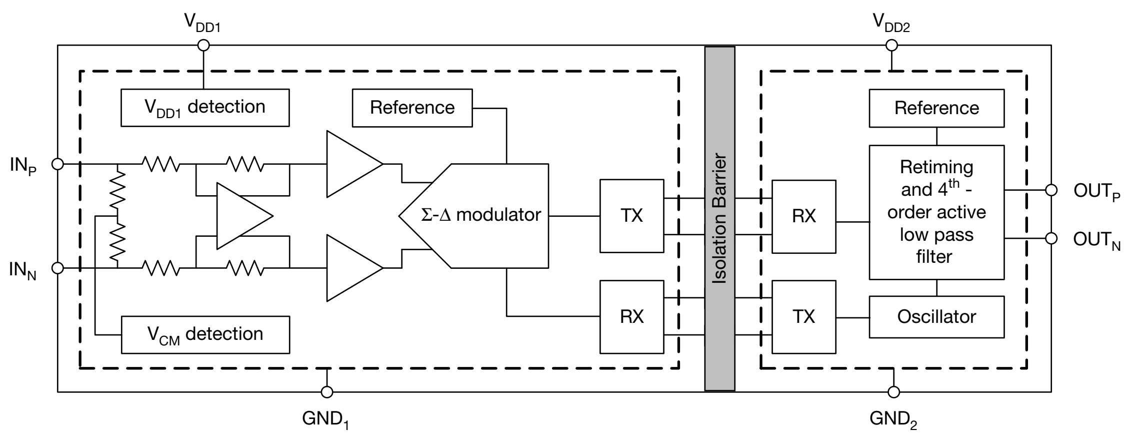


Fig. 1 - VIA0050DD Block Diagram

RECOMMENDED OPERATING CONDITIONS (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER		**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Side 1 power supply		V_{DD1}	3.0	5.0	5.5	V
Side 2 power supply		V_{DD2}	3.0	3.3	5.5	V
VIA0050DD	Differential input voltage before clipping output	$V_{clipping}$	-	± 64	-	mV
	Linear differential input full scale voltage	V_{FSR}	-50	-	+50	mV
	Operating common-mode input voltage	V_{CM}	-0.032	-	0.8	V
Operating ambient temperature		T_{amb}	-40	-	+125	°C

PIN CONFIGURATION AND FUNCTIONS

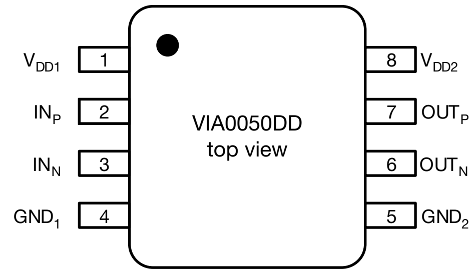


Fig. 2 - VIA0050DD Package

PIN CONFIGURATION AND DESCRIPTION		
PIN NO.	**SYMBOL**	**FUNCTION**
1	V_{DD1}	Power supply for isolator side 1 (3.0 V to 5.5 V)
2	IN_P	Positive analog input (± 50 mV recommended for VIA0050DD)
3	IN_N	Negative analog input
4	GND_1	Ground 1, the ground reference for isolator side 1
5	GND_2	Ground 2, the ground reference for isolator side 2
6	OUT_N	Negative output
7	OUT_P	Positive output
8	VDD_2	Power supply for isolator side 2 (3.0 V to 5.5 V)

ELECTRICAL CHARACTERISTICS: VIA0050DD (V_{DD1}, V_{DD2} = 3 V to 5.5 V, IN_P = -50 mV to +50 mV, IN_N = GND_1 = 0 V, T_{amb} = -40 °C to +125 °C) (V_{DD1} = 5 V, V_{DD2} = 3.3 V, T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
POWER SUPPLY						
Side 1 supply voltage		V_{DD1}	3.0	5.0	5.5	V
Side 2 supply voltage		V_{DD2}	3.0	3.3	5.5	V
Side 1 supply current		I_{DD1}	-	11.4	15.1	mA
Side 2 supply current		I_{DD2}	-	6.3	8.4	mA
V_{DD1} undervoltage detection threshold voltage	V_{DD1} falling	V_{DD1_UV}	1.8	2.3	2.7	V
ANALOG INPUT						
Common-mode overvoltage detection level	Detection level has a typical hysteresis of 96 mV	V_{CMov}	0.9	-	-	V
Input offset voltage	IN_P = IN_N = GND_1	V_{OS}	-0.1	± 0.01	+0.1	mV
Input offset drift		TCV_{OS}	-0.8	± 0.15	+1	μV/°C
Common-mode rejection ratio	IN_P = IN_N, f_{IN} = 0 Hz, $V_{CM\ min.} \leq V_{IN} \leq V_{CM\ max.}$	$CMRR_{DC}$	-	-120	-	dB
	IN_P = IN_N, f_{IN} = 10 Hz, $V_{CM\ min.} \leq V_{IN} \leq V_{CM\ max.}$	$CMRR_{AC}$	-	-112	-	dB
Single-ended input resistance	IN_N = GND_1	R_{IN}	-	4.75	-	kΩ
Differential input resistance		R_{IND}	-	4.9	-	kΩ
Input capacitance		C_I	-	2	-	pF
Input bias current	IN_P = IN_N = GND_1, $I_{IB} = (I_{IBP} + I_{IBN})/2$	I_{IB}	-29	-22	-14	μA
Input bias current drift		TCI_{IB}	-	± 1.5	-	nA/°C
ANALOG OUTPUT						
Nominal gain			-	41	-	V/V
Gain error		E_G	-0.3	± 0.05	+0.3	%
Gain error thermal drift		TCE_G	-50	± 15	+50	ppm/°C
Non-linearity			-0.03	± 0.01	+0.03	%
Non-linearity drift			-	± 1	-	ppm/°C
Total harmonic distortion	V_{IN} = 100 mV_{pp}, f_{IN} = 10 kHz, BW = 100 kHz	THD		-85	-	dB
Output noise	IN_P = IN_N = GND_1, BW = 100 kHz		-	260	-	μV_{RMS}
Signal to noise ratio	V_{IN} = 100 mV_{pp}, f_{IN} = 1 kHz, BW = 10 kHz	SNR	80	84	-	dB
	V_{IN} = 100 mV_{pp}, f_{IN} = 10 kHz, BW = 100 kHz		-	72	-	dB
Common-mode output voltage		V_{CMout}	1.39	1.44	1.49	V
Fail-safe differential output voltage	$V_{CM} > V_{CMov}$, or V_{DD1} missing	$V_{Fail\text{-}Safe}$	-	-2.6	-2.5	V
Output bandwidth		BW	250	310	-	kHz
Power supply rejection ratio (1)	PSRR vs. V_{DD1}, at DC	$PSRR_{DC}$	-	-118	-	dB
	PSRR vs. V_{DD1}, 100 mV and 10 kHz ripple	$PSRR_{AC}$	-	-116	-	dB
	PSRR vs. V_{DD2}, at DC	$PSRR_{DC}$	-	-108	-	dB
	PSRR vs. V_{DD2}, 100 mV and 10 kHz ripple	$PSRR_{AC}$	-	-97	-	dB
Output resistance		R_{OUT}	-	< 0.2	-	Ω
Output short-circuit current		$I_{OUT.OC}$	-	± 13	-	mA
Common-mode transient immunity		CMTI	100	150	-	kV/μs
TIMING						
Rising time of OUT_P, OUT_N		t_r	-	1.3	-	μs
Falling time of OUT_P, OUT_N		t_f	-	1.3	-	μs
IN_P, IN_N to OUT_P, OUT_N signal delay (50 % to 50 %)		t_{PD}	-	1.6	2.1	μs
Analog setting time	V_{DD1} step to 3.0 V with $V_{DD2} \geq 3.0$ V, to OUT_P, OUT_N valid, 0.1 % settling	t_{AS}	-	0.5	-	ms

Note

(1) Input referred

THERMAL INFORMATION			
PARAMETER	SYMBOL	VALUE	UNIT
Junction to ambient thermal resistance	$R_{\theta JA}$	86	°C/W
Junction to case (top) thermal resistance	$R_{\theta JC(top)}$	28	°C/W
Junction to board thermal resistance	$R_{\theta JB}$	42	°C/W
Junction to top characterization parameter	Ψ_{JT}	4	°C/W
Junction to board characterization parameter	Ψ_{JB}	42	°C/W

TYPICAL CHARACTERISTICS

(V_{DD1} = 5 V, V_{DD2} = 3.3 V, V_{IN} = -50 mV to +50 mV)

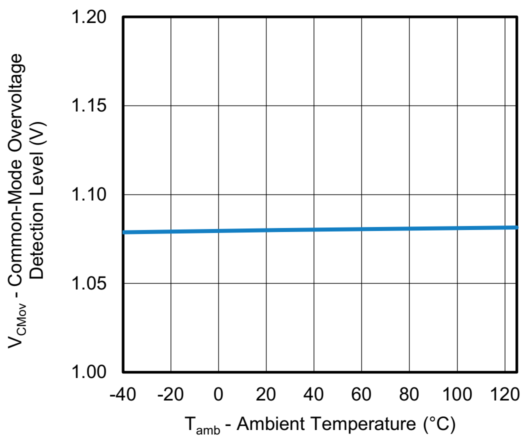


Fig. 3 - Common-Mode Overvoltage Detection Level vs. Ambient Temperature

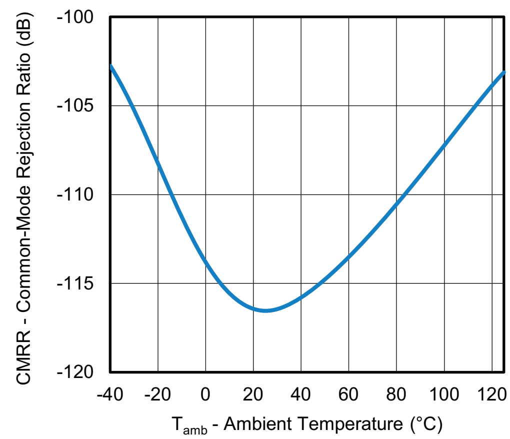


Fig. 5 - Common-Mode Rejection Ratio vs. Ambient Temperature

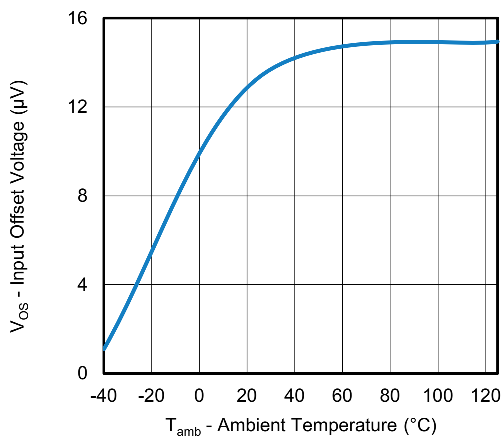


Fig. 4 - Input Offset Voltage vs. Ambient Temperature

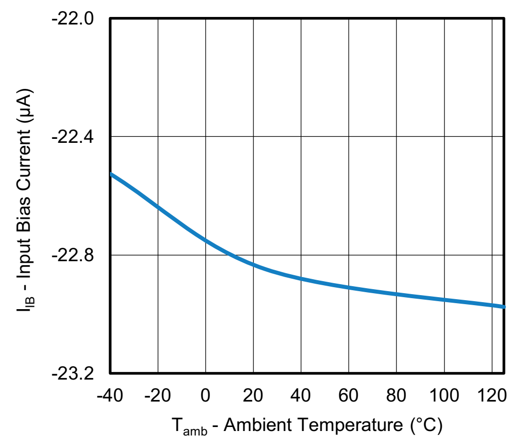


Fig. 6 - Input Bias Current vs. Ambient Temperature

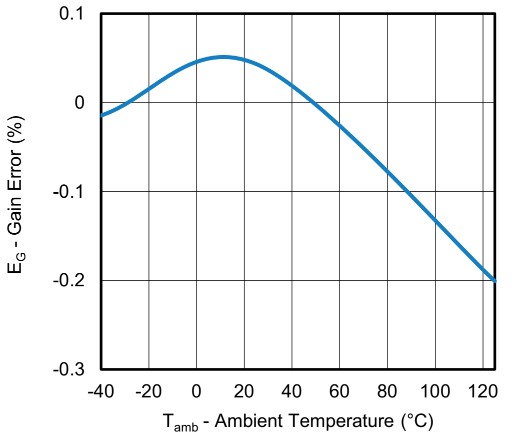


Fig. 7 - Gain Error vs. Ambient Temperature

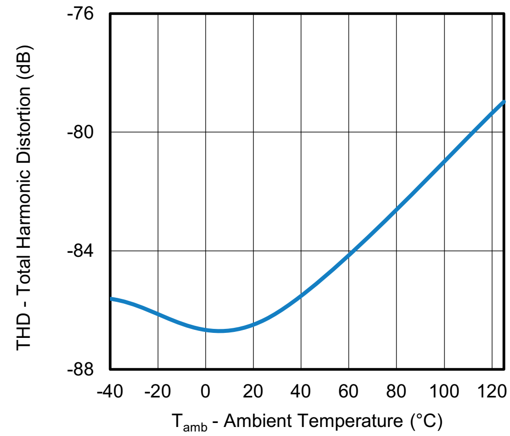


Fig. 10 - Total Harmonic Distortion vs. Ambient Temperature

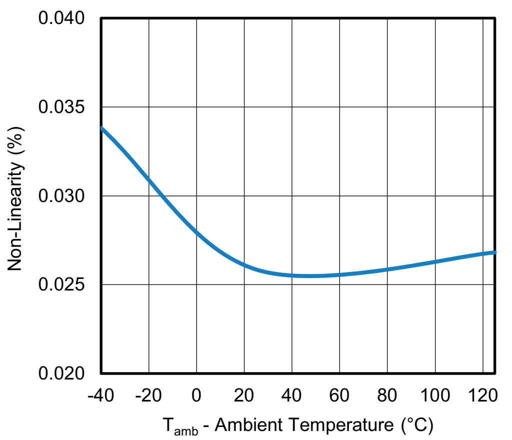


Fig. 8 - Non-Linearity vs. Ambient Temperature

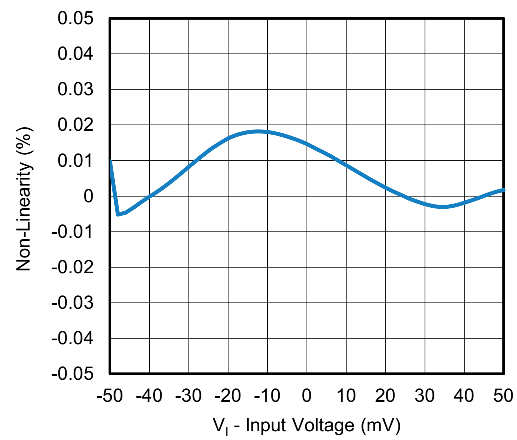


Fig. 11 - Non-Linearity vs. Input Voltage

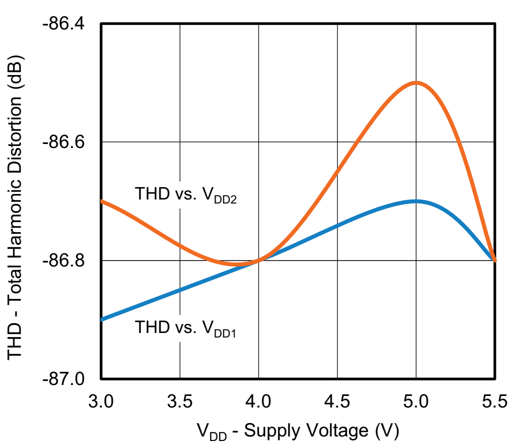


Fig. 9 - Total Harmonic Distortion vs. Supply Voltage

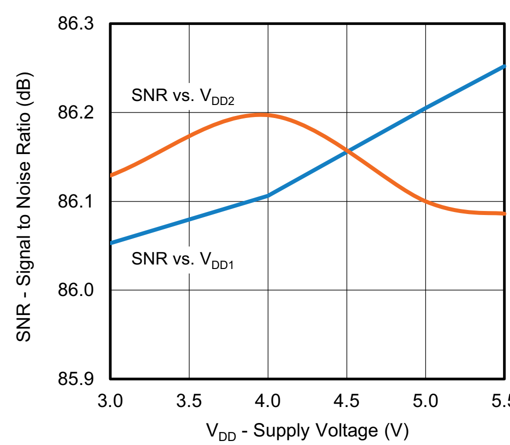


Fig. 12 - Signal to Noise Ratio vs. Supply Voltage

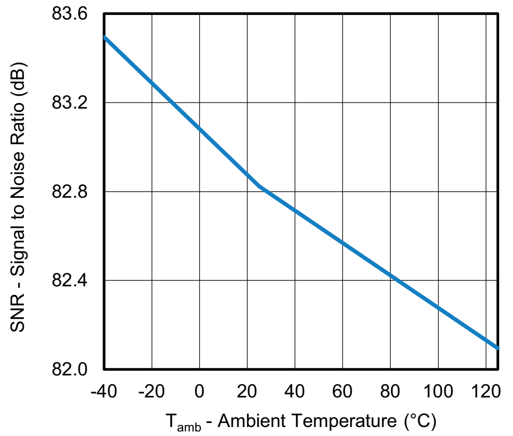


Fig. 13 - Signal to Noise Ratio vs. Ambient Temperature

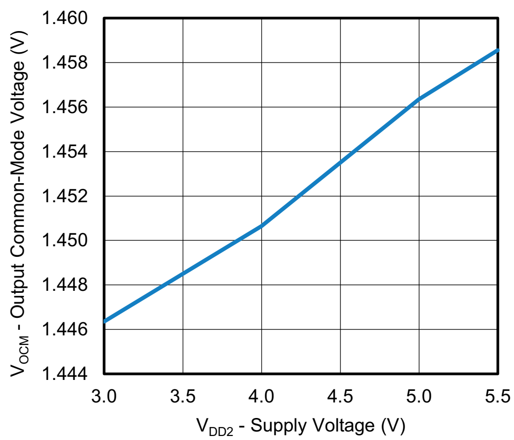


Fig. 14 - Output Common-Mode Voltage vs. Supply Voltage

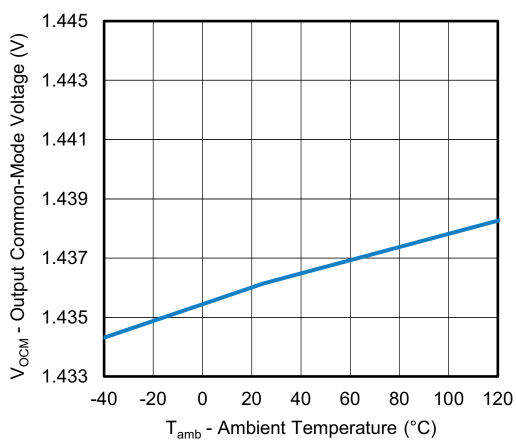


Fig. 15 - Output Common-Mode Voltage vs. Ambient Temperature

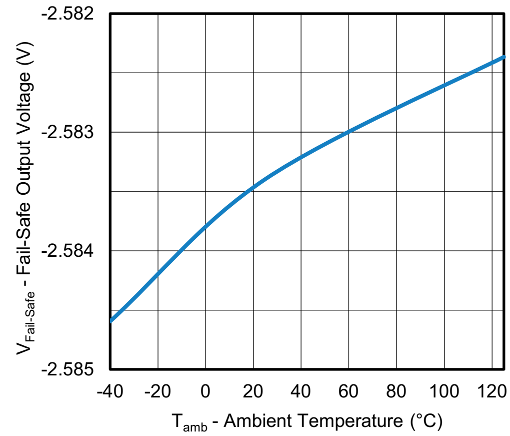


Fig. 16 - Fail-Safe Output Voltage vs. Ambient Temperature

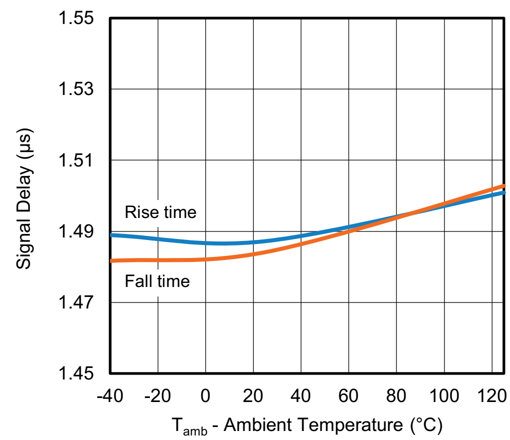


Fig. 17 - Signal Delay vs. Ambient Temperature

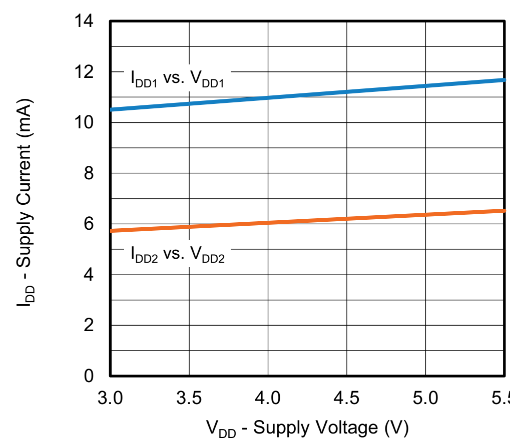


Fig. 18 - Supply Current vs. Supply Voltage

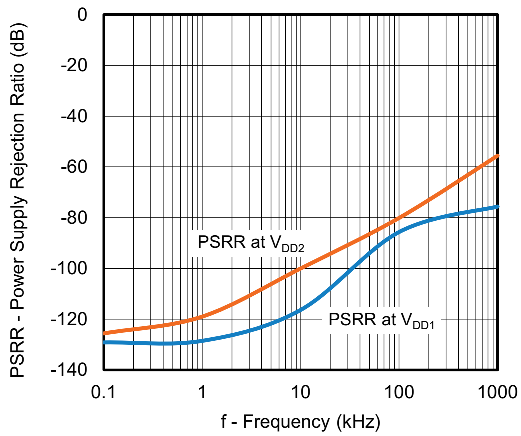


Fig. 19 - Power Supply Rejection Ratio vs. Ripple Frequency

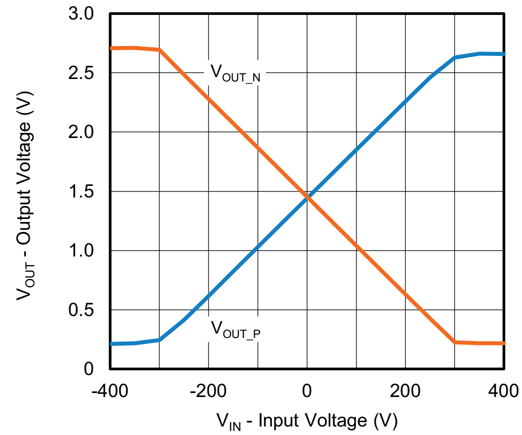


Fig. 21 - Output Voltage vs. Input Voltage

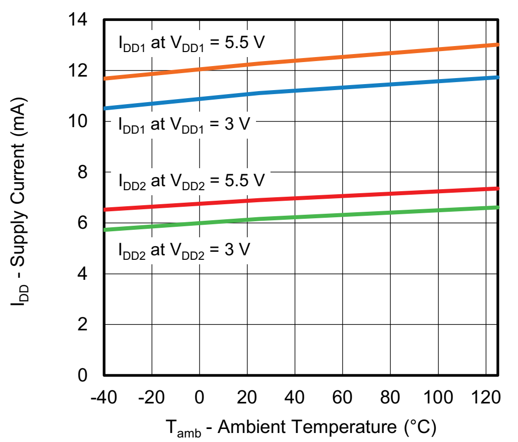


Fig. 20 - Supply Current vs. Ambient Temperature

PARAMETER MEASUREMENT INFORMATION

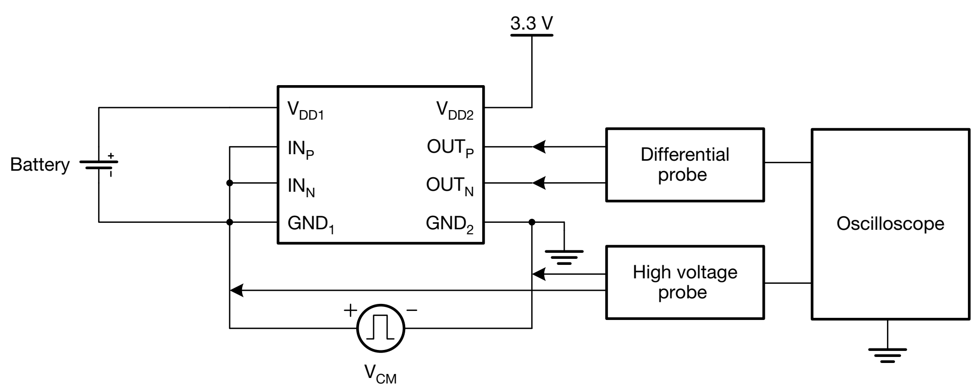


Fig. 22 - Common-Mode Transient Immunity Test Circuit

SAFETY AND INSULATION RATINGS				
PARAMETER	**TEST CONDITION**	**SYMBOL**	**VALUE**	**UNIT**
Climatic classification	According to IEC 68 part 1		40 / 125 / 21	
Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	CTI	> 600	
Maximum rated withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 1 min (qualification); V_{TEST} = 1.2 x V_{ISO}, t = 1 s (100 % production test)	V_{ISO}	5000	V_{RMS}
Maximum transient isolation voltage	t = 1 min	V_{IOTM}	8000	V_{peak}
Maximum repetitive isolation voltage		V_{IORM}	2121	V_{peak}
Maximum surge isolation voltage	Test method per IEC 60065, 1.2/50 μs waveform, $V_{TEST} = V_{IOSM}$ x 1.6	V_{IOSM}	6250	V_{peak}
Maximum working isolation voltage	AC voltage	V_{IOWM}	1500	V_{RMS}
	DC voltage		2121	V_{DC}
Isolation resistance	T_{amb} = 25 °C, V_{IO} = 500 V	R_{IO}	> 10^{12}	Ω
	T_{amb} = 125 °C, V_{IO} = 500 V	R_{IO}	> 10^{10}	Ω
	T_{amb} = 150 °C, V_{IO} = 500 V	R_{IO}	> 10^{9}	Ω
Total power dissipation at 25 °C	θ_{JA} = 86 °C/W, V_I = 5.5 V, T_j = 150 °C, T_{amb} = 25 °C	P_S	1430	mW
Safety input, output, or supply current	θ_{JA} = 86 °C/W, V_I = 5.5 V, T_j = 150 °C, T_{amb} = 25 °C	I_S	260	mA
Maximum safety temperature		T_S	150	°C
Creepage distance	SOP-8 (300 mils)		≥ 8	mm
Clearance distance			≥ 8	mm
Insulation thickness	Distance through insulation	DTI	32	μm
Material group	IEC 60664-1		I	
For rated mains voltage ≤ 150 V_{RMS}			I to IV	
For rated mains voltage ≤ 300 V_{RMS}			I to IV	
For rated mains voltage ≤ 400 V_{RMS}			I to IV	
Pollution degree per DIN VDE 0110, table 1			2	
Input to output test voltage, method B1	V_{IORM} x 1.875 = $V_{pd(m)}$, 100 % production test; $t_{ini} = t_m$ = 1 s, partial discharge < 5 pC	$V_{pd(m)}$	3977	V_{peak}
After environmental tests subgroup 1	V_{IORM} x 1.6 = $V_{pd(m)}$, t_{ini} = 1 s, t_m = 10 s, partial discharge < 5 pC	$V_{pd(m)}$	3394	V_{peak}
Isolation capacitance	f = 1 MHz	C_{IO}	0.8	pF

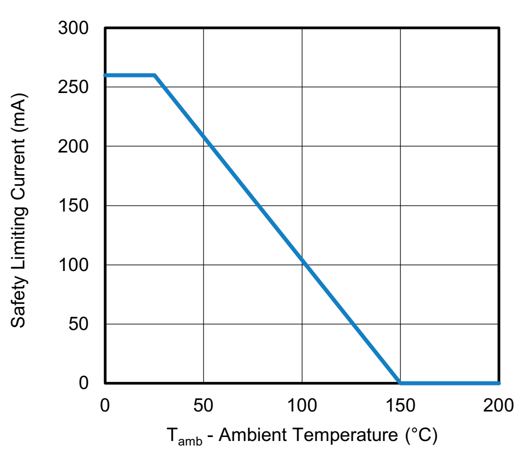


Fig. 23 - VIA0050DD Thermal Derating Curve, Dependence of Safety Limiting Values With Case Temperature per DIN VOE V0884-11

FUNCTION DESCRIPTION

Overview

The VIA0050DD is a high performance isolated amplifier that accept fully-differential input. The fully-differential input is ideally suited to shunt current monitoring in high voltage applications where isolation is required. The analog input is continuously sampled by a second-order - modulator in the device, which is driven by a pre-stage fully-differential amplifier in the device. With the internal voltage reference and clock generator, the modulator convert the analog input signal to a digital bitstream. The output of the modulator is transferred by the drivers (called TX in the functional block diagram) across the isolation barrier that separates the isolated side 1 and side 2 voltage. The received bitstream and clock are synchronized and processed, as shown in the functional block diagram, by a fourth-order analog filter on the side 2 and has a differential output.

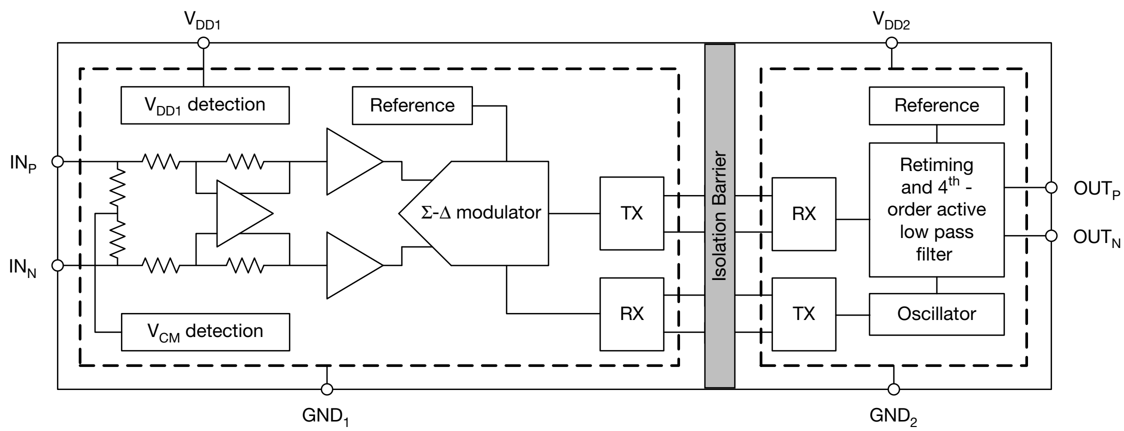


Fig. 24 - Function Block Diagram

Analog Input

Below mentioned are the restrictions on the analog input signal (V_{IN}).

1. If the input voltage exceeds the range GND_1 - 6 V to V_{DD1} + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on
2. The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range

Analog Output

For linear input range, the analog output of VIA0050DD has a fixed gain of 41. If a full-scale input signal is applied to the VIA0050DD ($V_I \geq V_{anosing}$), the analog output will be clipped (typically, 2.45 V for positive clipping and -2.45 V for negative clipping).

In addition, VIA0050DD integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail safe output is a negative differential output voltage that is activated in the conditions mentioned below. Please note that the fail safe output does not occur during normal operation.

1. When the undervoltage of V_{DD1} is detected ($V_{DD1} < V_{DD1uv}$)
2. When the overvoltage of common-mode input voltage is detected ($V_{aw} > V_{cewo}$)

APPLICATION NOTE

Typical Application Circuit

VIA0050DD is ideally suited to shunt resistor-based current sensing in high voltage applications such as frequency inverters. The typical application circuit is shown in Fig. 25.

The voltage across the shunt resistor R_{sense} is applied to the differential input of VIA0050DD through a RC filter. The differential output of the isolated amplifier is converted to a single-ended analog output with an operational-amplifier-based circuit. Suggest to add > 1 kΩ resistor on the OUT_P and OUT_N pin to prevent output over-current. An analog to digital converter usually receives the analog output and converts to digital signal for controller processing.

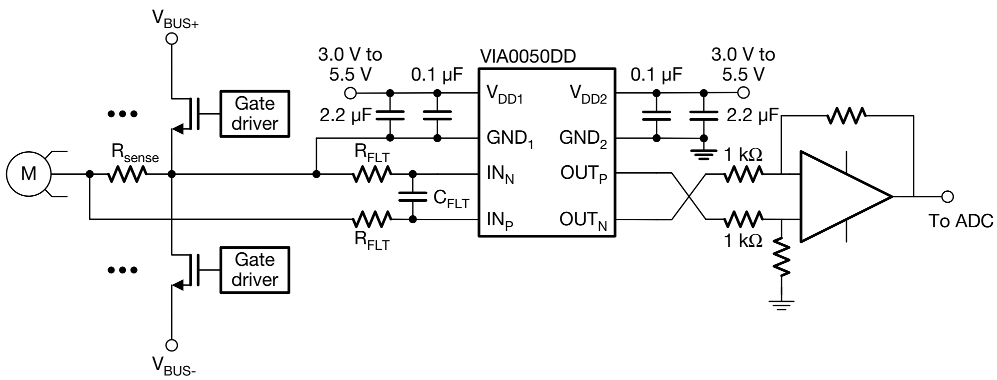


Fig. 25 - Typical Application Circuit in Phase Current Sensing

Shunt Resistor Selection

Choosing a particular shunt resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistor decreases power dissipation, while larger sense resistor can improve measure accuracy by utilizing the full input range of isolated amplifier.

There are two other factors should be considered when selecting the shunt resistor:

- The voltage-drop caused by the rated current range must not exceed the recommended linear input voltage range: $V_{SHUNT} \leq FSR$
- The voltage-drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{clipping}$

PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- VIA0050DD requires a 0.1 µF bypass capacitor between V_{DD1} and GND_1, V_{DD2} and GND_2. The capacitor should be placed as close as possible to the V_{DD} pin. If better filtering is required, an additional 1 µF to 10 µF capacitor may be used.
- Kelvin rules is recommended for the connection between shunt resistor to VIA0050DD. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the IN_P and IN_N inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the VIA0050DD. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

PACKAGE DIMENSIONS (in millimeters)

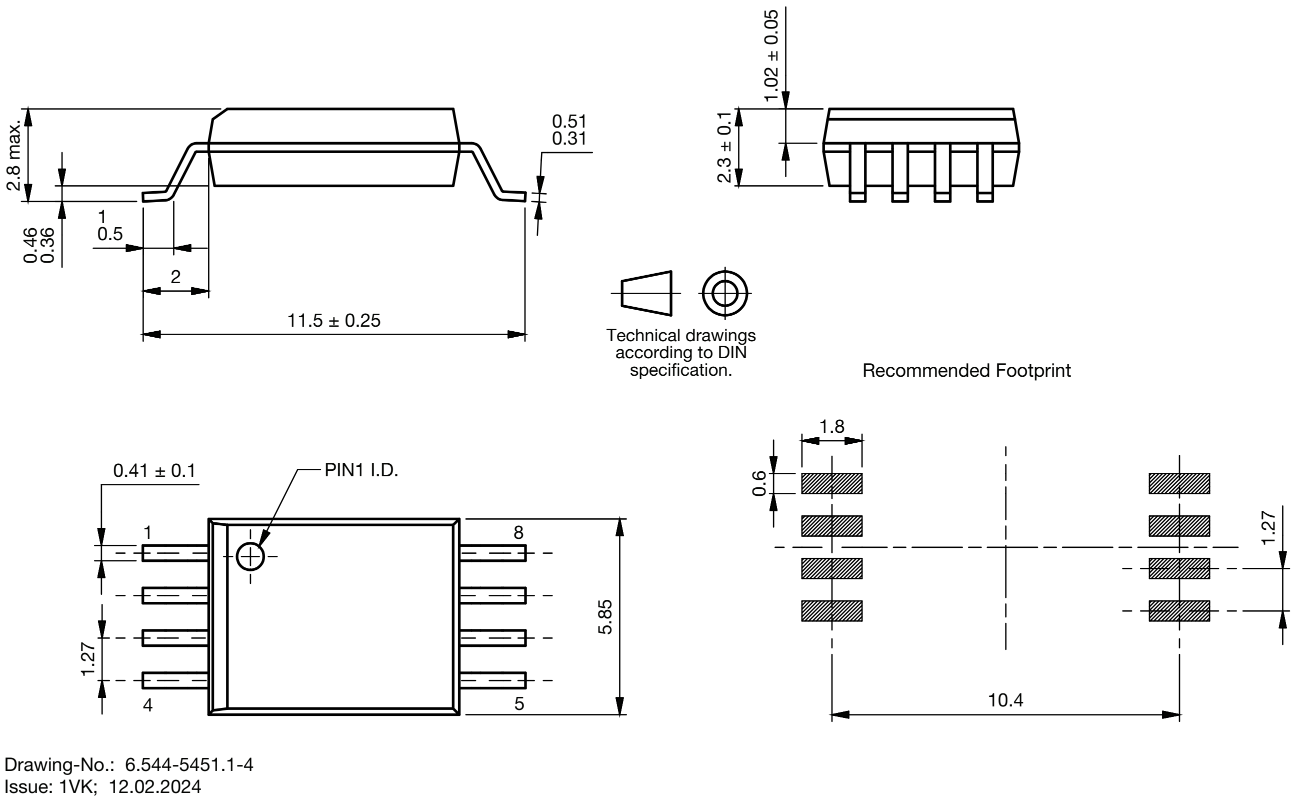


Fig. 26 - SOP-8 (300 mil) Package Shape and Dimensions

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