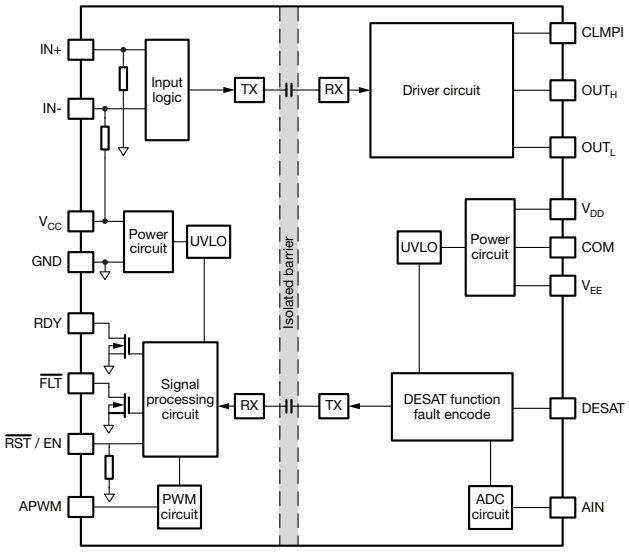
Single Channel Isolated Smart Gate Driver





DESCRIPTION

The VID21750A is 10 A output current smart gate driver. It features active miller clamping, analog monitor feedback for thermal or other sensors, VCE fault and integrated VCE detection, under voltage lockout (UVLO), “soft” IGBT turn-off, isolated open collector fault feedback and fault reset to provide maximum design flexibility and circuit protection.

The VID21750A is intended to drive power IGBTs and Si/SiC MOSFETs, used in motor control inverter applications with ratings up to 1500 V and 150 A.

The very high noise isolation performance is released using capacitive coupling in CMOS technology without noisy and interfering RF signal transmission.

FEATURES

- AEC-Q100 qualified
- 33 V maximum output drive voltage
- 10 A peak source and sink output current
- 4 A internal active miller clamp
- 150 kV/µs minimum CMTI
- 400 mA soft turn off current
- 130 ns (maximum) propagation delay
- 25 ns (maximum) pulse width distortion
- 200 ns response time fast DESAT protection
- Isolated analog sensor with PWM output
- Fault report function
- Fault reset from $\overline{\text{RST}}$/EN
- Fast enable / disable response on $\overline{\text{RST}}$/EN
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

Pb-free

e3

RoHS COMPLIANT

HALOGEN FREE GREEN (5-2008)

AGENCY APPROVALS

- UL1577 (pending)
- CQC CQC11-471543-2012, GB4943.1-2022 (pending)
- DIN EN 60747-17 (VDE 0884-17) (pending)
- AEC-Q100 (pending)

APPLICATIONS

- Traction inverter for EVs
- Industrial inverters and uninterruptible power supply
- On-board charger and DC/DC converter for HEV / EVs
- AC and brushless DC motor drives
- Isolated IGBT / power MOSFET gate driver

DEVICE INFORMATION			
PART NUMBER	**AIN OUTPUT**	**DEAD TIME**	**PACKAGE**
VID21750AADT	Yes	Yes	SOIC-16, wide body
VID21750AAT		No	

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ABSOLUTE MAXIMUM RATINGS (over operating ambient temperature range (unless otherwise noted))				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUE**	**UNIT**
Input supply voltage	V_{CC}	V_{CC} to GND	-0.3 to 7	V
Output positive supply voltage	V_{DD}	V_{DD} to COM	-0.3 to 36	V
Output negative supply voltage	V_{EE}	V_{EE} to COM	-17.5 to 0.3	V
Output positive to negative supply voltage	$V_{max.}$	V_{DD} to V_{EE}	-0.3 to 36	V
Logic input voltage	IN+	Reference to GND	-0.3 to V_{CC}	V
	IN-			
	$\overline{RST}$/EN			
Analog input voltage	DESAT	Reference to COM	-0.3 to V_{DD} + 0.3	V
	AIN		-0.3 to 5	
Gate driver pull up output	OUT_H		V_{EE} - 0.3 to V_{DD}	V
Gate driver pull down output	OUT_L			
Active Miller clamp output	CLMPI			
Power good signal output	RDY	Reference to GND	-0.3 to V_{CC}	V
Fault alarm output	$\overline{FLT}$			
Isolated analog sensing PWM output	APWM			
$\overline{FLT}$ input current	$I_{\overline{FLT}}$		0 to 20	mA
$\overline{RDY}$ input current	I_{RDY}			
APWM pin output current	I_{APWM}			
Operating temperature	T_{amb}		-40 to +125	°C
Junction temperature	T_j		-40 to +150	°C
Storage temperature	T_{stg}		-65 to +150	°C
Maximum power dissipation (both sides)	P_{IO}	V_{CC} = 5 V, V_{DD} to COM = 20 V, COM to V_{EE} = 5 V, IN+ = 5 V, IN- = 0 V, 150 kHz, 50 % duty cycle for 10 nF load, T_{amb} = 25 °C	990	mW
Maximum power dissipation by transmitter side	P_{in}		20	
Maximum power dissipation by receiver side	P_{out}		970	

Note

- AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI / ESDA / JEDEC® JS-001 specification

THERMAL CHARACTERISTICS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUE**	**UNIT**
Junction to ambient thermal resistance	$R_{\theta JA}$		70.3	°C/W
Junction to case thermal resistance	$R_{\theta JC}$		28.5	°C/W

ESD CHARACTERISTICS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUE**	**UNIT**
Electrostatic discharge	V_{ESD}	Human-body model (HBM) per AEC Q100-002 (1)	± 3000	V
Electrostatic discharge		Charged-device model (CDM) per AEC Q100-011	± 2000	

Note

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI / ESDA / JEDEC® JS-001 specification

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FUNCTIONAL BLOCK DIAGRAM

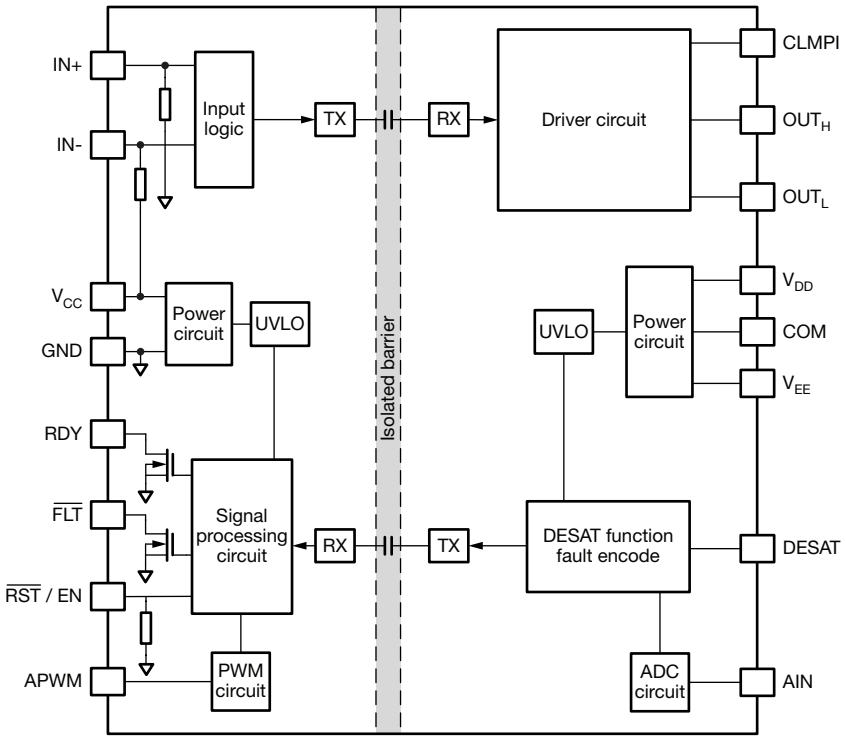


Fig. 1 - VID21750A Block Diagram

RECOMMENDED OPERATING CONDITIONS (over operating ambient temperature range (unless otherwise noted))					
PARAMETER		**SYMBOL**	**MIN.**	**MAX.**	**UNIT**
Input power supply voltage		V_{CC}	3.0	5.5	V
Output positive power supply voltage		V_{DD}	13	33	V
Output positive to negative supply voltage		$V_{max.}$	-	33	V
IN+, IN-, $\overline{RST}$/EN	Logic high input voltage		0.7 x V_{CC}	V_{CC}	V
	Logic low input voltage		0	0.3 x V_{CC}	V
Analog sensing input		A_{IN}	0.5	4.5	V
Enable and shutdown time		$t_{\overline{RST}/EN}$	800	-	ns
Ambient temperature		T_{amb}	-40	+125	°C
Junction temperature		T_j	-40	+150	°C

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PIN CONFIGURATION AND DESCRIPTION

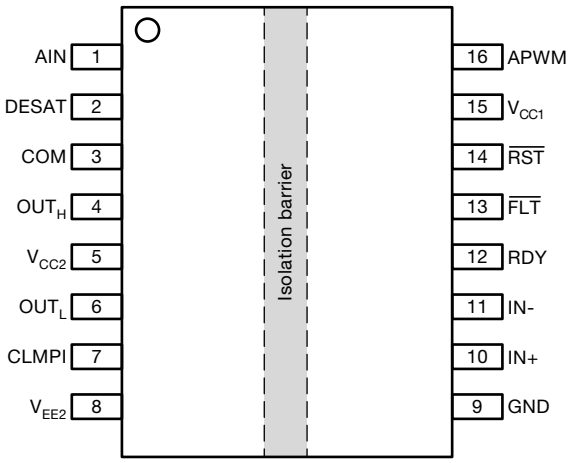


Fig. 2 - VID21750A Package

PIN CONFIGURATION AND DESCRIPTION		
PIN NO.	**SYMBOL**	**FUNCTION**
1	A_{IN}	Isolated analog sensing input; connect a a small capacitor in parallel to COM for a better noise immunity; connect to COM if unused
2	DESAT	Desaturation current protection input; connect to COM if unused
3	COM	Output power supply and ground reference; connect to emitter pin for IGBTs and source pin for MOSFETs
4	OUT_H	Gate driver output pull up
5	V_{DD}	Positive output power supply rail for gate drive voltage; bypass with a decoupling capacitor (> 10 µF) to COM close to the pin
6	OUT_L	Gate driver output pull down
7	CLMPI	Internal active miller clamp; connect this pin directly to the gate of the power transistor; leaving floating or tie to V_{EE} if unused
8	V_{EE}	Negative output power supply rail for gate drive voltage; bypass with a decoupling capacitor (> 10 µF) to COM close to the pin
9	GND	Input power supply and logic ground reference
10	IN+	Non-inverting gate driver control input; connect to V_{CC} if unused
11	IN-	Inverting gate driver control input; connect to GND if unused
12	RDY	Power good status signal output for V_{CC} to GND and V_{DD} to COM; it is an open drain configuration and can be paralleled with other signals
13	$\overline{FLT}$	Active low fault alarm signal output upon over current or short circuit; it is an open drain configuration and can be paralleled with other signals
14	$\overline{RST}$/EN	The $\overline{RST}$/EN signal input serves two purposes: 1) Enable / shutdown of the output side 2) Resets the DESAT condition signaled on $\overline{FLT}$ pin if terminal $\overline{RST}$/EN is set to logic low for more than 1 ms
15	V_{CC}	Input power supply; bypass with a decoupling capacitor (> 1 µF) to GND close to the pin
16	APWM	Isolated analog sensing PWM output; leave floating if unused

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SAFETY AND INSULATION RATINGS				
PARAMETER	**TEST CONDITION**	**SYMBOL**	**VALUE**	**UNIT**
Climatic classification			40 / 125 / 21	
Comparative tracking index	DIN IEC 112 / VDE 0303 Part 1	CTI	≥ 600	V
Maximum rated withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 1 min (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100 % production test)	V_{ISO}	5700	V_{RMS}
Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 1 min (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100 % production test)	V_{IOTM}	8060	V_{peak}
Maximum repetitive isolation voltage	AC voltage (bipolar)	V_{IORM}	2121	V_{peak}
Maximum surge isolation voltage	Test method per IEC 602368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	V_{IOSM}	6250	V_{peak}
Maximum working isolation voltage	AC voltage (sine wave) time dependent dielectric breakdown (TDDB) test	V_{IOWM}	1500	V_{RMS}
	DC voltage		2121	V_{DC}
Isolation resistance	T_{amb} = 25 °C, V_{IO} = 500 V	R_{IO}	$> 10^{12}$	Ω
	100 °C ≤ T_{amb} ≤ 125 °C, V_{IO} = 500 V	R_{IO}	$> 10^{11}$	Ω
	$T_{amb} = T_S$ = 150 °C	R_{IO}	$> 10^{9}$	Ω
Safety input, output, or total power	$R_{\theta JA}$ = 70.3 °C/W, V_{DD} = 20 V, V_{EE} = -5 V, T_J = 150 °C, T_{amb} = 25 °C	P_S	1200	mW
Safety input, output, or supply current	$R_{\theta JA}$ = 70.3 °C/W, V_{DD} = 15 V, V_{EE} = -5 V, T_J = 150 °C, T_{amb} = 25 °C	I_S	60	mA
	$R_{\theta JA}$ = 70.3 °C/W, V_{DD} = 20 V, V_{EE} = -5 V, T_J = 150 °C, T_{amb} = 25 °C		47	mA
Safety temperature (1)		T_S	150	°C
Creepage distance	SOIC-16, wide body		≥ 8	mm
Clearance distance			≥ 8	mm
Material group	Material group (DIN VDE 0110, 1/89)		I	
Overvoltage category per IEC 60664–1	Rated mains voltage. 600 V_{RMS}		I to IV	
	Rated mains voltage. 1000 V_{RMS}		I to III	
Pollution degree per DIN VDE 0110, table 1			2	
Isolation capacitance	V_{IO} = 0.4 x sin(2πft), f = 1 MHz	C_{IO}	1	pF
Apparent charge	Method a: after I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$ = 2545 V_{peak}, t_m = 10 s	q_{pd}	≤ 5	pC
	Method a: after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$ = 3394 V_{peak}, t_m = 10 s		≤ 5	
	Method b1: at routine test (100 % production) and preconditioning (type test) $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$ = 3977 V_{peak}, t_m = 1 s		≤ 5	

Note

- $T_{J\,(max.)} = T_S = T_{amb} + R_{\theta JA} \times P_S$, where $T_{J\,(max.)}$ is the maximum allowed junction temperature; $P_S = I_S \times V_I$, where V_I is the maximum supply voltage

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ELECTRICAL CHARACTERISTICS

(unless otherwise noted, all typ. values at T_{amb} = 25 °C, V_{CC} = 3.3 V or 5 V, 1 µF capacitor from V_{CC} to GND, V_{DD} to COM = 20 V, 18 V, or 15 V, COM to V_{EE} = 0 V, 5 V, 8 V, or 15 V, C_L = 100 pF, T_j = -40 °C to +150 °C)

PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
V_{CC} CHARACTERISTICS						
V_{CC} quiescent current	OUT_H = high, f_S = 0 Hz, AIN = 2 V	I_{VCCQ}	-	2.2	-	mA
	OUT_L = low, f_S = 0 Hz, AIN = 2 V		-	1.7	-	mA
V_{CC} UVLO rising threshold		V_{VCC_ON}	2.5	2.7	2.9	V
V_{CC} UVLO falling threshold		V_{VCC_OFF}	2.3	2.5	2.7	V
V_{CC} UVLO hysteresis		V_{VCC_HYS}	-	0.2	-	V
V_{CC} UVLO deglitch time		t_{VCCFIL}	0.9	1.273	2.0	µs
V_{CC} UVLO on delay to output logic high	IN+ = V_{CC}, IN- = GND	$t_{VCC+ to OUT}$	12	18	30	µs
V_{CC} UVLO on delay to output logic low		$t_{VCC- to OUT}$	1.0	1.373	2.1	µs
V_{CC} UVLO on delay to RDY logic high	$\overline{RST}$/EN = V_{CC}	$t_{VCC+ to RDY}$	12	18	30	µs
V_{CC} UVLO on delay to RDY logic low		$t_{VCC- to RDY}$	0.8	1.3	2.0	µs
V_{DD} CHARACTERISTICS						
V_{DD} quiescent current	OUT_H = high, f_S = 0 Hz, AIN = 2 V	I_{VDDQ}	-	3.1	-	mA
	OUT_L = low, f_S = 0 Hz, AIN = 2 V		-	2.1	-	mA
V_{DD} UVLO rising threshold		V_{VDD_ON}	11.2	12	12.8	V
V_{DD} UVLO falling threshold		V_{VDD_OFF}	9.9	10.7	11.5	V
V_{DD} UVLO hysteresis		V_{VDD_HYS}	-	1.3	-	V
V_{DD} UVLO deglitch time		t_{VDDFIL}	1.3	1.8	2.4	µs
V_{DD} UVLO on delay to output logic high	IN+ = V_{CC}, IN- = GND	$t_{VDD+_to_OUT}$	28	36	54	µs
V_{DD} UVLO on delay to output logic low		$t_{VDD-_to_OUT}$	1.4	1.8	2.5	µs
V_{DD} UVLO on delay to RDY logic high	$\overline{RST}$/EN = $\overline{FLT}$ = high	$t_{VDD+_to_RDY}$	25	36	45	µs
V_{DD} UVLO on delay to RDY logic low		$t_{VDD-_to_RDY}$	8	13	23	µs
INPUT PIN CHARACTERISTIC						
Input high threshold		V_{INH}	-	0.5 x V_{CC}	0.7 x V_{CC}	V
Input low threshold		V_{INL}	0.3 x V_{CC}	0.35 x V_{CC}	-	V
Input threshold hysteresis		V_{INHYS}	-	0.15 x V_{CC}	-	V
Input high level input leakage current	V_{IN} = V_{CC}	I_{IH}	-	106	-	µA
Input low level input leakage	V_{IN} = GND	I_{IL}	-	-106	-	µA
Input pins pull down resistance		R_{IND}	-	47	-	kΩ
Input pins pull up resistance		R_{INU}	-	47	-	kΩ
IN+, IN-, and $\overline{RST}$/EN deglitch (ON and OFF) filter time		t_{INFIL}	-	40	-	ns
Deglitch filter time to reset $\overline{FLT}$		t_{RSTFIL}	-	650	-	ns
GATE DRIVER STAGE						
Peak source current	C_L = 0.18 µF, f_S = 1 kHz	I_{OUTH}	-	10	-	A
Peak sink current		I_{OUTL}	-	-10	-	A
Output pull-up resistance	I_{OUT} = -0.1 A	R_{OUTH}	-	0.5	-	Ω
Output pull-down resistance	I_{OUT} = 0.1 A	R_{OUTL}	-	0.5	-	Ω
High level output voltage	I_{OUT} = -0.2 A, V_{DD} = 18 V	V_{OUTH}	-	17.9	-	V
Low level output voltage	I_{OUT} = 0.2 A	V_{OUTL}	-	100	-	mV
ACTIVE PULLDOWN						
Output active pull down on OUT, OUT_L	I_{OUTL} or I_{OUT} = 0.1 x I_{OUTL}, V_{DD} = open, V_{EE} = COM	V_{OUTPD}	-	-	2.5	V

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ELECTRICAL CHARACTERISTICS

(unless otherwise noted, all typ. values at T_{amb} = 25 °C, V_{CC} = 3.3 V or 5 V, 1 µF capacitor from V_{CC} to GND, V_{DD} to COM = 20 V, 18 V, or 15 V, COM to V_{EE} = 0 V, 5 V, 8 V, or 15 V, C_L = 100 pF, T_j = -40 °C to +150 °C)

PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
INTERNAL ACTIVE MILLER CLAMP						
Miller clamp threshold voltage	Reference to V_{EE}	V_{CLMPTH}	1.7	2.0	2.3	V
Output low clamp voltage	I_{CLMPI} = 1 A	V_{CLMPI}	-	V_{EE}+ 0.5	-	V
Output low clamp current	V_{CLMPI} = 0 V, VEE = -2.5 V	I_{CLMPI}	-	4	-	A
Miller clamp pull down resistance	I_{CLMPI} = 0.2 A	R_{CLMPI}	-	0.6	-	Ω
Miller clamp ON delay time	C_L = 1.8 nF	t_{DCLMPI}	-	27	50	ns
SHORT CIRCUIT CLAMPING						
V_{OUT} - V_{DD}, V_{OUTH} - V_{DD}	OUT = low, I_{OUTH} = 500 mA, t_{CLP} = 10 µs	$V_{CLP-OUTH}$	-	0.85	1.35	V
V_{OUT} - V_{DD}, V_{OUTL} - V_{DD}	OUT = high, I_{OUTL} = 500 mA, t_{CLP} = 10 µs	$V_{CLP-OUTL}$	-	1.25	2	V
V_{CLMPI} - V_{DD}	OUT = high, I_{CLMPI} = 20 mA, t_{CLP} = 10 µs	$V_{CLP-CLMPI}$		1	-	V
DESAT PROTECTION						
Blanking capacitor charge current	V_{DESAT} = 2.0 V	I_{CHG}	450	500	550	µA
Blanking capacitor discharge current	V_{DESAT} = 6.0 V	I_{DCHG}	10	15	-	mA
Detection threshold		V_{DESAT}	8.5	9.0	9.5	V
Voltage when OUT_L = low, reference to COM		V_{DESATL}	-	-	1	V
Leading edge blank time		$t_{DESATLEB}$	-	200	-	ns
DESAT deglitch filter		$t_{DESATFIL}$	-	150	-	ns
DESAT propagation delay to OUT_L 90 %		$t_{DESATOFF}$	-	200	-	ns
DESAT to $\overline{FLT}$ low delay		$t_{DESATFLT}$	-	440	-	ns
INTERNAL SOFT TURN-OFF						
Soft turn-off current on fault conditions		I_{STO}	250	400	570	mA
ISOLATED TEMPERATURE SENSE AND MONITOR (AIN - APWM)						
Analog sensing voltage range		V_{AIN}	0.5		4.5	V
Internal current source	V_{AIN} = 2.5 V, -40 °C < T_J < 150 °C	I_{AIN}	196	200	204	µA
APWM output frequency	V_{AIN} = 2.5 V	f_{APWM}	380	400	420	kHz
APWM Duty cycle	V_{AIN} = 0.5 V	D_{APWM}	89.3	90	91.4	%
	V_{AIN} = 2.5 V		49.1	50	51.5	%
	V_{AIN} = 4.5 V		7.9	10	11.8	%
FLT AND RDY REPORTING						
V_{DD} UVLO $\overline{RDY}$ low minimum holding time		t_{RDYHLD}	0.55	0.73	1.0	ms
Output mute time on fault	Reset fault through $\overline{RST}$/EN	$t_{FLTMUTE}$	0.55	0.73	1.0	ms
Open drain output on resistance	I_{ODON} = 5 mA	R_{ODON}	-	30	-	Ω
Open drain low output voltage	I_{ODON} = 5 mA	V_{ODL}	-	-	0.3	V
CMTI						
Common-mode transient immunity		CMTI	150	-	-	kV/us

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SWITCHING CHARACTERISTICS
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PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Propagation delay time to high output level		t_{PLH}	60	98	130	ns
Propagation delay time to low output level		t_{PHL}	60	98	130	ns
Pulse width distortion		PWD	-	-	25	ns
Dead time for shoot through protection		t_{dead}	680	816	980	ns
Rise time	C_L = 10 nF	t_r	-	33	-	ns
Fall time	C_L = 10 nF	t_f	-	32	-	ns
Maximum switching frequency		$f_{max.}$	-	-	1	MHz

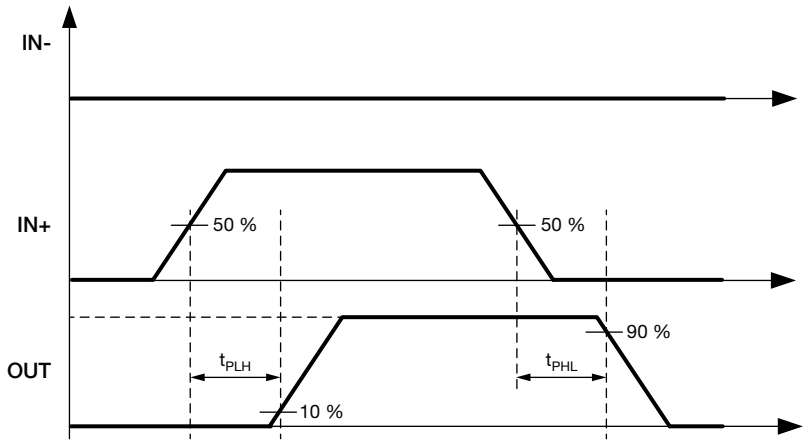


Fig. 3 - Propagation Delay Measurement (non-invertig)

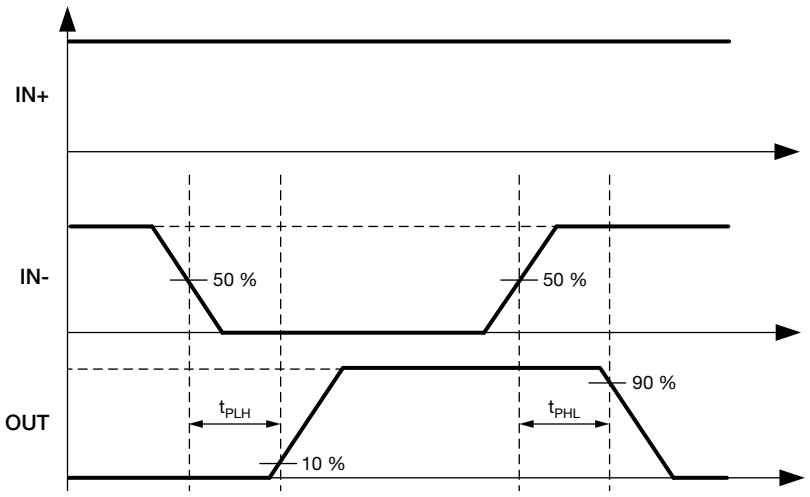


Fig. 4 - Propagation Delay Measurement (inverting)

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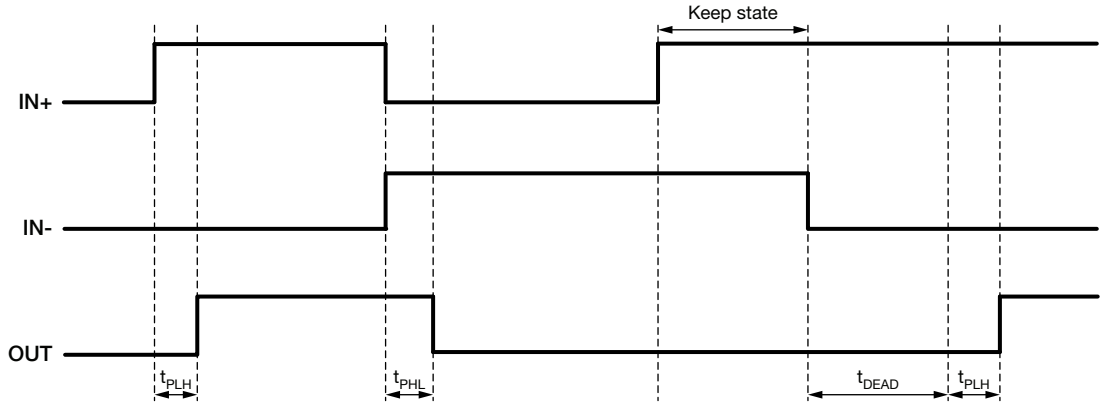


Fig. 5 - Logic Relationship Timing Diagram With Dead Time Setting

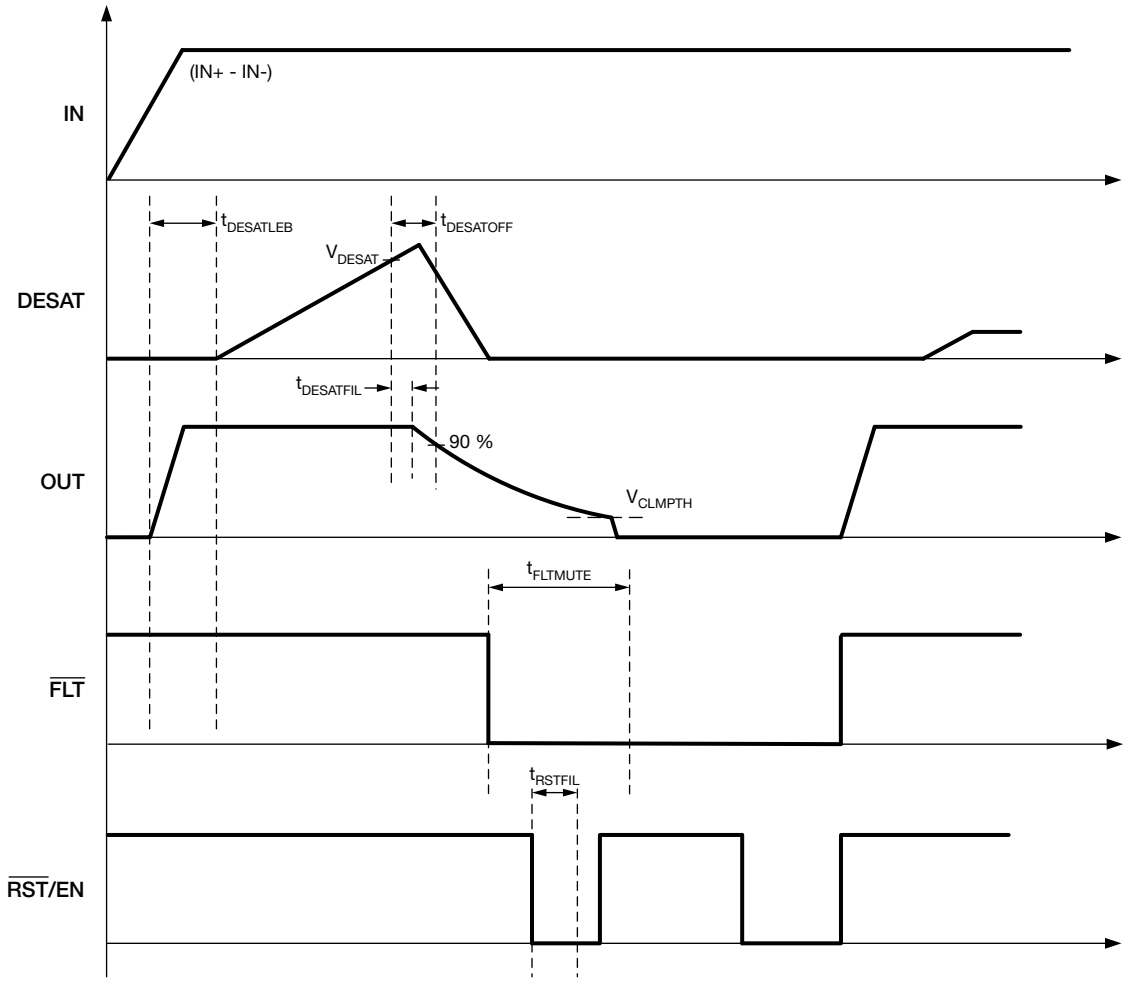


Fig. 6 - DESAT Protection Timing Diagram

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FUNCTION DESCRIPTION

Overview

The VID21750A is a gate driver with specific integrated protection functions. The most important are fault protection, active miller clamp, desaturation detection and soft turn off and analog to PWM transmission.

The output driver can source and sink 10 A of current and has the capability to drive IGBTs with ratings of up to 150 A and 1500 V. Because of the fast switching times, driving SiC transistors and modules is also possible.

The Active Miller clamp function can prevent fault switching in severe working conditions.

With a typical propagation delay of 98 ns, the reaction time between the signal from input (typically a microcontroller or DSP) and the transistor (IGBT, SiC) is very low. The maximum switching frequency can be up to 1 MHz.

The desaturation detection prevent the damage of the power switching transistor due to over current, while a separated and isolated feedback channel provides a fault status feedback signal to the input (microcontroller or DSP).

UVLO function monitors the power supply voltage to avoid the lower gate voltage of the IGBT / SiC transistor.

Additionally, the VID21750A integrates an ADC module, which can convert the input analog signal on the output side to PWM signal on the input side. The ADC module can be used to detect voltage, current, temperature, etc.

A reinforced isolation barrier based on capacitive isolation can support up to 5700 V_{RMS} isolation per UL1577. The high CMTI capability (150 V/ns minimum) guarantees the reliability of the system with fast switching speed. Compared to other isolation technologies, the VID21750A uses a noise and RF free differential signal transmission technology, resulting in less EMI and RFI issues within the application.

Power Supply

The supply voltage (V_{CC}) on the input supports a wide voltage range, covering 3 V to 5.5 V. At the driver output (V_{DD}), the voltage range covers 13 V up to 33 V. Because the input and output sides are isolated, the driver side can also be driven with a negative power supply. This can prevent the power transistors from a false turn on during fast switching conditions. The maximum voltage between COM and V_{EE} can be up to 17.5 V.

Output Stage

The VID21750A has P-channel MOSFET to pull up the OUT_H pin, and two N-channel MOSFETs to pulldown the OUT_L pin. The two N-channel MOSFETs connected to the OUT_L pin have different functions. One MOSFET function as the main turn off, another MOSFET function as the soft turn off MOSFET. The VID21750A has 10 A current source and sink capability because of the lower output impedance.

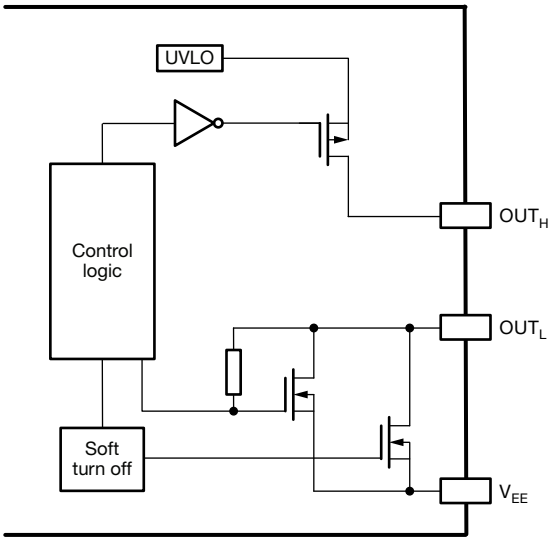


Fig. 7 - Output Stage

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V_{CC} and V_{DD} Undervoltage Lockout (UVLO)

The VID21750A supports an internal UVLO protection on input and driver output side. When the supply voltage is lower than the threshold voltage, the driver output remains “low”. When the supply voltage is too low on driver side, the output driving voltage will be too low to drive the gate and the IGBT may operate in the linear region, where the power loss is high and the IGBT might be damaged. On the one hand, the UVLO protection feature can protect the power device from thermal damage, on the other hand UVLO protection can increase the efficiency of the power system. The UVLO+ threshold voltage is 12.0 V, UVLO- threshold voltage is 10.7 V, and the voltage hysteresis is 1.3 V. The timing diagrams of the UVLO feature of V_{CC} and V_{DD} are shown in Fig. 8 and Fig. 9.

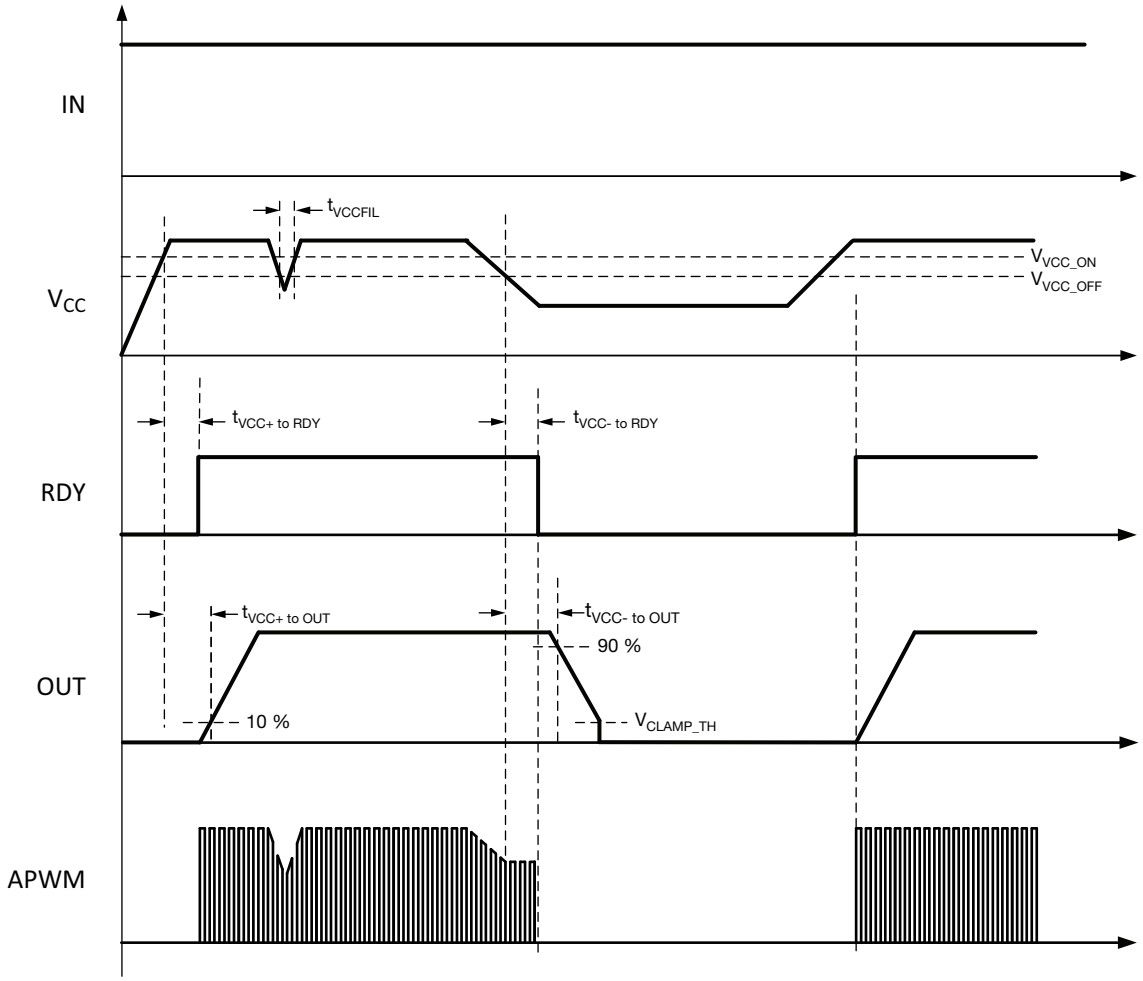


Fig. 8 - V_{CC} UVLO Timing Diagram

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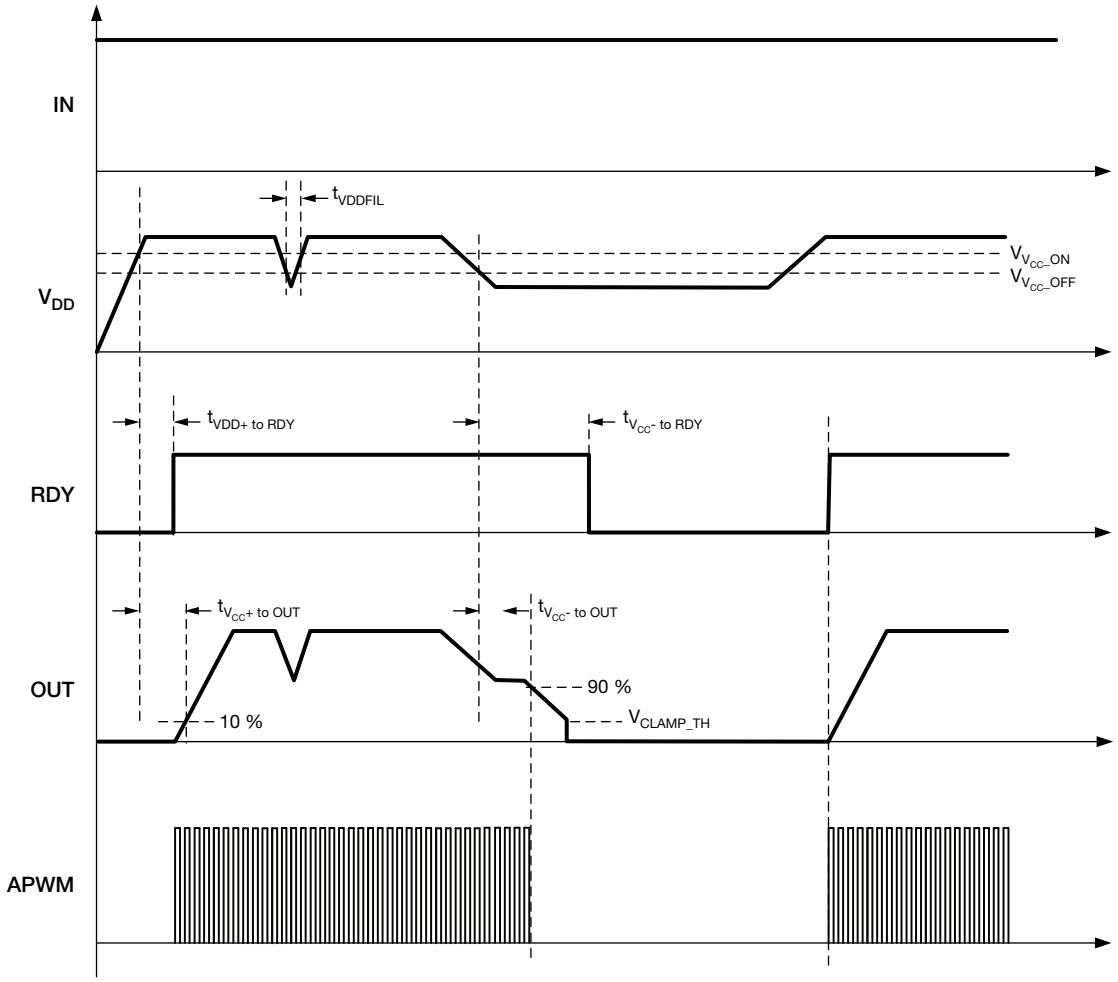


Fig. 9 - V_{DD} UVLO Timing Diagram

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Active Pull-Down

The active pull-down function prevent the output from being undesired turned on. When the V_{DD} is floating, the output will be clamped to V_{EE}.

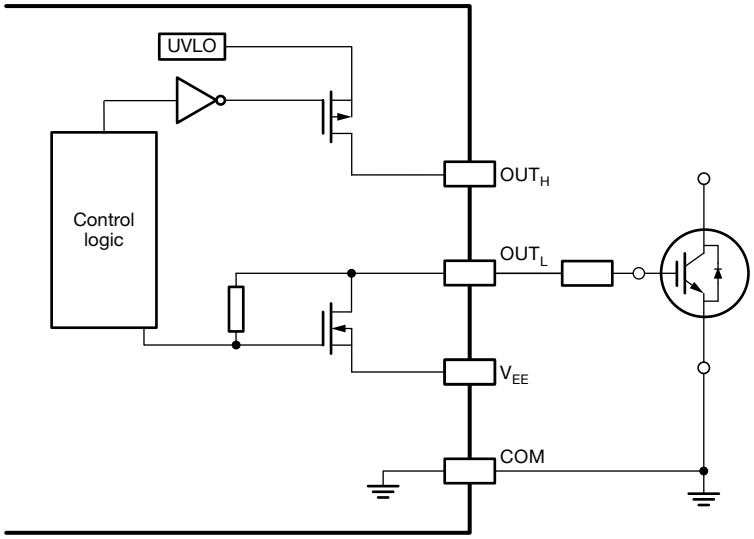


Fig. 10 - Active Pull-Down

Short Circuit Clamping

Under short circuit condition, the voltage drop through the IGBT or MOSFET changes fast, the gate voltage tends to rise because of the miller capacitance. The diode between OUT_H/CLMPI and V_{DD} pins inside the driver clamp this voltage to approximately 0.7 V higher than the supply voltage. The maximum current of 500 mA may be fed back to the supply through this diode. An external Schottky diode may be added if needed.

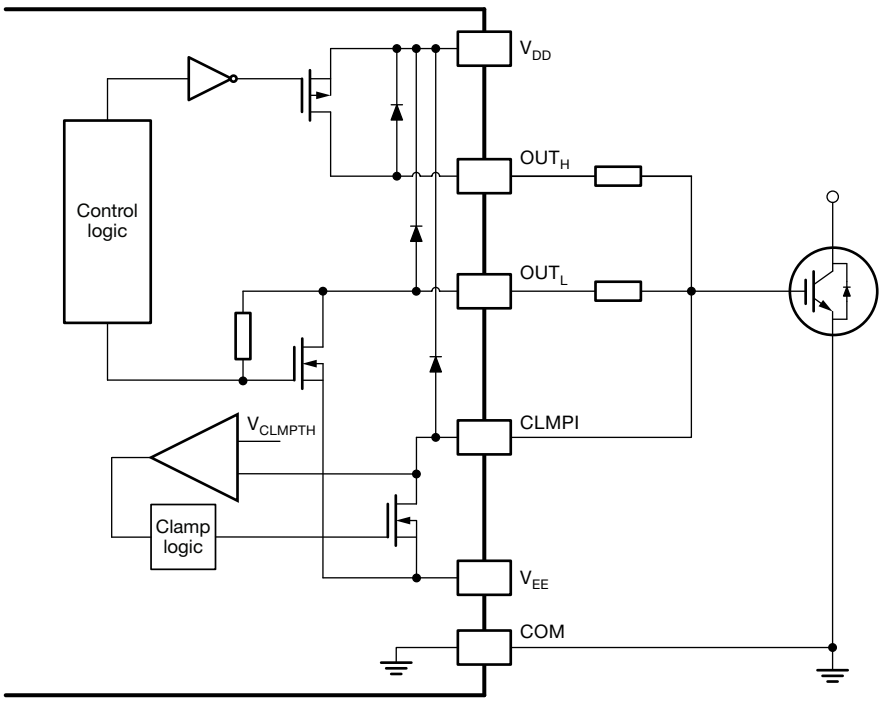


Fig. 11 - Short Circuit Clamping

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Internal Active Miller Clamp

When the driver output is low, the IGBT is switched off. In power systems especially some high power system, the switching noise may cause high dV/dt. The gate voltage may reach the turn on voltage through the miller capacitor. Negative supply voltage can reduce the noise on the gate voltage. During turn-off, the gate voltage is monitored, and the clamp output is activated when gate voltage goes below 2 V (relative to V_{EE}).

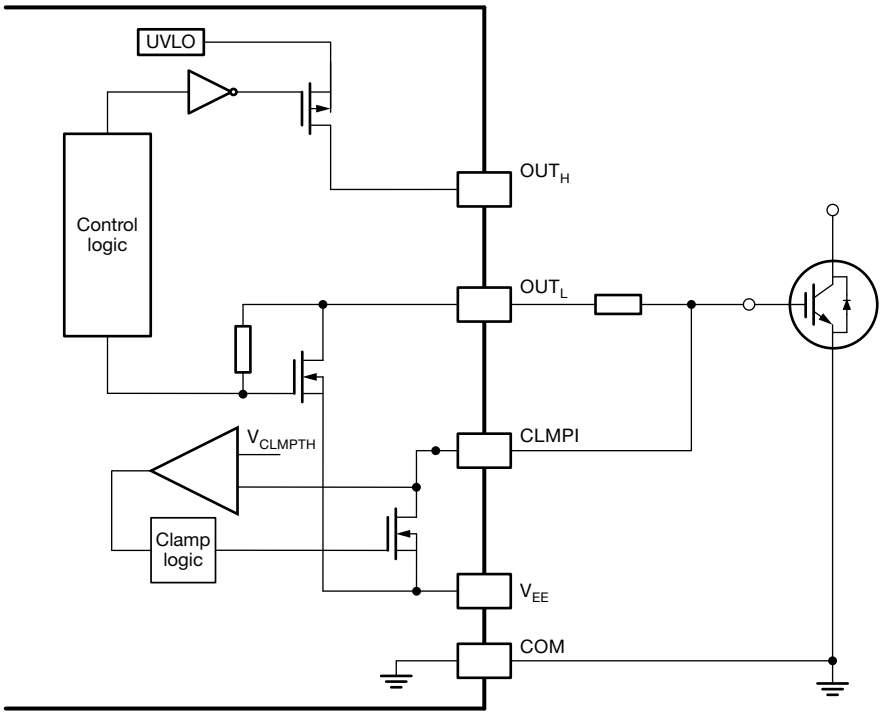


Fig. 12 - Active Miller Clamp

Desaturation (DESAT) Protection

By turning the driver output high, the internal current source of the DESAT pin is activated after a leading blank time. The internal current source is 500 µA, the leading-edge blanking time is 200 ns. During the on state if the over current or short circuit happens the voltage on the DESAT pin will exceed the protection threshold voltage. The DESAT pin has a typical 9 V threshold. By directly measuring the voltage through IGBT, the VID21750A limits the power dissipation in the IGBT. Once the desaturation is detected, the protection circuit will slowly shut down the IGBT.

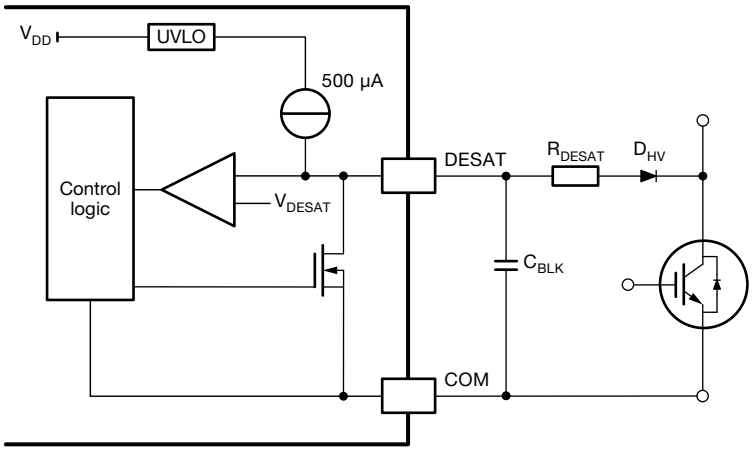


Fig. 13 - DESAT Protection

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Soft Turn-Off

The soft turn-off is triggered when voltage on the DESAT pin exceeds the threshold value. Short circuit or over current may cause the voltage rise. When fault occurs, the external power transistor will turn off. the faster the IGBT turns off the higher di/dt occurs. This may result in the overshoot voltage on the parasitic inductance of the emitter. Therefore, the device should be turned off slowly to avoid overshoot. The turn off time also has an impact on the total power loss in the power devices. Long turn off time may cause the thermal breakdown. There is a balance between the overshoot and large energy dissipation. 400mA soft turn off current is a compromising choice.

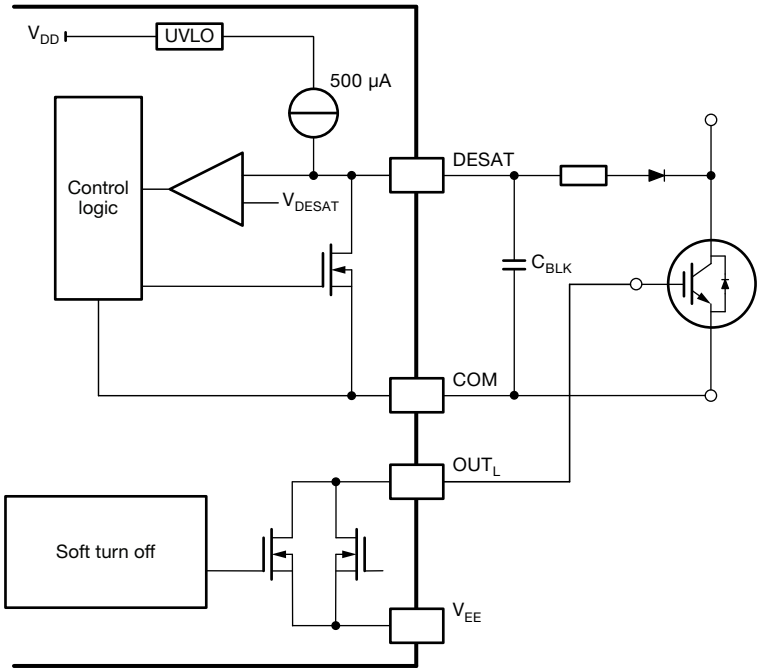


Fig. 14 - Soft Turn-Off

Fault ($\overline{FLT}$, Reset, and Enable ($\overline{RST}$/EN)

When the voltage on the DESAT pin exceeds the threshold voltage the fault is detected. The $\overline{FLT}$ pin is open drain the internal MOSFET connected to the $\overline{FLT}$ pin will be turned on to GND after the fault is detected. The $\overline{FLT}$ pin remains low until a reset signal is received from $\overline{RST}$/EN. The device ignores any reset signal during a fault mute time $t_{FLTMUTE}$.

A 50 kΩ resistor is connected to the $\overline{RST}$/EN pin when this pin is floating the device is disabled. Apply a high level to enable the driver. The pin has two functions:

- To reset the $\overline{FLT}$ pin. To reset, then $\overline{RST}$/EN pin is pulled low: if the pin is set and held in low state for more than t_{RSTFIL} after the mute time $t_{FLTMUTE}$, then the fault signal is reset, and $\overline{FLT}$ is reset back to the high impedance status at the rising edge of the input signal at $\overline{RST}$/EN pin.
- Enable and shutdown the device. If the $\overline{RST}$/EN pin is pulled low for longer than t_{RSTFIL}, the driver will be disabled and OUT_L will be activated to pull down the gate of the IGBT or SiC MOSFET. The pin must be pulled up externally to enable the part, otherwise the device is disabled by default.

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Isolated Analog to PWM Signal Function

The VID21750A contains an isolated analog to PWM signal module. Its function is to convert a voltage signal to a PWM signal. An internal current source of 200 µA is connected to AIN pin to bias an external thermal diode or temperature sensing resistor which allows the isolated temperature sensing, high voltage DC bus voltage sensing, etc. The voltage at the AIN input can be between 0.5 V to 4.5 V. The corresponding duty cycle of the APWM output ranges from 90 % to 10 %. When AIN is floating, the AIN voltage is 5 V and the APWM operates at 400 kHz with approximately 10 % duty cycle. The accuracy of the duty cycle is ± 3 % across temperature without one time calibration. When a resistor divider is used to detect current or voltage, the internal current source I_{AIN} should be considered. Calculate the detected voltage or current through the superposition principle. The duty cycle of the PWM can be represented using equation below.

$$D_{APWM}\,(\%) = -20 \times V_{AIN} + 100 \quad (1)$$

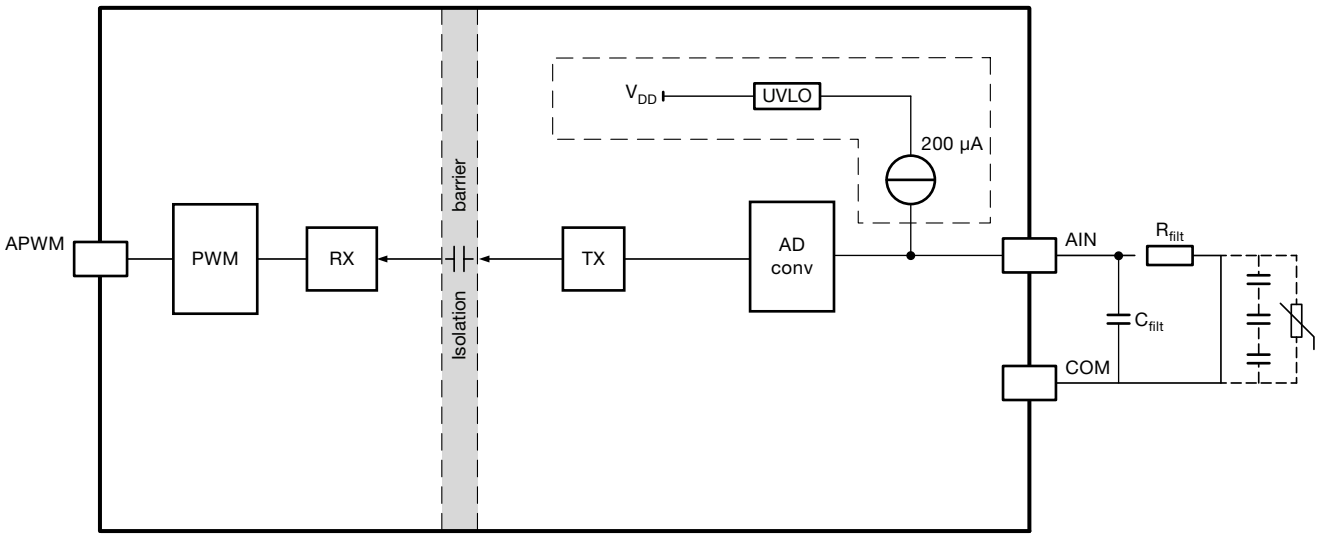


Fig. 15 - Isolated Analog to PWM Signal

Device Functional Modes

DEVICE FUNCTIONAL MODES

INPUT (1)							OUTPUT					
V_{CC}	V_{DD}	V_{EE}	IN+	IN-	$\overline{RST}$/EN	AIN	RDY	$\overline{FLT}$	CLMPI	APWM	OUT (no DT)	OUT (DT)
PU	PD	PU	X	X	X	X	Low	HiZ	Low	Low	Low	Low
PD	PU	PU	X	X	X	X	Low	HiZ	Low	Low	Low	Low
PU	PU	PU	X	X	Low	X	HiZ	HiZ	Low	PWM	Low	Low
PU	Open	PU	X	X	X	X	Low	HiZ	Low	Low	Low	Low
PU	PU	Open	X	X	X	X	Low	HiZ	Low	Low	Low	Low
PU	PU	PU	Low	X	High	X	HiZ	HiZ	Low	PWM	Low	Low
PU	PU	PU	X	High	High	X	HiZ	HiZ	Low	PWM	Low	Low
PU	PU	PU	High	High	High	X	HiZ	HiZ	Low	PWM	Low	Hold
PU	PU	PU	High	Low	High	X	HiZ	HiZ	HiZ	PWM	High	High

Note

(1) PU: power up
PD: power down
X: irrelevant
HiZ: high impedance

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PACKAGE DIMENSIONS (in millimeters)

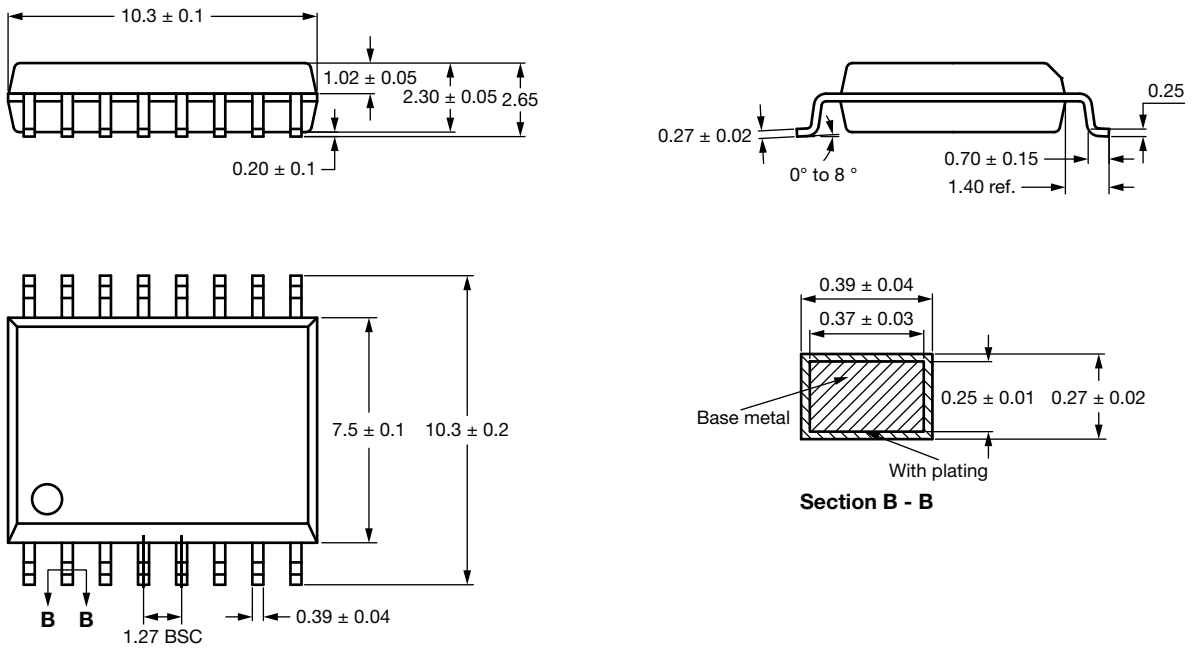


Fig. 16 - 16-Lead Wide Body Outline Package (SOIC-16, wide body)

FOOTPRINT (in millimeters)

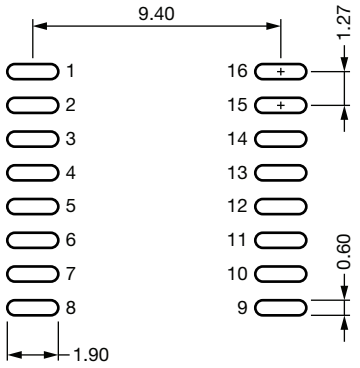


Fig. 17 - 16-Lead Wide Body SOIC (SOIC-16, wide body) Land Pattern

PACKAGE MARKING (example)

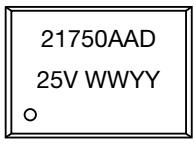


Fig. 18 - Example of VID21750AADT

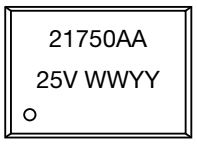


Fig. 19 - Example of VID21750AAT

Notes

- "WWYY" is the date code marking (Y = year code, WW = week code)
- Tape and reel suffix (T) is not part of the package marking

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PACKING INFORMATION

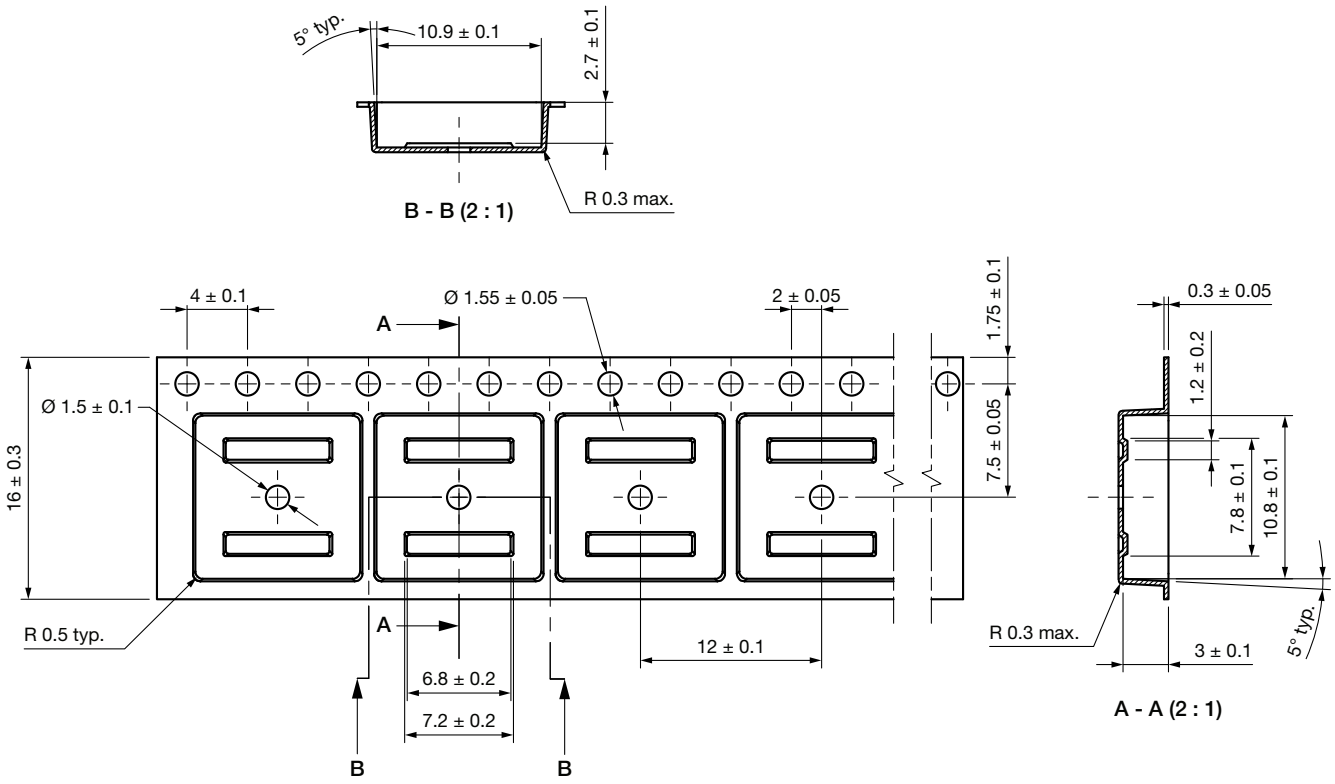


Fig. 20 - 16-Lead Wide Body Outline Package (1500 pieces on reel)

HANDLING AND STORAGE CONDITIONS

Floor life: unlimited

Conditions: T_{amb} < 30 °C, RH < 85 %

Moisture sensitivity level rating: Level-2-260C-1 year, according to the JEDEC industry standard classifications, and peak solder temperature

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REVISION HISTORY		
DATASHEET VERSION	**REVISION DATE**	**CHANGE**
1.0	19-Oct-2026	Initial datasheet release

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