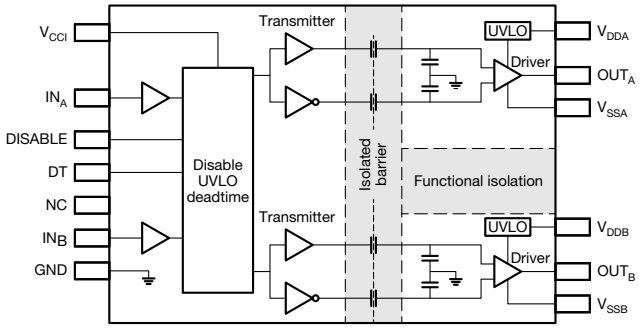
# Dual Channel Isolated Smart Gate Driver






## AGENCY APPROVALS

- UL1577 (pending)
- DIN EN IEC 60747-17 VDE 0884-17) (pending)
- CQC GB4943.1-2022 (pending)
- CSA IEC 60950-1, IEC 62368-1, IEC 61010-1, and IEC 60601-1 end equipment standards (pending)
- AEC-Q100 (pending)

## DESCRIPTION

The VID21540A series are isolated dual-channel gate driver and are suitable for gate drive of standard silicon MOSFETs, IGBTs, and SiC MOSFETs. The peak drive current is 5 A sourcing and 7 A sinking. The operating voltage between primary and secondary side can be up to 1500 $V_{DC}$.

Every driver can be configured as two low side drivers or two high side drivers, or work as a half-bridge driver with programmable dead time to avoid overlapping currents.

The disable function enables shutting down both outputs simultaneously to protect the transistors.

The switching frequency can be up to 5 MHz. And with 125 kV/µs, the VID21540A is well immune against common mode transients.

The very high noise isolation performance is released using capacitive coupling in CMOS technology without noisy and interfering RF signal transmission.

## FEATURES

AUTOMOTIVE GRADE

Pb-free

e3

RoHS COMPLIANT

HALOGEN FREE GREEN (5-2008)

- AEC-Q100 qualified
- Flexible configuration as dual low side/ dual high side or as half bridge driver
- 5700 $V_{ISO}$ high isolation SOIC-14 wide body package
- High isolation distance between channels on output
- 5 A (peak) source, 7 A (peak) sink output
- 39 ns (typ.) propagation delay
- 5 ns (max.) pulse width distortion
- 125 kV/µs common-mode transient immunity
- Operating temperature range: -40 °C to +125 °C
- Isolation barrier life > 40 years
- Digital TTL and CMOS compatible inputs
- Up to 40 $V_{DD}$ output driver supply voltage
- Programmable overlap and dead time
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

## APPLICATIONS

- Motor drives and solar inverters
- HEV and BEV battery chargers
- Uninterruptible power supply (UPS)
- Inverter drives in white goods and aircons
- Isolated converters in high performance DC/DC and AC/DC power supplies



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## ORDERING INFORMATION

| V | I | D | 2 | 1 | 5 | 4 | 0 | A | A | T |
|---|---|---|---|---|---|---|---|---|---|---|
| PART NUMBER | | | | | | | | | UVLO OPTION | TAPE AND REEL |

## DEVICE INFORMATION

| PART NUMBER | UVLO VOLTAGE (V) | PACKAGE |
|---|---|---|
| VID21540AAT | 6.0 | SOIC-14, wide body |
| VID21540ABT | 9.2 | SOIC-14, wide body |
| VID21540ACT | 13.7 | SOIC-14, wide body |
| VID21540ADT | 18.0 | SOIC-14, wide body |

## ABSOLUTE MAXIMUM RATINGS (over operating ambient temperature range (unless otherwise noted))

| PARAMETER | SYMBOL | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| Input supply voltage | $V_{CCI}$ | $V_{CCI}$ to GND | -0.3 to 7 | V |
| Driver bias supply | $V_{DDA}$ | $V_{DDA}$ to $V_{SSA}$ | -0.3 to 40 | V |
| | $V_{DDB}$ | $V_{DDB}$ to $V_{SSB}$ | -0.3 to 40 | V |
| Input signal voltage | $IN_A$ | $IN_A$ to GND | -0.3 to $V_{CCI}$ + 0.3 | V |
| | $IN_B$ | $IN_B$ to GND | -0.3 to $V_{CCI}$ + 0.3 | V |
| | DIS | DIS to GND | -0.3 to $V_{CCI}$ + 0.3 | V |
| | DT | DT to GND | -0.3 to $V_{CCI}$ + 0.3 | V |
| | $IN_A$ | Transient for 50 ns | -5 to $V_{CCI}$ + 0.3 | V |
| | $IN_B$ | Transient for 50 ns | -5 to $V_{CCI}$ + 0.3 | V |
| Output signal voltage | $OUT_A$ | $OUT_A$ to $V_{SSA}$ | -0.3 to $V_{DDA}$ + 0.3 | V |
| | $OUT_B$ | $OUT_B$ to $V_{SSB}$ | -0.3 to $V_{DDB}$ + 0.3 | V |
| | $OUT_A$ | $OUT_A$ to $V_{SSA}$, transient for 200 ns | -2 to $V_{DDA}$ + 0.3 | V |
| | $OUT_B$ | $OUT_B$ to $V_{SSB}$, transient for 200 ns | -2 to $V_{DDB}$ + 0.3 | V |
| | $OUT_A$ | $OUT_A$ to $V_{SSA}$, transient for 10 ns | -20 to $V_{DDA}$ + 0.3 | V |
| | $OUT_B$ | $OUT_B$ to $V_{SSB}$, transient for 10 ns | -20 to $V_{DDB}$ + 0.3 | V |
| Channel to channel voltage | $V_{SSA}$ | $V_{SSA}$ to $V_{SSB}$ | -1500 to 1500 | V |
| | $V_{SSB}$ | $V_{SSB}$ to $V_{SSA}$ | -1500 to 1500 | V |
| Operating temperature | $T_{amb}$ | | -40 to +125 | °C |
| Junction temperature | $T_J$ | | -40 to +150 | °C |
| Storage temperature | $T_{stg}$ | | -65 to +150 | °C |
| Power dissipation (coupler) | $P_{IO}$ | $V_{CCI}$ = 3.3 V, $V_{DDA}$ = 12 V, $V_{DDB}$ = 12 V, $IN_A$ = 3.3 V, $IN_B$ = 3.3 V, f = 2 MHz, 50 % duty cycle, square wave, 1 nF load capacitance | 0.77 | W |
| Power dissipation by transmitter side | $P_{in}$ | | 0.01 | W |
| Power dissipation by each driver side | $P_{out}$ | | 0.38 | W |

**Note**

- Stresses in excess of the absolute maximum ratings can cause permanent damage to the device; functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document; exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability

## THERMAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| Junction to ambient thermal resistance | $R_{\theta JA}$ | | 100 | °C/W |
| Junction to case (top) thermal resistance | $R_{JC\ (top)}$ | | 32.7 | °C/W |
| Junction to top characterization parameter | $\Psi_{JT}$ | | 27.3 | °C/W |
| Junction to case thermal resistance | $\Psi_{JB}$ | | 39.5 | °C/W |


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| ESD CHARACTERISTICS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **VALUE** | **UNIT** |
| Electrostatic discharge | $V_{ESD}$ | Human-body model (HBM), per AEC Q100-002 | ± 4000 | V |
| Electrostatic discharge | | Charged-device model (CDM), per AEC Q100-011 | ± 2000 | |

## FUNCTIONAL BLOCK DIAGRAM

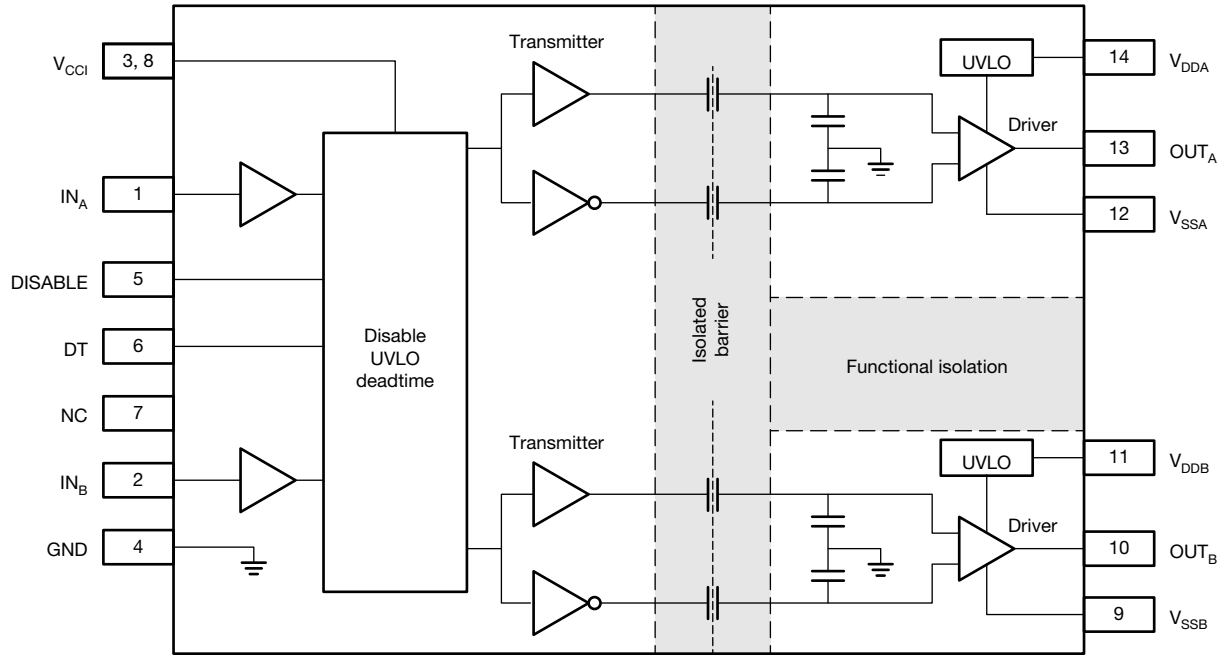



Fig. 1 - VID21540A Block Diagram

| RECOMMENDED OPERATING CONDITIONS (over operating ambient temperature range (unless otherwise noted)) | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **MIN.** | **MAX.** | **UNIT** |
| Input power supply voltage | $V_{CCI}$ | 3 | 5.5 | V |
| Driver output bias supply (VID21540AAT) | $V_{DDA}$ to $V_{SSA}$ | 6 | 36 | V |
| | $V_{DDB}$ to $V_{SSB}$ | 6 | 36 | V |
| Driver output bias supply (VID21540ABT) | $V_{DDA}$ to $V_{SSA}$ | 9.2 | 36 | V |
| | $V_{DDB}$ to $V_{SSB}$ | 9.2 | 36 | V |
| Driver output bias supply (VID21540ACT) | $V_{DDA}$ to $V_{SSA}$ | 13.7 | 36 | V |
| | $V_{DDB}$ to $V_{SSB}$ | 13.7 | 36 | V |
| Driver output bias supply (VID21540ADT) | $V_{DDA}$ to $V_{SSA}$ | 18 | 36 | V |
| | $V_{DDB}$ to $V_{SSB}$ | 18 | 36 | V |
| Logic high input voltage | $IN_A$ to GND | 0 | $V_{CCI}$ | V |
| | $IN_B$ to GND | | | |
| | DISABLE to GND | | | |
| Driver output voltage | $OUT_A$ to $V_{SSA}$ | 0 | $V_{DDA}$ | V |
| | $OUT_B$ to $V_{SSB}$ | 0 | $V_{DDB}$ | V |
| Ambient temperature | $T_{amb}$ | -40 | 125 | °C |


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## PIN CONFIGURATION AND DESCRIPTION

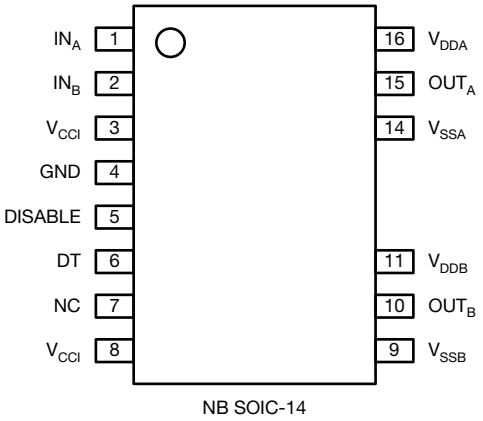



Fig. 2 - VID21540A Package

| PIN CONFIGURATION AND DESCRIPTION | | |
|---|---|---|
| **PIN NO.** | **SYMBOL** | **FUNCTION** |
| 1 | $IN_A$ | Input signal for channel A. $IN_A$ input has a TTL / CMOS compatible input threshold; this pin is pulled to logic low internally if left open; connect to ground if not used to achieve better noise immunity |
| 2 | $IN_B$ | Input signal for channel B. $IN_B$ input has a TTL / CMOS compatible input threshold; this pin is pulled logic low internally if left open; connect to ground if not used to achieve better noise immunity |
| 3, 8 | $V_{CCI}$ | Primary-side supply voltage; bypass with a low ESR / ESL capacitor to GND close to the pin |
| 4 | GND | Primary-side ground reference; all signals at the primary side are referenced to this ground potential |
| 5 | DISABLE | Disables both driver outputs if pulled to logic high and enables both driver outputs if pulled to logic low or left open; this pin is pulled to logic low internally if left open; connect to ground if not used to achieve better noise immunity; when connecting to a microcontroller, bypass with a low ESR / ESL capacitance (~ 1 nF) to ground |
| 6 | DT | Programmable dead time function; tying DT to $V_{CCI}$ allows the outputs to overlap; leaving DT open sets, the dead time to < 15 ns; placing a 50 Ω to 200 kΩ resistor ($R_{DT}$) between DT and GND adjusts dead time according to: DT (in ns) ~10 × $R_{DT}$ (in kΩ) |
| 7 | NC | No internal connection |
| 9 | $V_{SSB}$ | Ground for secondary-side driver B and reference for secondary side channel B |
| 10 | $OUT_B$ | Output of driver B; connect to the gate of the B channel FET or IGBT |
| 11 | $V_{DDB}$ | Secondary-side power for driver B; bypass with a low ESR / ESL capacitor to $V_{SSB}$ close to the pin |
| 14 | $V_{SSA}$ | Ground for secondary-side driver A and reference for secondary side channel A |
| 15 | $OUT_A$ | Output of driver A; connect to the gate of the A channel FET or IGBT |
| 16 | $V_{DDA}$ | Secondary-side power for driver A; bypass with a low ESR / ESL capacitor to $V_{SSA}$ close to the pin |


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| SAFETY AND INSULATION RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITION** | **SYMBOL** | **VALUE** | **UNIT** |
| Climatic classification | | | 40 / 125 / 21 | |
| Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | CTI | ≥ 600 | V |
| Maximum rated withstanding isolation voltage | $V_{TEST} = V_{ISO}$, t = 1 min (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100 % production test) | $V_{ISO}$ | 5700 | $V_{RMS}$ |
| Maximum transient isolation voltage | $V_{TEST} = V_{IOTM}$, t = 1 min (qualification), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100 % production test) | $V_{IOTM}$ | 8062 | $V_{peak}$ |
| Maximum repetitive isolation voltage | AC voltage (bipolar) | $V_{IORM}$ | 2121 | $V_{peak}$ |
| Maximum working isolation voltage | AC voltage (sine wave) | $V_{IOWM}$ | 1500 | $V_{RMS}$ |
| | DC voltage | | 2121 | $V_{DC}$ |
| Maximum surge isolation voltage | Test method per IEC 62368-1, 1.2/50 µs waveform | $V_{IOSM}$ | 12 800 | $V_{peak}$ |
| Isolation resistance | $V_{IO}$ = 500 V, $T_{amb}$ = 25 °C | $R_{IO}$ | > $10^{12}$ | Ω |
| | $V_{IO}$ = 500 V, 100 °C, ≤ $T_{amb}$ ≤ 125 °C | $R_{IO}$ | > $10^{11}$ | Ω |
| | $V_{IO}$ = 500 V, $T_{amb} = T_S$ = 150 °C | $R_{IO}$ | > $10^{9}$ | Ω |
| Safety output supply current | Driver A, $R_{\theta JA}$ = 100 °C/W, $V_{DDA}$ = 12 V, $T_{amb}$ = 25 °C, $T_J$ = 150 °C | $I_S$ | 50 | mA |
| | Driver B, $R_{\theta JA}$ = 100 °C/W, $V_{DDB}$ = 12 V, $T_{amb}$ = 25 °C, $T_J$ = 150 °C | | 50 | |
| | Driver A, $R_{\theta JA}$ = 100 °C/W, $V_{DDA}$ = 25 V, $T_{amb}$ = 25 °C, $T_J$ = 150 °C | | 24 | |
| | Driver B, $R_{\theta JA}$ = 100 °C/W, $V_{DDB}$ = 25 V, $T_{amb}$ = 25 °C, $T_J$ = 150 °C | | 24 | |
| Safety supply power (total) | $R_{\theta JA}$ = 101 °C/W, $T_{amb}$ = 25 °C, $T_J$ = 150 °C | $P_S$ | 1250 | mW |
| Safety temperature (1) | | $T_S$ | 150 | °C |
| Creepage distance | SOIC-14, wide body | | ≥ 8 | mm |
| Clearance distance | | | ≥ 8 | mm |
| Distance through insulation | Minimum internal gap (internal clearance) of the double insulation (2 × 10.5 µm) | DTI | > 21 | µm |
| Material group | According to IEC 60664-1 | | I | |
| Overvoltage category per IEC 60664-1 | Rated mains voltage ≤ 150 $V_{RMS}$ | | I to IV | |
| | Rated mains voltage ≤ 300 $V_{RMS}$ | | I to IV | |
| | Rated mains voltage ≤ 600 $V_{RMS}$ | | I to IV | |
| | Rated mains voltage ≤ 1000 $V_{RMS}$ | | I to III | |
| Pollution degree | | | 2 | |
| Isolation capacitance | $V_{IO}$ = 0.4 × sin(2 πft), f = 1 MHz | $C_{IO}$ | 1.2 | pF |
| Apparent charge | Method a: after I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, $t_m$ = 10 s | $q_{pd}$ | ≤ 5 | pC |
| | Method a: after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)} = 1.3 \times V_{IORM}$, $t_m$ = 10 s | | ≤ 5 | |
| | Method b1: at routine test (100 % production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, $t_{ini}$ = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM}$, $t_m$ = 1 s | | ≤ 5 | |

**Note**

(1) The maximum safety temperature, $T_S$, has the same value as the maximum junction temperature, $T_J$, specified for the device. The $I_S$ and $P_S$ parameters represent the safety current and safety power respectively. The maximum limits of $I_S$ and $P_S$ should not be exceeded. These limits vary with the ambient temperature, $T_{amb}$. The junction to air thermal resistance, $R_{\theta JA}$, in the thermal information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: $T_{J\,(max.)} = T_S = T_{amb} + R_{\theta JA} \times P_S$, where $T_{J\,(max.)}$ is the maximum allowed junction temperature. $P_S = I_S \times V_I$, where $V_I$ is the maximum input voltage. The junction to air thermal resistance, $R_{\theta JA}$, in the thermal information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: these limits vary with the ambient $T_J = T_{amb} + R_{\theta JA} \times P$, where $T_{J\,(max.)}$ is the maximum allowed junction temperature, and P is the power dissipated in the device


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## ELECTRICAL CHARACTERISTICS

(unless otherwise noted, all typ. values at $T_{amb}$ = 25 °C, $V_{CCI}$ = 3.3 V or 5 V, 0.1 µF capacitor from $V_{CCI}$ to GND, $V_{DDA}$ = $V_{DDB}$ = 12 V, 1 µF capacitor from $V_{DDA}$ to $V_{SSA}$ and $V_{DDB}$ to $V_{SSB}$, $T_{amb}$ = -40 °C to +125 °C)

| PARAMETER | TEST CONDITION | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{CCI}$ quiescent current | $V_{INA}$ = 0 V, $V_{INB}$ = 0 V | $I_{VCCIq}$ | - | 0.9 | 1.8 | mA |
| $I_{VDDA}$ quiescent current | $V_{INA}$ = 0 V | $I_{VDDAq}$ | - | 1.3 | 2 | mA |
| $I_{VDDB}$ quiescent current | $V_{INB}$ = 0 V | $I_{VDDBq}$ | - | 1.3 | 2 | mA |
| $V_{CCI}$ supply current | $V_{INA}$, $V_{INB}$ input signal f = 500 kHz, 50 % duty cycle, each channel load capacitance 100 pF ± 20 %, including the input capacitance of the measuring instrument | $I_{VCCI}$ | - | 1.8 | - | mA |
| Driver A supply current | | $I_{VDDA}$ | - | 3.5 | - | mA |
| Driver B supply current | | $I_{VDDB}$ | - | 3.5 | - | mA |
| $V_{CCI}$ UVLO rising threshold | | $V_{VCCI_ON}$ | 2.55 | 2.75 | 2.95 | V |
| $V_{CCI}$ UVLO falling threshold | | $V_{VCCI_OFF}$ | 2.35 | 2.6 | 2.75 | V |
| UVLO threshold hysteresis | | $V_{VCCI_HYS}$ | - | 0.15 | - | V |
| VID21540AA UVLO rising threshold | 6 V UVLO version | $V_{VDDA_ON}$, $V_{VDDB_ON}$ | 5.2 | 5.6 | 6 | V |
| VID21540AA UVLO falling threshold | | $V_{VDDA_OFF}$, $V_{VDDB_OFF}$ | 4.9 | 5.3 | 5.7 | V |
| VID21540AA UVLO threshold hysteresis | | $V_{VDDA_HYS}$, $V_{VDDB_HYS}$ | - | 0.3 | - | V |
| VID21540AB UVLO rising threshold | 9.2 V UVLO version | $V_{VDDA_ON}$, $V_{VDDB_ON}$ | 8.3 | 8.7 | 9.2 | V |
| VID21540AB UVLO falling threshold | | $V_{VDDA_OFF}$, $V_{VDDB_OFF}$ | 7.8 | 8.2 | 8.7 | V |
| VID21540AB UVLO threshold hysteresis | | $V_{VDDA_HYS}$, $V_{VDDB_HYS}$ | - | 0.5 | - | V |
| VID21540AC UVLO rising threshold | 13.7 V UVLO version | $V_{VDDA_ON}$, $V_{VDDB_ON}$ | 11.9 | 12.8 | 13.7 | V |
| VID21540AC UVLO falling threshold | | $V_{VDDA_OFF}$, $V_{VDDB_OFF}$ | 10.9 | 11.8 | 12.7 | V |
| VID21540AC UVLO threshold hysteresis | | $V_{VDDA_HYS}$, $V_{VDDB_HYS}$ | - | 1 | - | V |
| VID21540AD UVLO rising threshold | 18 V UVLO version | $V_{VDDA_ON}$, $V_{VDDB_ON}$ | 16 | 17 | 18 | V |
| VID21540AD UVLO falling threshold | | $V_{VDDA_OFF}$, $V_{VDDB_OFF}$ | 15 | 16 | 17 | V |
| VID21540AD UVLO threshold hysteresis | | $V_{VDDA_HYS}$, $V_{VDDB_HYS}$ | - | 1 | - | V |
| Input high threshold voltage | | $V_{INAH}$, $V_{INBH}$, $V_{DISH}$ | 1.6 | 1.8 | 2 | V |
| Input low threshold voltage | | $V_{INAL}$, $V_{INBL}$, $V_{DISL}$ | 0.8 | 1 | 1.2 | V |
| Input threshold hysteresis | | $V_{INA_HYS}$, $V_{INB_HYS}$, $V_{DIS_HYS}$ | - | 0.8 | - | V |
| Input pins pull down resistance | | $R_{IND}$ | - | 180 | - | kΩ |
| Peak output source current | $C_{VDD}$ = 10 µF, $C_{LOAD}$ = 0.68 µF, f = 100 Hz, bench test | $I_{OHA+}$, $I_{OHB+}$ | - | 5 | - | A |
| Peak output sink current | | $I_{OLA-}$, $I_{OLB-}$ | - | 7 | - | A |
| Output resistance at high state | $I_{OUT}$ = -10 mA | $R_{OHA}$, $R_{OHB}$ | - | 1 | - | Ω |
| Output resistance at low state | $I_{OUT}$ = -10 mA, $T_{amb}$ = 25 °C | $R_{OLA}$, $R_{OLB}$ | - | 0.4 | - | Ω |
| Output voltage at high state | $V_{DDA}$ to $V_{OUTA_H}$, $V_{DDB}$ to $V_{OUTB_H}$, $I_{OUTA}$ = $I_{OUTB}$ = -10 mA, $V_{INA}$ = $V_{INB}$ = logic H | $V_{OUTA_H}$, $V_{OUTB_H}$ | - | 10 | - | mV |
| Output voltage at low state | $V_{OUTA_L}$ to $V_{SSA}$, $V_{OUTB_L}$ to $V_{SSA}$, $I_{OUTA}$ = $I_{OUTB}$ = -10 mA, $V_{INA}$ = $V_{INB}$ = logic L | $V_{OUTA_L}$, $V_{OUTB_L}$ | - | 4 | - | mV |


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## ELECTRICAL CHARACTERISTICS

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| PARAMETER | TEST CONDITION | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Clamping voltage | $V_{CLP}$ to $V_{OUT}$, $IN_A$ = $IN_B$ = logic L, $I_{OUT}$ = 500 mA, t = 10 µs | $V_{OUTA}$ to $V_{DDA}$ | - | 1 | - | V |
| Clamping voltage | | $V_{OUTB}$ to $V_{DDB}$ | - | 1 | - | V |
| Clamping voltage | | $V_{SSA}$ to $V_{OUTA}$ | - | 1 | - | V |
| Clamping voltage | | $V_{SSB}$ to $V_{OUTB}$ | - | 1 | - | V |
| Active pull-down voltage on $OUT_X$ | $I_{OUT}$ = 0.1 × $I_{OX\ (typ.)}$, $V_{DDX}$ = open | $V_{OUTSD}$ | - | - | 2.5 | V |
| Clamping voltage to $V_{DD}$ | $V_{OUTA}$ to $V_{DDA}$, $IN_A$ = logic L, $I_{OUTA}$ = 500 mA, t = 10 µs | $V_{CLP-OUT}$ | - | 1 | - | V |
| | $V_{OUTB}$ to $V_{DDB}$, $IN_B$ = logic L, $I_{OUTB}$ = 500 mA, t = 10 µs | | - | 1 | - | V |
| Clamping voltage to GND | $V_{SSA}$ to $V_{OUTA}$, $IN_A$ = logic H, $I_{OUTA}$ = -500 mA, t = 10 µs | $V_{CLP-OUT}$ | - | 1 | - | V |
| | $V_{SSB}$ to $V_{OUTB}$, $IN_B$ = logic H, $I_{OUTB}$ = -500 mA, t = 10 µs | | - | 1 | - | V |

## SWITCHING CHARACTERISTICS

(unless otherwise noted, all typ. values at $T_{amb}$ = 25 °C, $V_{CCI}$ = 3.3 V or 5 V, 0.1 µF capacitor from $V_{CCI}$ to GND, $V_{DDA}$ = $V_{DDB}$ = 15 V for 6 V, 9.2 V, and 13.7 V UVLO, and 20 V for 18 VUVLO, 1 µF capacitor from $V_{DDA}$ to $V_{SSA}$ and $V_{DDB}$ to $V_{SSB}$, $T_{amb}$ = -40 °C to +125 °C)

| PARAMETER | TEST CONDITION | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Output rise time | $C_{OUT}$ = 1.8 nF | $t_r$ | - | 10 | 18 | ns |
| Output fall time | $C_{OUT}$ = 1.8 nF | $t_f$ | - | 10 | 18 | ns |
| Device start-up time at $V_{CCI}$ | Time from $V_{CCI}$ = $V_{CCI_UV+}$ to OUT, IN = logic H | $t_{VCCI+}$ to OUT | - | 72 | 100 | µs |
| Device start-up time at $V_{DDA}$ | Time from $V_{DDA}$ = $V_{DDA_UV+}$ to $OUT_A$, $IN_A$ = logic H | $t_{VDDA+}$ to OUT | - | 13 | 20 | µs |
| Device start-up time at $V_{DDB}$ | Time from $V_{DDB}$ = $V_{DDB_UV+}$ to $OUT_B$, $IN_B$ = logic H | $t_{VDDB+}$ to OUT | - | 13 | 20 | µs |
| Minimum pulse width | Output off for less than minimum, $C_{OUT}$= 0 pF | $t_{PWmin.}$ | - | 12 | 20 | ns |
| Propagation delay from INA to OUTA falling edges | | $t_{PDHL}$ | 29 | 39 | 49 | ns |
| Propagation delay from INB to OUTB falling edges | | $t_{PDHL}$ | 29 | 39 | 49 | ns |
| Propagation delay from INA to OUTA rising edges | | $t_{PDLH}$ | 29 | 39 | 49 | ns |
| Propagation delay from INB to OUTB rising edges | | $t_{PDLH}$ | 29 | 39 | 49 | ns |
| Pulse width distortion | $\lvert t_{PDLH} - t_{PDHL} \rvert$ | $t_{PWD}$ | - | - | 5 | ns |
| Propagation delays matching between $V_{OUTA}$, $V_{OUTB}$ | f = 100 kHz | $t_{DM}$ | - | - | 5 | ns |
| Shutdown time from disable logic true | | $t_{SD}$ | - | - | 60 | ns |
| Restart Time from Disable False | | $t_{RESTART}$ | - | - | 60 | ns |
| Dead Time | Pull DT pin to $V_{CCI}$ | $t_D$ | Overlap determined by $IN_A$, $IN_B$ | | | ns |
| | DT pin is left open | | 0 | 8 | 15 | ns |
| | $R_{DT}$ = 20 kΩ | | 150 | 200 | 250 | ns |


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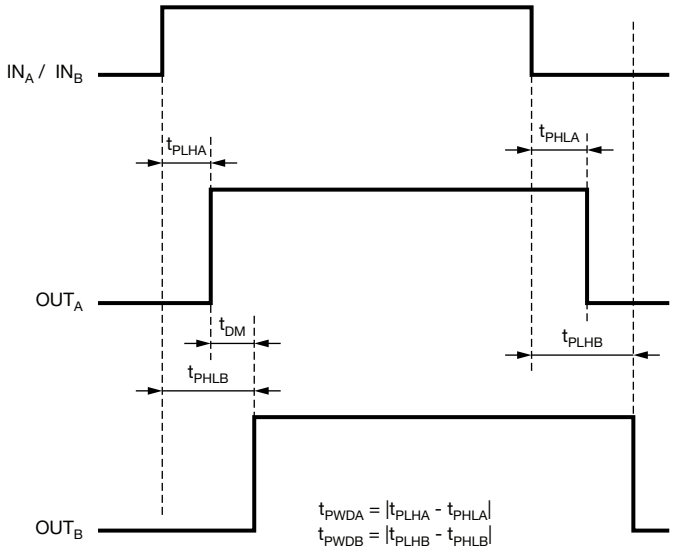



Fig. 3 - Pulse Width Distortion Measurement

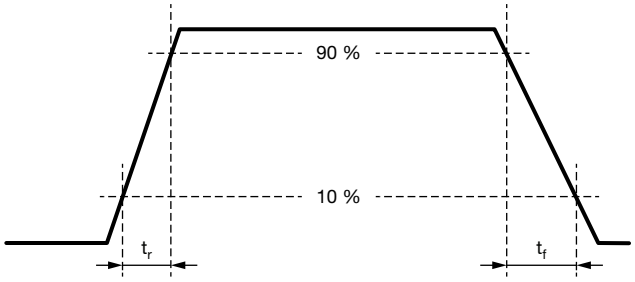



Fig. 4 - Rising and Falling Time Measurement

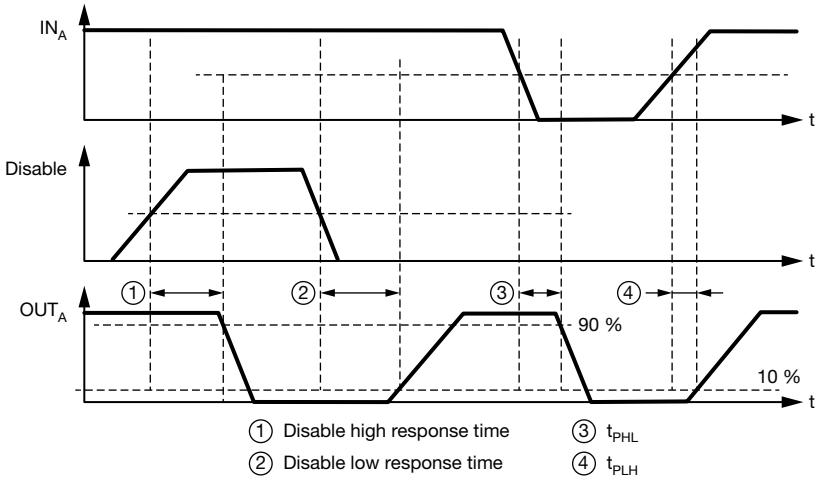



Fig. 5 - Disable Pin Timing Measurement


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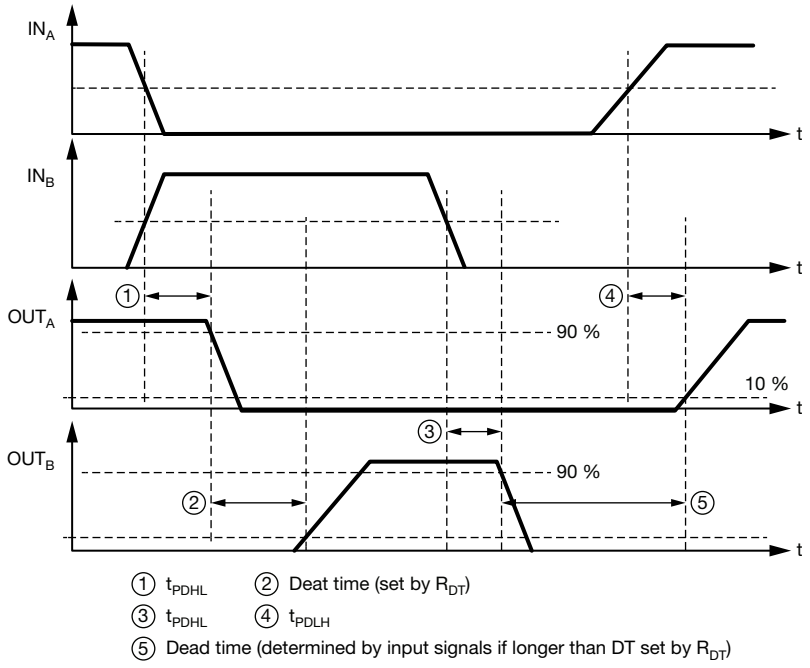



Fig. 6 - Dead Time Switching Diagram

Before the driver is ready to deliver a proper output state, there is a power-up delay from the UVLO rising edge to output and it is defined as $t_{VCCI+}$ to OUT for $V_{CCI}$ UVLO (typically 82 µs) and $t_{VDD+}$ to OUT for $V_{DD}$ UVLO (typically 45 µs). It is recommended to consider proper margin before launching PWM signal after the driver's $V_{CCI}$ and $V_{DD}$ bias supply is ready. Fig. 32 and Fig. 33 show the power up UVLO delay timing diagram for $V_{CCI}$ and $V_{DD}$.

If $IN_A$ or $IN_B$ are active before $V_{CCI}$ or $V_{DD}$ have crossed above their respective on thresholds, the output will not update until $t_{VCCI+}$ to OUT or $t_{VDD+}$ to OUT after $V_{CCI}$ or $V_{DD}$ crossing its UVLO rising threshold. However, when either $V_{CCI}$ or $V_{DD}$ receive a voltage less than their respective off thresholds, there is < 1 µs delay, depending on the voltage slew rate on the supply pins, before the outputs are held low. This asymmetric delay is designed to ensure safe operation during $V_{CCI}$ or $V_{DD}$ brownouts.

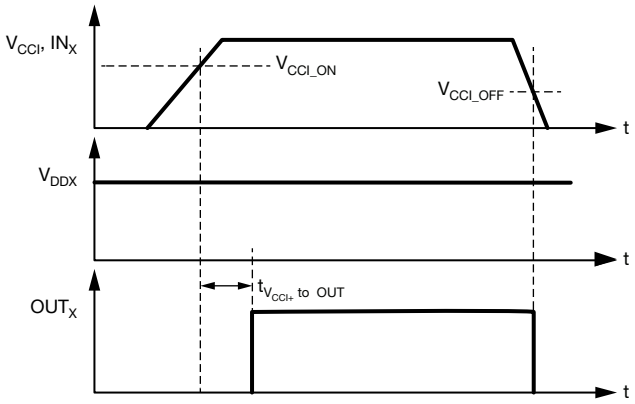



Fig. 7 - $V_{CCI}$ Power-Up UVLO Delay

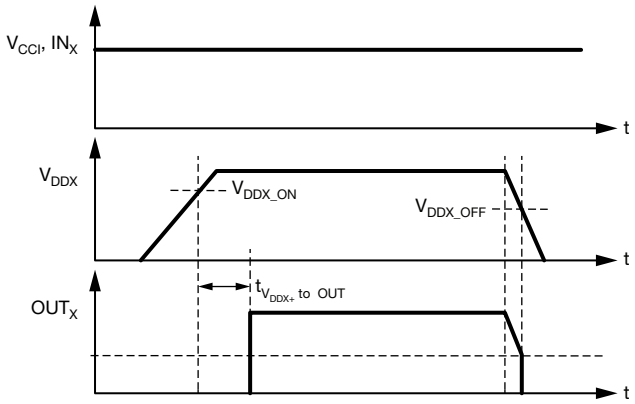



Fig. 8 - $V_{DDA}$ / $V_{DDB}$ Power-Up UVLO Delay


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**COMMON MODE TRANSIENT IMMUNITY**

(unless otherwise noted, all typ. values at $T_{amb}$ = 25 °C, $V_{CCI}$ = 3.3 V or 5 V, 0.1 µF capacitor from $V_{CCI}$ to GND, $V_{DDA}$ = $V_{DDB}$ = 15 V for 6 V, 9.2 V, and 13.7 V UVLO, and 20 V for 18 V UVLO, 1 µF capacitor from $V_{DDA}$ to $V_{SSA}$ and $V_{DDB}$ to $V_{SSB}$, $T_{amb}$ = -40 °C to +125 °C)

| PARAMETER | TEST CONDITION | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| High-level common-mode transient immunity | $IN_A$ and $IN_B$ both are tied to $V_{CCI}$; $V_{CM}$ = 1000 V | $\|CM_H\|$ | 125 | - | - | kV/µs |
| Low-level common-mode transient immunity | $IN_A$ and $IN_B$ both are tied to GND; $V_{CM}$ = 1000 V | $\|CM_L\|$ | 125 | - | - | kV/µs |

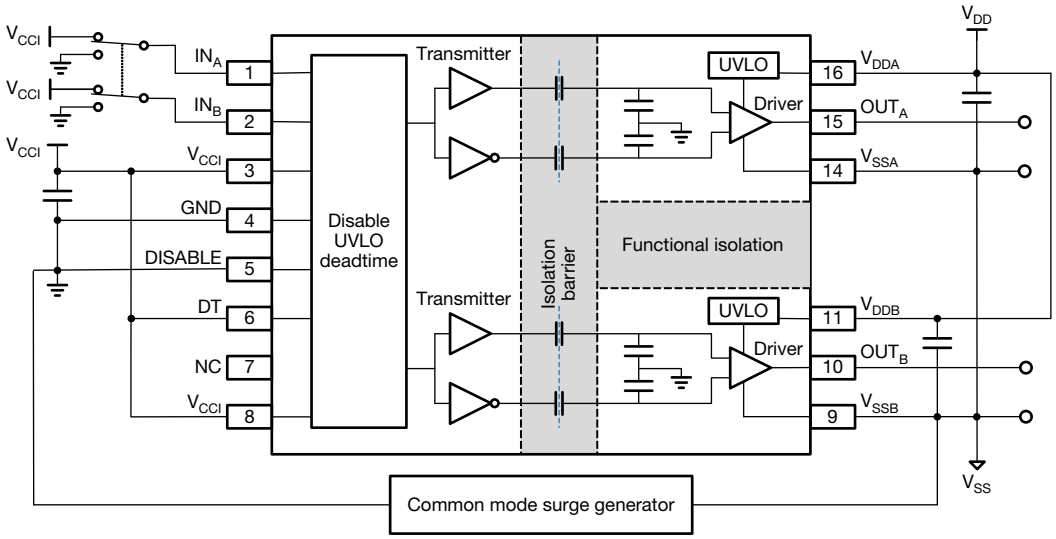



Fig. 9 - Simplified CMTI Test Setup


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## FUNCTIONAL DESCRIPTION

The VID21540A is a dual-channel gate driver with integrated functions like a programmable dead time (DT) control, a DISABLE function and the undervoltage lockout (UVLO) function.

To avoid malfunction at open inputs or too short input pulses, the outputs were kept on low level to inhibit the switching transistors from turning on.

### $V_{DD}$, $V_{CCI}$, and Under Voltage Lock Out (UVLO)

The VID21540A has a under-voltage protection (UVLO) function on primary and secondary side. When the $V_{DD}$ voltage is lower than $V_{VDD_ON}$ at device start-up or lower than $V_{VDD_OFF}$ after start-up, the $V_{DD}$ UVLO feature holds the corresponding output low, regardless of the logic status of the input pins ($IN_A$ and $IN_B$).

| $V_{CCI}$ UVLO FEATURE LOGIC | | | | |
|---|---|---|---|---|
| **CONDITION** | **INPUTS** | | **OUTPUTS** | |
| | **$IN_A$** | **$IN_B$** | **$OUT_A$** | **$OUT_B$** |
| $V_{CCI}$ to GND < $V_{VCCI_ON}$ during device start up | H | L | L | L |
| | L | H | L | L |
| | H | H | L | L |
| | L | L | L | L |
| $V_{CCI}$ to GND < $V_{VCCI_OFF}$ after device start up | H | L | L | L |
| | L | H | L | L |
| | H | H | L | L |
| | L | L | L | L |
| $V_{DDA}$, $V_{DDB}$ to $V_{SSA}$, $V_{SSB}$ < $V_{VDD_ON}$ during device start up | H | L | L | L |
| | L | H | L | L |
| | H | H | L | L |
| | L | L | L | L |
| $V_{DDA}$, $V_{DDB}$ to $V_{SSA}$, $V_{SSB}$ < $V_{VDD_OFF}$ after device start up | H | L | L | L |
| | L | H | L | L |
| | H | H | L | L |
| | L | L | L | L |

### Input and Output Logic Table

INPUT / OUTPUT logic table (assuming that $V_{CCI}$, $V_{DDA}$, $V_{DDB}$ are powered up).

| | | | | | |
|---|---|---|---|---|---|
| **INPUTS** | | **DISABLE** | **OUTPUTS** | | **COMMENTS** |
| **$IN_A$** | **$IN_B$** | | **$OUT_A$** | **$OUT_B$** | |
| L | L | L or left open | L | L | If dead time function is used, output transitions occur after the dead time expires |
| L | H | L or left open | L | H | |
| H | L | L or left open | H | L | |
| H | H | L or left open | L | L | DT is left open or programmed with RDT |
| H | H | L or left open | H | H | DT pin pulled to $V_{CCI}$ |
| Left open | Left open | L or left open | L | L | - |
| X (1) | X (1) | H | L | L | - |

**Note**

(1) "X" means L, H, or left open


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### Disable Function

Setting the DISABLE pin to logic high shuts down both outputs simultaneously. Leaving the DISABLE pin open or tying to GND will ensure the normal operation.

In case of malfunction or other events, the response time is in the range of 20 ns. Assuming that $V_{CCI}$ is above the UVLO threshold level.

If not used, please connect the DISABLE pin to GND. Further it is recommended to bypass the pin with a 1 nF low ESR / ESL capacitor close to the pin for a better noise immunity.

## DEAD TIME (DT) FUNCTION

The dead time (DT) can be adjusted as following:

### DT Pin connected to $V_{CC}$

Output levels follow input logic levels. This allows the both outputs to overlap.

### DT Pin Left Open or Connected to a Programming Resistor Between DT and GND

If the DT pin is left open, the dead time duration ($t_{DT}$) is set to < 15 ns.

The dead time duration ($t_{DT}$) can be programmed using a resistor ($R_{DT}$)) between the DT pin and GND. The duration time can be calculated as $t_{DT} \approx 10 \times R_{DT}$. Where $R_{DT}$ is in kΩ and $t_{DT}$ is in ns units.

The programmed dead time is being triggered by a falling edge of the input signals.

In case both inputs are set to logic high simultaneously, both outputs will immediately be set low level. This feature is used to prevent shoot-through, and it doesn't affect the programmed dead time setting for normal operation.

**INPUT AND OUTPUT RELATIONSHIP**

| CONDITION | $IN_B$ | $IN_A$ | $OUT_A$ / $OUT_B$ |
|---|---|---|---|
| A | Goes low | Goes high | $IN_B$ sets $OUT_B$ low immediately and assigns the programmed dead time to $OUT_A$; $OUT_A$ is allowed to go high after the programmed dead time |
| B | Goes high | Goes low | Now $IN_A$ sets $OUT_A$ low immediately and assigns the programmed dead time to $OUT_B$; $OUT_B$ is allowed to go high after the programmed dead time |
| C | Goes low | Still low | Condition C: $IN_B$ goes low, $IN_A$ is still lowing sets $OUT_B$ low immediately and assigns the programmed dead time for obtain this case, the input signal's own dead time is longer than the programmed dead time; thus, when $IN_A$ goes high, it immediately sets $OUT_A$ high |
| D | Still low | Goes low | Condition D: $IN_A$ goes low, $IN_B$ is still lowing sets $OUT_A$ low immediately and assigns the programmed dead time to $OUT_B$; $IN_B$'s own dead time is longer than the programmed dead time; thus, when $IN_B$ goes high, it immediately sets $OUT_B$ high |
| E | Still high | Goes high | Condition E: $IN_A$ goes high, while $IN_B$ and $OUT_B$ are still high; to avoid overshoot, $IN_A$ immediately pulls $OUT_B$ low and keeps $OUT_A$ low; after some time $IN_B$ goes low and assigns the programmed dead time to $OUT_A$; $OUT_B$ is already low; after the programmed dead time, $OUT_A$ is allowed to go high |
| F | Goes high | Still high | Condition F: $IN_B$ goes high, while $IN_A$ and $OUT_A$ are still high; to avoid overshoot, $IN_B$ immediately pulls $OUT_A$ low and keeps $OUT_B$ low; after some time $IN_A$ goes low and assigns the programmed dead time to $OUT_B$; $OUT_A$ is already low; after the programmed dead time, $OUT_B$ is allowed to go high |

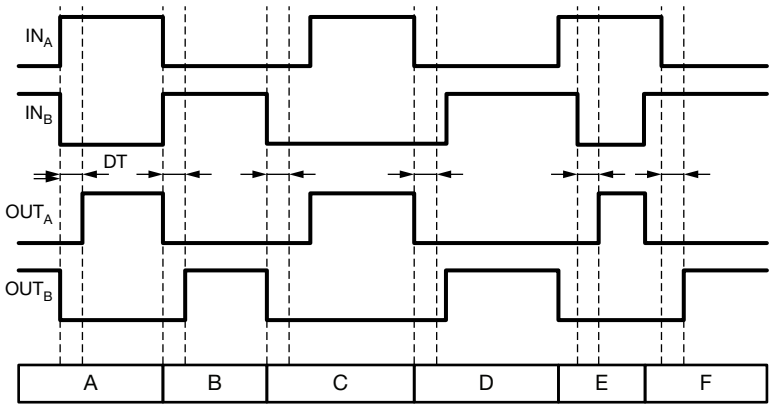



Fig. 10 - Input, Output, and Deadtime Logic Table


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## OUTPUT STAGE CONFIGURATION WITH ACTIVE PULLDOWN FEATURE

The VID21540A series output stages are designed with a P-channel MOSFET for pull-up and an N-Channel MOSFET for pulldown the output voltage level.

To prevent the output from being false turned on in case off floating $V_{DDx}$, the output stages support an active pulldown feature which clamps the output to the respective $V_{SSx}$.

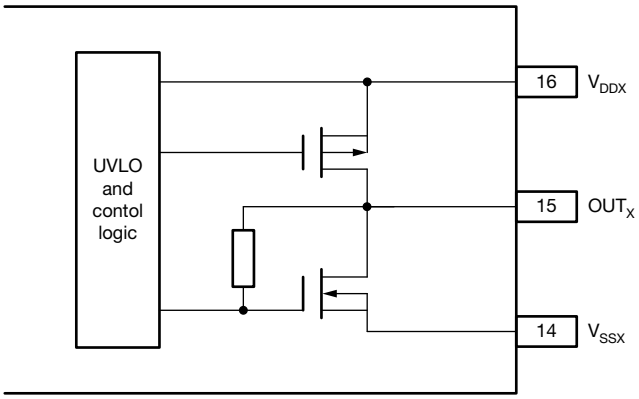



Fig. 11

## SHORT CIRCUIT CLAMPING

In case of a short circuit condition, the voltage drop through the driven power Transistor (IGBT, SiC, GaN, MOSFET) changes rapidly and the gate voltage will rise, too, because of the miller capacitance. The internal protection diode between OUTx and $V_{DDx}$ pins clamp this voltage to ~1 V higher than the respective supply voltage. A current of 500mA (max) may be sourced back to the supply pin via this diode. If required, an external Schottky diode may be added.

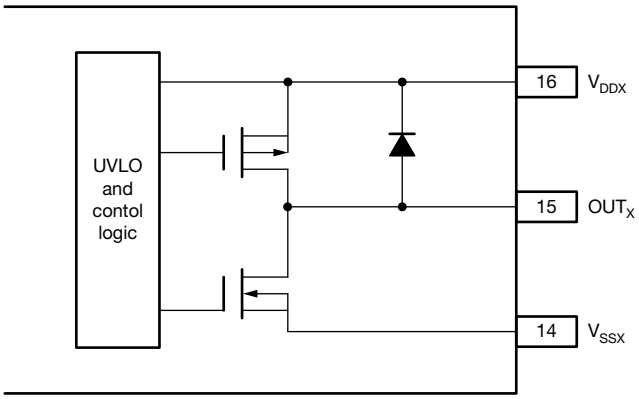



Fig. 12


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## SHORT CIRCUIT PROTECTION

In case the input is in logic “H” state, the respective driver output tries to pull to $V_{DDx}$ with $I_{OUT}$ current for 5 µs. If it fails to pull up normally 10 consecutive times, the internal short-circuit protection is triggered and the output does not longer follows the input to pull up. To reset and return to normal condition, the driver side needs to be is powered on again.

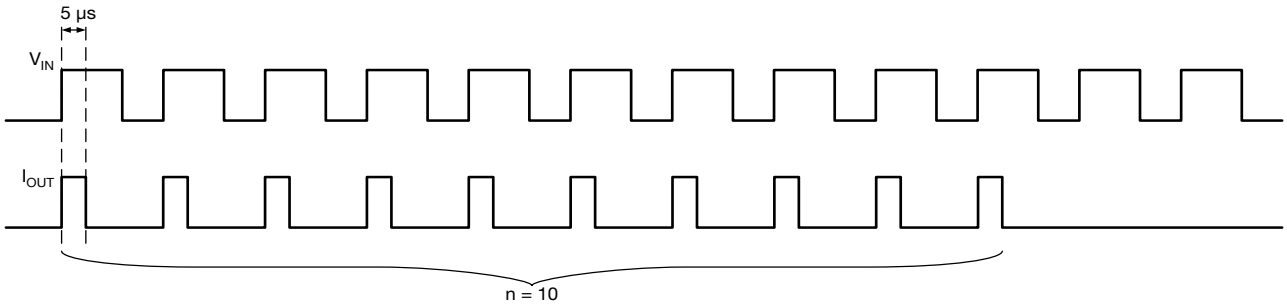



Fig. 13

## PACKAGE DIMENSIONS (in millimeters)

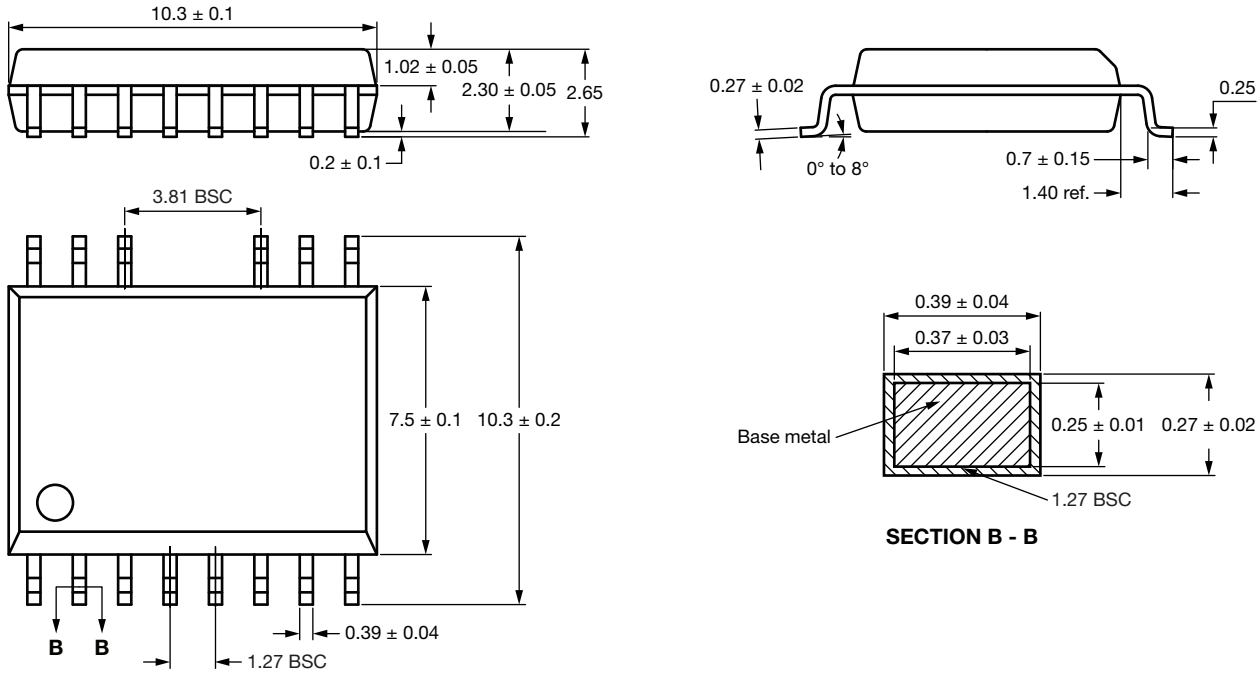



Fig. 14 - 14-Lead Wide Body Outline Package (SOIC-14, wide body)


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**FOOTPRINT** (in millimeters)

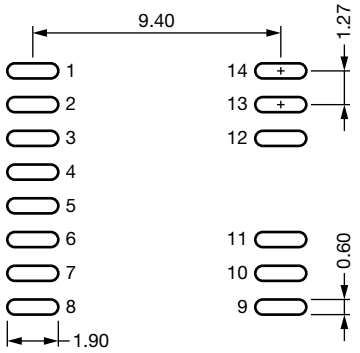



Fig. 15 - 14-Lead Wide Body SOIC (SOIC-14, wide body) Land Pattern

**PACKAGE MARKING** (example)

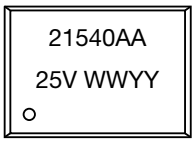



Fig. 16 - Example of VID21540AAT

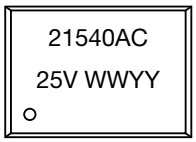



Fig. 18 - Example of VID21540ACT

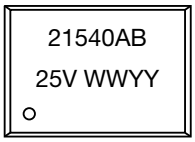



Fig. 17 - Example of VID21540ABT

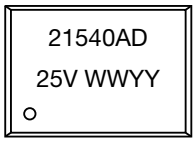



Fig. 19 - Example of VID21540ADT

**Notes**
- “WWYY” is the date code marking (Y = year code, WW = week code)
- Tape and reel suffix (T) is not part of the package marking


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## PACKING INFORMATION

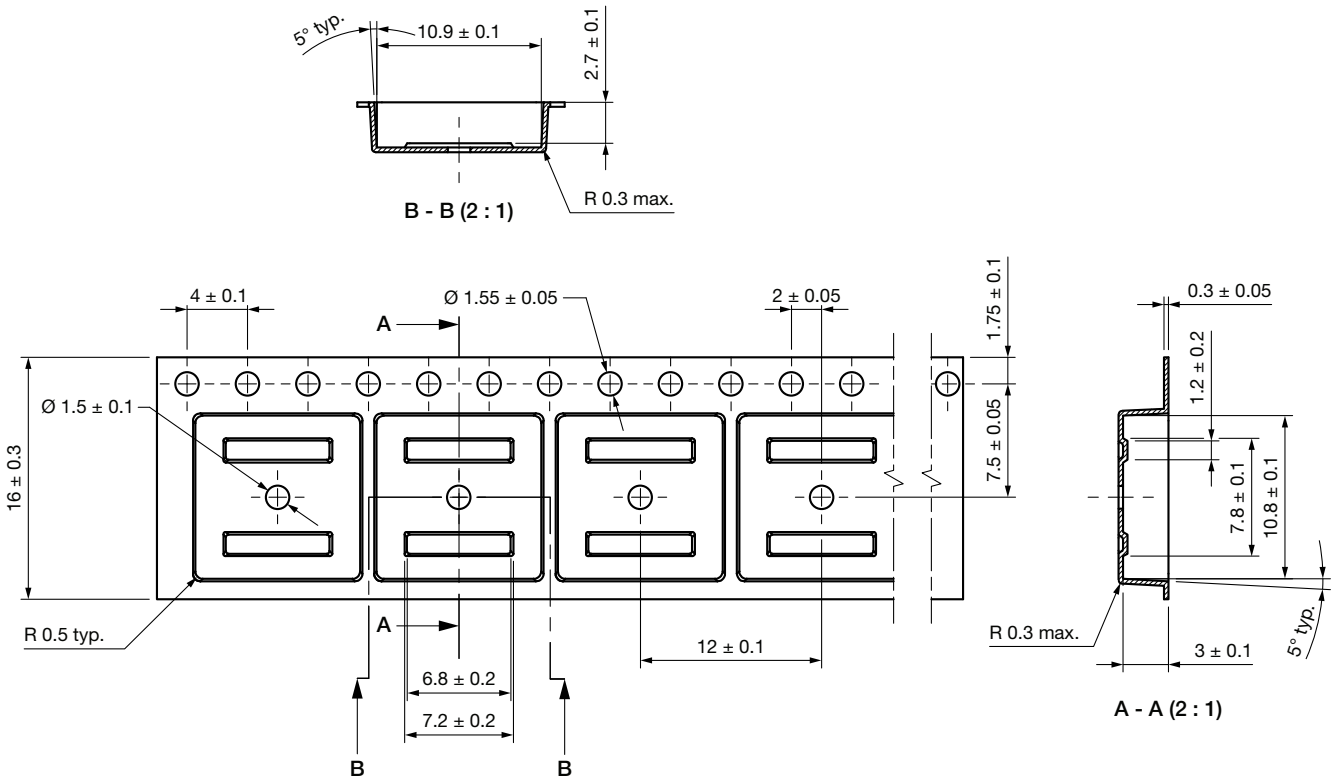



Fig. 20 - 14-Lead Wide Body Outline Package (1500 pieces on reel)

## HANDLING AND STORAGE CONDITIONS

Floor life: unlimited

Conditions: $T_{amb}$ < 30 °C, RH < 85 %

Moisture sensitivity level rating: Level-2-260C-1 year, according to the JEDEC industry standard classifications, and peak solder temperature


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|---|---|---|
| **DATASHEET VERSION** | **REVISION DATE** | **CHANGE** |
| 1.0 | 21-Oct-2026 | Initial datasheet release |


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