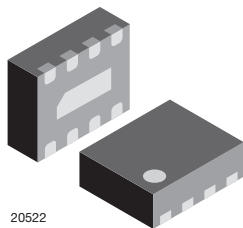
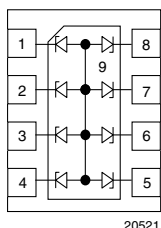


# 8-Line ESD Protection Diode Array in LLP1713-9L



## FEATURES

- Ultra compact LLP1713-9L package
- Low package profile < 0.6 mm
- 8-line ESD protection
- Low leakage current  $I_R < 1 \mu A$
- Low load capacitance  $C_D = 30 \text{ pF}$
- ESD immunity acc. IEC 61000-4-2  
± 25 kV contact discharge  
± 30 kV air discharge
- Working voltage range  $V_{RWM} = 5 \text{ V}$
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



## MARKING (example only)



Dot = pin 1 marking  
Y = type code (see table below)  
XX = date code

## LINKS TO ADDITIONAL RESOURCES



| ORDERING INFORMATION |                    |  |                        |
|----------------------|--------------------|--|------------------------|
| DEVICE NAME          | ORDERING CODE      | TAPED UNITS PER REEL<br>(8 mm TAPE ON 7" REEL) | MINIMUM ORDER QUANTITY |
| VESD05A8A-HNH        | VESD05A8A-HNH-GS08 | 3000   | 15 000                 |

| PACKAGE DATA  |              |           |        |   |                                      |                              |
|---------------|--------------|-----------|--------|---|--------------------------------------|------------------------------|
| DEVICE NAME   | PACKAGE NAME | TYPE CODE | WEIGHT | MOLDING COMPOUND<br>FLAMMABILITY RATING | MOISTURE<br>SENSITIVITY LEVEL        | SOLDERING CONDITIONS         |
| VESD05A8A-HNH | LLP1713-9L   | B         | 3.7 mg | UL 94 V-0                               | MSL level 1<br>(according J-STD-020) | Peak temperature max. 260 °C |

| ABSOLUTE MAXIMUM RATINGS VESD05A8A-HNH |  |           |             |      |
|--|--|-----------|-------------|------|
| RATING                                 | TEST CONDITIONS  | SYMBOL    | VALUE       | UNIT |
| Peak pulse current                     | BiAs-mode: each input (pin 1 to pin 8) to ground (pin 9)<br>acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ ; single shot                           | $I_{PPM}$ | 5           | A    |
|  | BiSy-mode: each input (pin 1 to pin 8) to any other input pin.<br>Pin 9 not connected. Acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ /single shot | $I_{PPM}$ | 2.5         | A    |
| Peak pulse power                       | BiAs-mode: each input (pin 1 to pin 8) to ground (pin 9)<br>acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ ; single shot                           | $P_{PP}$  | 65          | W    |
|  | BiSy-mode: each input (pin 1 to pin 8) to any other input pin<br>Pin 9 not connected. Acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ /single shot  | $P_{PP}$  | 33          | W    |
| ESD immunity                           | Contact discharge acc. IEC 61000-4-2; 10 pulses<br>BiAs-mode: each input (pin 1 to pin 8) to ground (pin 9)                                | $V_{ESD}$ | ± 25        | kV   |
|  | Air discharge acc. IEC 61000-4-2; 10 pulses<br>BiAs-mode: each input (pin 1 to pin 8) to ground (pin 9)                                    | $V_{ESD}$ | ± 30        | kV   |
|  | Contact discharge acc. IEC 61000-4-2; 10 pulses<br>BiSy-mode: each input (pin 1 to pin 8) to any other input pin.<br>Pin 9 not connected.  | $V_{ESD}$ | ± 12        | kV   |
|  | Air discharge acc. IEC 61000-4-2; 10 pulses<br>BiSy-mode: each input (pin 1 to pin 8) to any other input pin.<br>Pin 9 not connected.      | $V_{ESD}$ | ± 12        | kV   |
| Operating temperature                  | Junction temperature   | $T_J$     | -40 to +125 | °C   |
| Storage temperature                    |  | $T_{STG}$ | -55 to +150 | °C   |

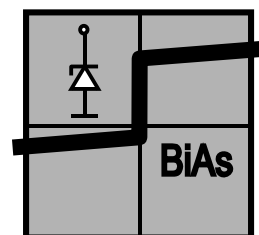
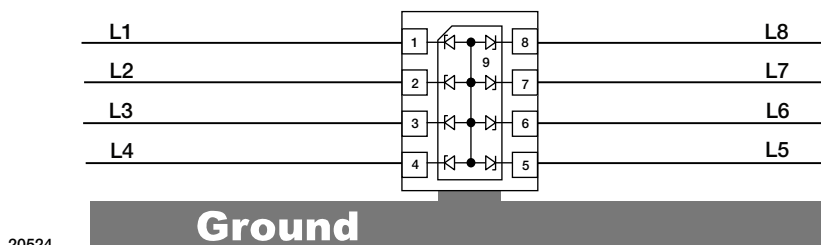
**BiAs-MODE** (8-line bidirectional asymmetrical protection mode)

With the VESD05A8A-HNH up to 8 signal- or data-lines (L1 to L8) can be protected against voltage transients. With pin 9 connected to ground and pin 1 up to pin 8 connected to a signal- or data-line which has to be protected. As long as the voltage level on the data- or signal-line is between 0 V (ground level) and the specified maximum reverse working voltage ( $V_{RWM}$ ) the protection diode between data line and ground offer a high isolation to the ground line. The protection device behaves like an open switch.

As soon as any positive transient voltage signal exceeds the breakdown voltage level of the protection diode, the diode becomes conductive and shorts the transient current to ground. Now the protection device behaves like a closed switch. The clamping voltage ( $V_C$ ) is defined by the breakdown voltage ( $V_{BR}$ ) level plus the voltage drop at the series impedance (resistance and inductance) of the protection device.

Any negative transient signal will be clamped accordingly. The negative transient current is flowing in the forward direction of the protection diode. The low forward voltage ( $V_F$ ) clamps the negative transient close to the ground level.

Due to the different clamping levels in forward and reverse direction the VESD05A8A-HNH clamping behaviour is bidirectional and asymmetrical (BiAs).

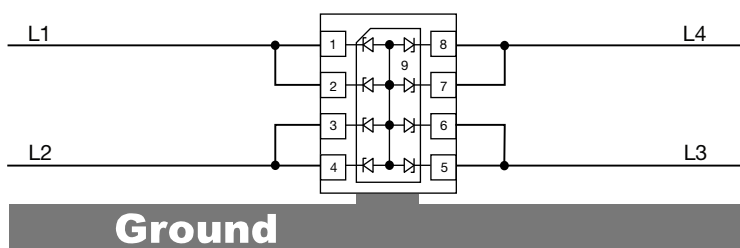

**ELECTRICAL CHARACTERISTICS VESD05A8A-HNH** (Between pin 1 to 8 and pin 9)

( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

| PARAMETER                 | TEST CONDITIONS/REMARKS                     | SYMBOL        | MIN. | TYP.  | MAX. | UNIT          |
|---------------------------|---|---------------|------|-------|------|---------------|
| Protection paths          | Number of lines which can be protected      | $N_{channel}$ | -    | -     | 8    | lines         |
| Reverse stand-off voltage | Max. reverse working voltage                | $V_{RWM}$     | -    | -     | 5    | V             |
| Reverse voltage           | at $I_R = 1\text{ }\mu\text{A}$             | $V_R$         | 5    | -     | -    | V             |
| Reverse current           | at $V_R = V_{RWM} = 5\text{ V}$             | $I_R$         | -    | < 0.1 | 1    | $\mu\text{A}$ |
| Reverse breakdown voltage | at $I_R = 1\text{ mA}$                      | $V_{BR}$      | 6    |       | 8    | V             |
| Reverse clamping voltage  | at $I_{PP} = 5\text{ A acc. IEC 61000-4-5}$ | $V_C$         | -    |       | 13   | V             |
| Forward clamping voltage  | at $I_F = 5\text{ A acc. IEC 61000-4-5}$    | $V_F$         | -    |       | 4.5  | V             |
| Capacitance               | at $V_R = 0\text{ V}; f = 1\text{ MHz}$     | $C_D$         | -    | 30    | 35   | pF            |
|                           | at $V_R = 2.5\text{ V}; f = 1\text{ MHz}$   | $C_D$         | -    | 18    | 23   | pF            |

If a higher surge current or peak pulse current ( $I_{PP}$ ) is needed, some protection diodes in the VESD05A8A-HNH can also be used in parallel in order to “multiply” the performance. If two diodes are switched in parallel you get

- double surge power = double peak pulse current ( $2 \times I_{PPM}$ )
- half of the line inductance = reduced clamping voltage
- half of the line resistance = reduced clamping voltage
- double line capacitance ( $2 \times C_D$ )
- double reverse leakage current ( $2 \times I_R$ )



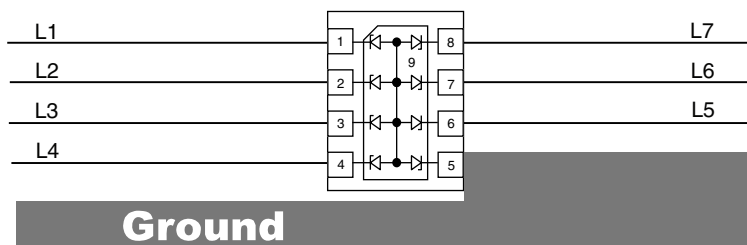
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### BiSy-MODE (7-line bidirectional symmetrical protection mode)

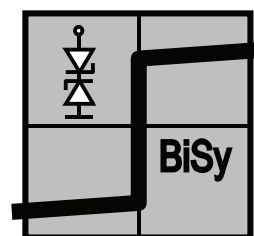
If a bipolar symmetrical protection device is needed the VESD05A8A-HNH can also be used as a seven-line protection device. Therefore seven pins (example: pin 1, 2, 3, 4, 6, 7 and 8) has to be connected to the signal or data-line (L1 to L7) and pin 5 to ground. Pin 9 must not be connected!

Positive and negative voltage transients will be clamped in the same way. The clamping current from one data line through the VESD05A8A-HNH to the ground passes one diode in forward direction and the other one in reverse direction. The clamping voltage ( $V_C$ ) is defined by the breakdown voltage ( $V_{BR}$ ) level of one diode plus the forward voltage of the other diode plus the voltage drop at the series impedances (resistances and inductances) of the protection device.

Due to the same clamping levels in positive and negative direction the VESD05A8A-HNH voltage clamping behaviour is also bidirectional but symmetrical (BiSy).



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### ELECTRICAL CHARACTERISTICS (Between two of the pins 1 to 8; other pins not connected)

( $T_{amb} = 25^\circ\text{C}$ , unless otherwise specified)

| PARAMETER                 | TEST CONDITIONS/REMARKS                                   | SYMBOL        | MIN. | TYP.  | MAX. | UNIT          |
|---------------------------|---|---------------|------|-------|------|---------------|
| Protection paths          | Number of lines which can be protected                    | $N_{channel}$ | -    | -     | 7    | lines         |
| Reverse stand-off voltage | Max. reverse working voltage                              | $V_{RWM}$     | -    | -     | 5.5  | V             |
| Reverse voltage           | at $I_R = 1 \mu\text{A}$                                  | $V_R$         | 5.5  | -     | -    | V             |
| Reverse current           | at $V_R = V_{RWM} = 5.5 \text{ V}$                        | $I_R$         | -    | < 0.1 | 1    | $\mu\text{A}$ |
| Reverse breakdown voltage | at $I_R = 1 \text{ mA}$                                   | $V_{BR}$      | 6.5  | -     | 8.7  | V             |
| Reverse clamping voltage  | at $I_{PP} = 2.5 \text{ A acc. IEC 61000-4-5}$            | $V_C$         | -    | -     | 13   | V             |
| Capacitance               | at $V_R = 0 \text{ V}; f = 1 \text{ MHz}$                 | $C_D$         | -    | 15    | 18   | pF            |
|                           | at $V_R = 2.5 \text{ V}; f = 1 \text{ MHz}$               |               | -    | 12    | 15   |               |
|                           | All pins at $V_R = 0 \text{ V}$ . Pin no. 9 not connected |               | -    | 26    | -    |               |

## TYPICAL CHARACTERISTICS ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

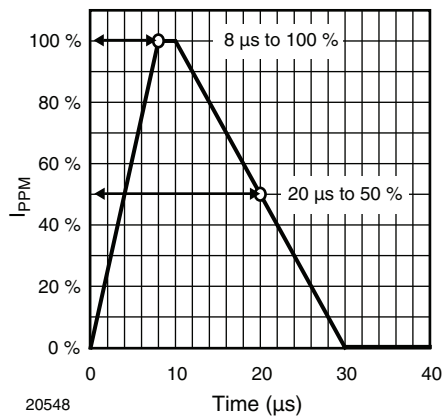


Fig. 1 - ESD Discharge Current Wave Form  
acc. IEC 61000-4-2 (330  $\Omega$ /150 pF)

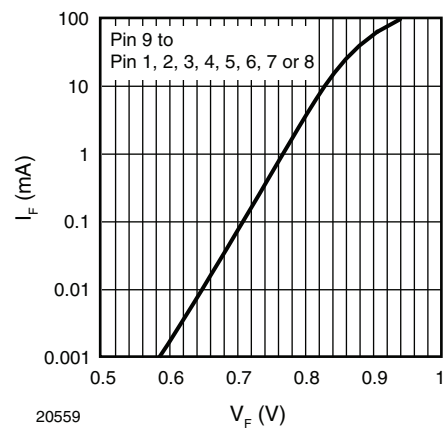


Fig. 4 - Typical Forward Current  $I_F$  vs. Forward Voltage  $V_F$

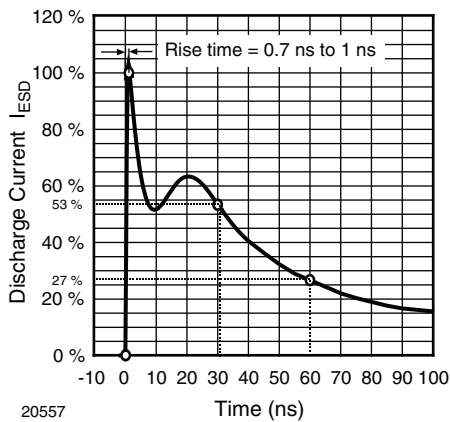


Fig. 2 - 8/20  $\mu\text{s}$  Peak Pulse Current Wave Form  
acc. IEC 61000-4-5

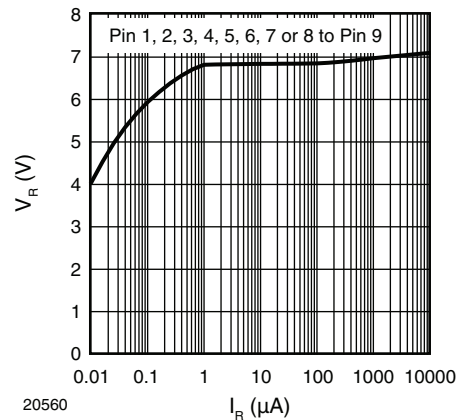


Fig. 5 - Typical Reverse Voltage  $V_R$  vs. Reverse Current  $I_R$

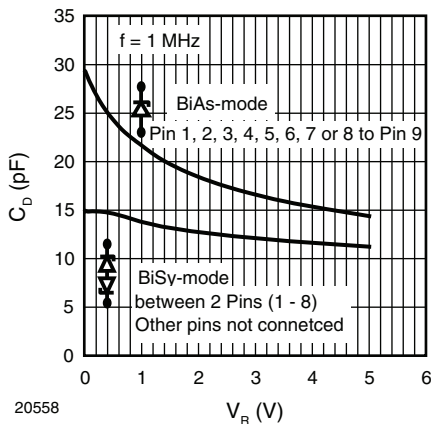


Fig. 3 - Typical Capacitance  $C_D$  vs. Reverse Voltage  $V_R$

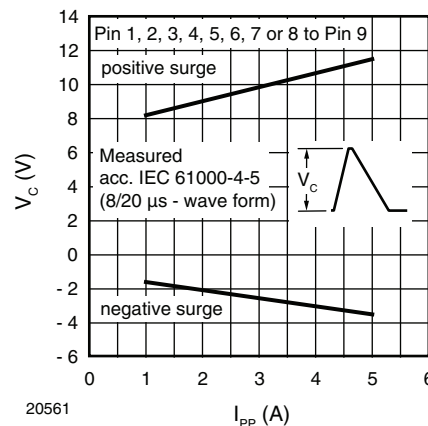


Fig. 6 - Typical Peak Clamping Voltage  $V_C$  vs.  
Peak Pulse Current  $I_{PP}$

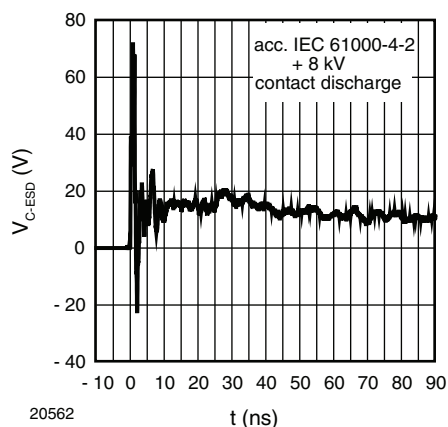


Fig. 7 - Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

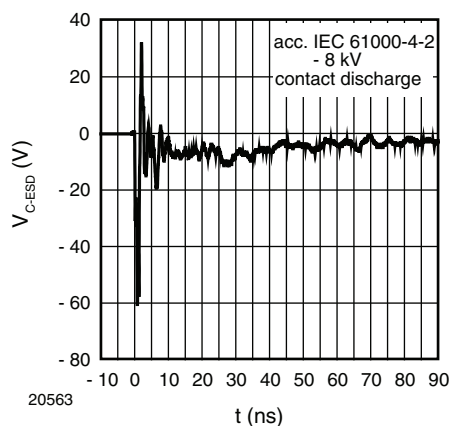


Fig. 8 - Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

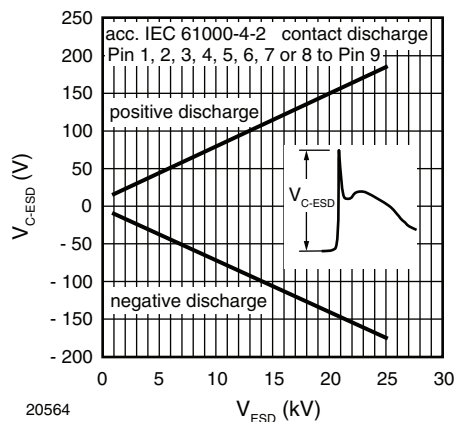
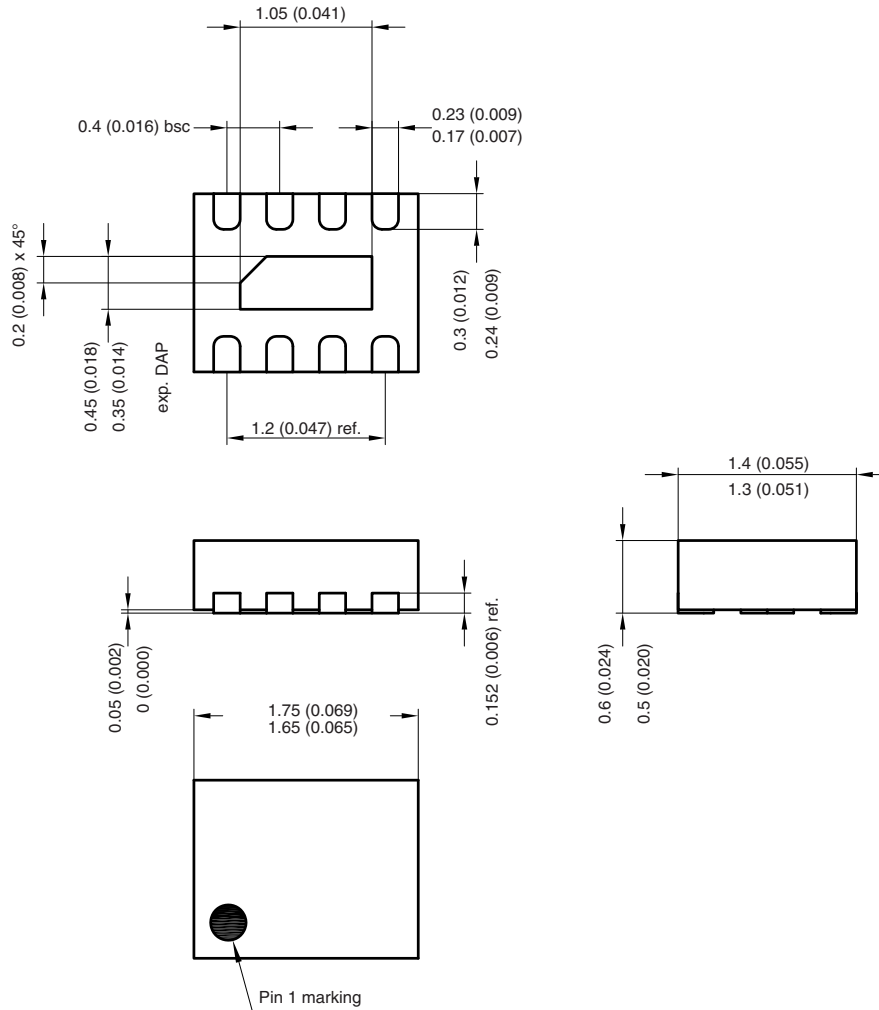
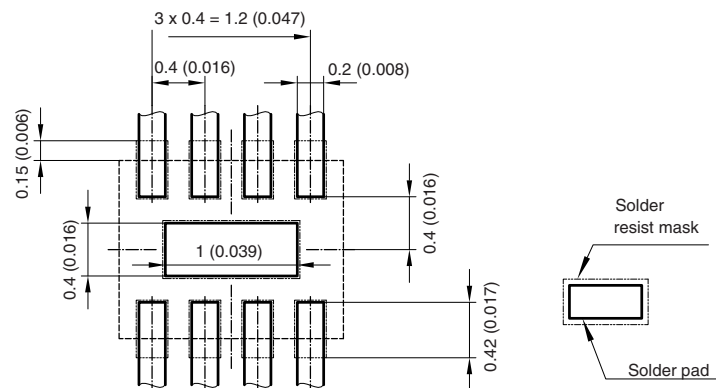


Fig. 9 - Typical Peak Clamping Voltage at ± ESD Contact Discharge (acc. IEC 61000-4-2)

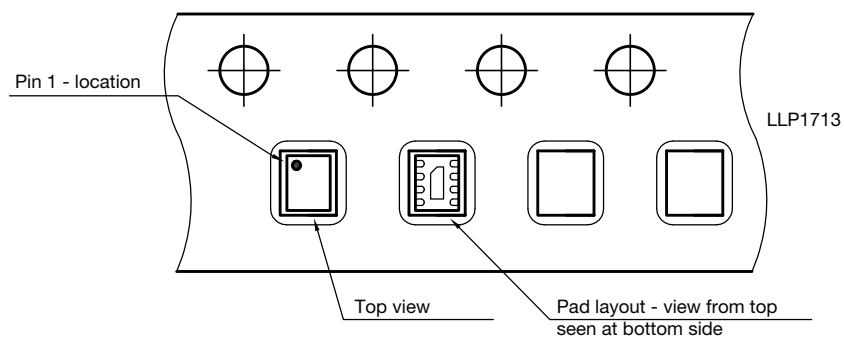
## PACKAGE DIMENSIONS in millimeters (Inches): **LLP1713-9L**



Foot print recommendation:



Document no.:S8-V-3906.04-001 (4)  
 Created - Date: 28. August 2006  
 Rev. 1 - Date: 27. May 2008  
 20386





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