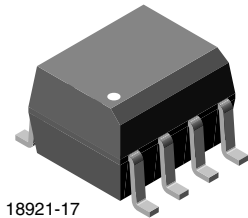
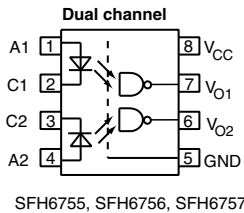
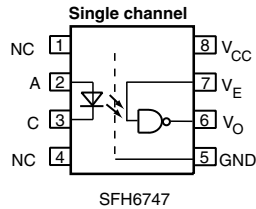


## High Speed Optocoupler, 10 MBd, SOIC-8 Package



18921-17



### DESCRIPTION

The SFH6747, SFH6755, SFH6756, and SFH6757 family are single and dual channel 10 MBd optocoupler utilizing a high efficient input LED coupled with an integrated optical photodiode IC detector. The detector has an open drain NMOS-transistor output, providing less leakage compared to an open collector Schottky clamped transistor output. For the single channel type, an enable function on pin 7 allows the detector to be strobed. The use of a 0.1  $\mu\text{F}$  bypass capacitor connected between pin 5 and 8 is recommended.

### AGENCY APPROVALS

- UL1577, file no. E52744
- cUL-file no. E52744, equivalent to CSAkm bulletin 5A

### FEATURES

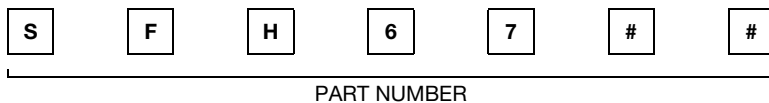
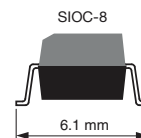
- Choice of CMR performance of 10 kV/ $\mu\text{s}$ , 5 kV/ $\mu\text{s}$ , and 0.1 kV/ $\mu\text{s}$
- High speed: 10 MBd typical
- + 5 V CMOS compatibility
- Pure tin leads
- Guaranteed AC and DC performance over temperature: -40 °C to +100 °C temperature range
- Meets IEC 60068-2-42 (SO<sub>2</sub>) and IEC 60068-2-43 (H<sub>2</sub>S) requirements
- Low input current capability: 5 mA
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT

### APPLICATIONS

- Microprocessor system M interface
- PLC, ATE input / output isolation
- Computer peripheral interface: SPI
- Digital fieldbus isolation: CC-Link, DeviceNet, profibus, SDS
- High speed A/D and D/A conversion
- AC plasma display panel level shifting
- Multiplexed data transmission
- Digital control power supply
- Ground loop elimination

### ORDERING INFORMATION


 T  
 TAPE  
 AND  
 REEL


AGENCY CERTIFIED/PACKAGE	1 CHANNEL		2 CHANNELS	
	CMR (kV/ $\mu\text{s}$ )		CMR (kV/ $\mu\text{s}$ )	
UL, cUL	10	0.1	5	10
SOIC-8	SFH6747T	SFH6755T	SFH6756T	SFH6757T



TRUTH TABLE (positive logic)		
LED	ENABLE <sup>(1)</sup>	OUTPUT
On	H	L
Off	H	H
On	L	H
Off	L	H
On	NC	L
Off	NC	H

**Note**

<sup>(1)</sup> Only applicable for single channel devices

ABSOLUTE MAXIMUM RATINGS (T <sub>amb</sub> = 25 °C, unless otherwise specified)				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
<b>INPUT</b>				
Average forward current (single channel)		I <sub>F</sub>	20	mA
Average forward current (dual channel)		I <sub>F</sub>	15	mA
Reverse input voltage		V <sub>R</sub>	5	V
Enable input voltage (single channel)		V <sub>E</sub>	V <sub>CC</sub> + 0.5 V	V
Enable input current (single channel)		I <sub>E</sub>	5	mA
Surge current	t = 100 μs	I <sub>FSM</sub>	200	mA
Input power dissipation (single channel)		P <sub>diss</sub>	35	mW
Input power dissipation (per channel for dual channel)		P <sub>diss</sub>	25	mW
<b>OUTPUT</b>				
Supply voltage	1 min maximum	V <sub>CC</sub>	7	V
Output current		I <sub>O</sub>	50	mA
Output voltage		V <sub>O</sub>	7	V
Output power dissipation (single channel)		P <sub>diss</sub>	85	mW
Output power dissipation (per channel for dual channel)		P <sub>diss</sub>	60	mW
<b>COUPLER</b>				
Isolation test voltage	t = 1 s	V <sub>ISO</sub>	4000	V <sub>RMS</sub>
Storage temperature		T <sub>stg</sub>	-55 to +150	°C
Operating temperature		T <sub>amb</sub>	-40 to +100	°C
Lead solder temperature	for 10 s		260	°C
Solder reflow temperature <sup>(1)</sup>	for 1 min		260	°C

**Notes**

- Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability.

<sup>(1)</sup> Refer to reflow profile for soldering conditions for surface mounted devices.

RECOMMENDED OPERATING CONDITION						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating temperature		T <sub>amb</sub>	-40	-	100	°C
Supply voltage		V <sub>CC</sub>	4.5	-	5.5	V
Input current low level		I <sub>FL</sub>	0	-	250	μA
Input current high level		I <sub>FH</sub>	5	-	15	mA
Output pull up resistor		R <sub>L</sub>	330	-	4000	Ω
Logic high enable voltage		V <sub>EH</sub>	2	-	V <sub>CC</sub>	V
Logic low enable voltage		V <sub>EL</sub>	0.0	-	0.8	V
Fanout	R <sub>L</sub> = 1 kΩ	N	-	-	5	-



<b>ELECTRICAL CHARACTERISTICS</b> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>INPUT</b>						
Input forward voltage	$I_F = 10\text{ mA}$	$V_F$	1.1	1.4	1.7	V
Reverse current	$V_R = 5\text{ V}$	$I_R$	-	0.01	10	$\mu\text{A}$
Input capacitance	$f = 1\text{ MHz}, V_F = 0\text{ V}$	$C_I$	-	55	-	pF
<b>OUTPUT</b>						
High level supply current (single channel)	$V_E = 0.5\text{ V}, I_F = 0\text{ mA}$	$I_{CCH}$	-	4.1	7	mA
	$V_E = V_{CC}, I_F = 0\text{ mA}$	$I_{CCH}$	-	3.3	6	mA
High level supply current (dual channel)	$I_F = 10\text{ mA}$	$I_{CCH}$	-	6.5	12	mA
Low level supply current (single channel)	$V_E = 0.5\text{ V}, I_F = 10\text{ mA}$	$I_{CCL}$	-	4	7	mA
	$V_E = V_{CC}, I_F = 10\text{ mA}$	$I_{CCL}$	-	3.3	6	mA
Low level supply current (dual channel)	$I_F = 10\text{ mA}$	$I_{CCL}$	-	6.5	12	mA
High level output current	$V_E = 2\text{ V}, V_O = 5.5\text{ V}, I_F = 250\text{ }\mu\text{A}$	$I_{OH}$	-	0.002	1	$\mu\text{A}$
Low level output voltage	$V_E = 2\text{ V}, I_F = 5\text{ mA}, I_{OL}(\text{sinking}) = 13\text{ mA}$	$V_{OL}$	-	0.2	0.6	V
Input threshold current	$V_E = 2\text{ V}, V_O = 5.5\text{ V}, I_{OL}(\text{sinking}) = 13\text{ mA}$	$I_{TH}$	-	2.4	5	mA
High level enable current		$I_{EH}$	-	-0.6	-1.6	mA
Low level enable current		$I_{EL}$	-	-0.8	-1.6	mA
High level enable voltage		$V_{EH}$	2	-	-	V
Low level enable voltage		$V_{EL}$	-	-	0.8	V

**Note**

- Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

<b>SWITCHING CHARACTERISTICS</b>						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Propagation delay time to high output level	$R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$	$t_{PLH}$	20	48	100	ns
Propagation delay time to low output level	$R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$	$t_{PHL}$	25	50	100	ns
Pulse width distortion	$R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$	$ t_{PHL} - t_{PLH} $	-	2.9	35	ns
Propagation delay skew	$R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$	$t_{PSK}$	-	8	40	ns
Output rise time (10 to 90 %)	$R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$	$t_r$	-	23	-	ns
Output fall time (90 to 10 %)	$R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$	$t_f$	-	7	-	ns
Propagation delay time of enable from $V_{EH}$ to $V_{EL}$	$R_L = 350\text{ }\Omega, C_L = 15\text{ pF}, V_{EL} = 0\text{ V}, V_{EH} = 3\text{ V}$	$t_{ELH}$	-	12	-	ns
Propagation delay time of enable from $V_{EL}$ to $V_{EH}$	$R_L = 350\text{ }\Omega, C_L = 15\text{ pF}, V_{EL} = 0\text{ V}, V_{EH} = 3\text{ V}$	$t_{EHL}$	-	11	-	ns

**Note**

- Over recommended temperature ( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+100\text{ }^{\circ}\text{C}$ ),  $V_{CC} = 5\text{ V}, I_F = 7.5\text{ mA}$  unless otherwise specified. All typicals at  $T_A = 25\text{ }^{\circ}\text{C}, V_{CC} = 5\text{ V}$ .

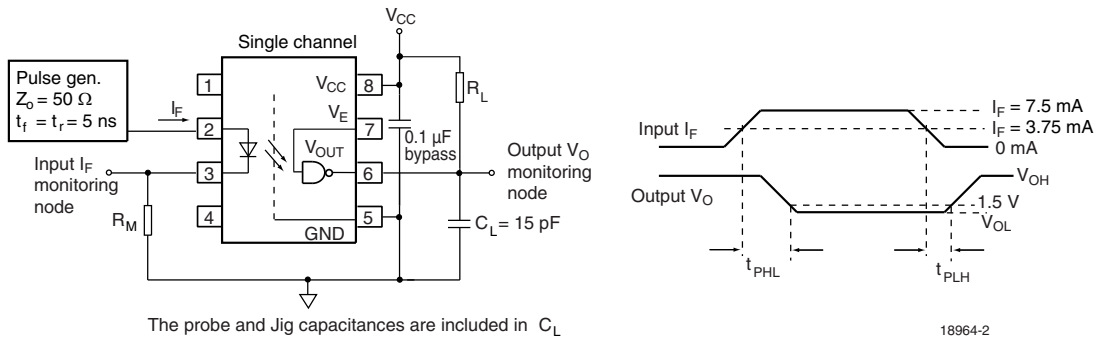


Fig. 1 - Single Channel Test Circuit for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$ , and  $t_f$

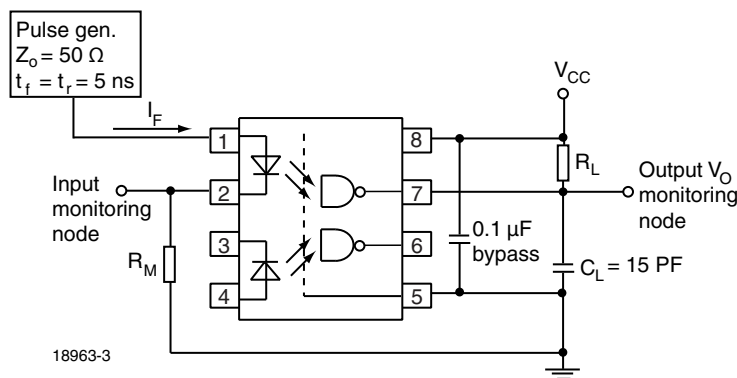


Fig. 2 - Dual Channel Test Circuit for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$ , and  $t_f$

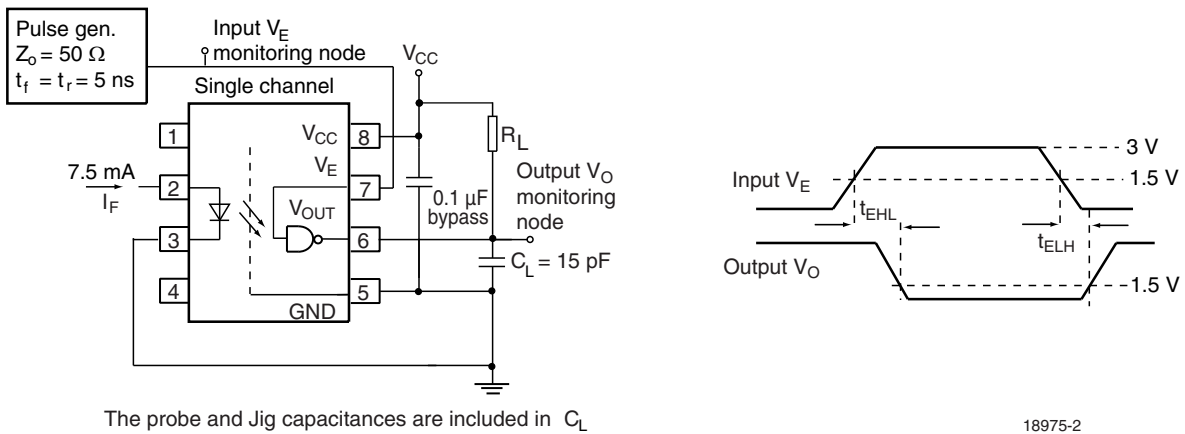


Fig. 3 - Single Channel Test Circuit for  $t_{EHL}$ ,  $t_{ELH}$

COMMON MODE TRANSIENT IMMUNITY						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Common mode transient immunity (high)	$ V_{CM}  = 10\text{ V}$ , $V_{CC} = 5\text{ V}$ , $I_F = 0\text{ mA}$ , $V_{O(\min)} = 2\text{ V}$ , $R_L = 350\ \Omega$ , $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ (1)	$ CM_H $	-	10 000	-	$\text{V}/\mu\text{s}$
	$ V_{CM}  = 50\text{ V}$ , $V_{CC} = 5\text{ V}$ , $I_F = 0\text{ mA}$ , $V_{O(\min)} = 2\text{ V}$ , $R_L = 350\ \Omega$ , $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ (2)	$ CM_H $	5000	10 000	-	$\text{V}/\mu\text{s}$
	$ V_{CM}  = 1\text{ kV}$ , $V_{CC} = 5\text{ V}$ , $I_F = 0\text{ mA}$ , $V_{O(\min)} = 2\text{ V}$ , $R_L = 350\ \Omega$ , $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ (3)	$ CM_H $	10 000	15 000	-	$\text{V}/\mu\text{s}$
Common mode transient immunity (low)	$ V_{CM}  = 10\text{ V}$ , $V_{CC} = 5\text{ V}$ , $I_F = 7.5\text{ mA}$ , $V_{O(\max)} = 0.8\text{ V}$ , $R_L = 350\ \Omega$ , $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ (1)	$ CM_L $	-	10 000	-	$\text{V}/\mu\text{s}$
	$ V_{CM}  = 50\text{ V}$ , $V_{CC} = 5\text{ V}$ , $I_F = 7.5\text{ mA}$ , $V_{O(\max)} = 0.8\text{ V}$ , $R_L = 350\ \Omega$ , $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ (2)	$ CM_L $	5000	10 000	-	$\text{V}/\mu\text{s}$
	$ V_{CM}  = 1\text{ kV}$ , $V_{CC} = 5\text{ V}$ , $I_F = 7.5\text{ mA}$ , $V_{O(\max)} = 0.8\text{ V}$ , $R_L = 350\ \Omega$ , $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ (3)	$ CM_L $	10 000	15 000	-	$\text{V}/\mu\text{s}$

**Notes**

- (1) For SFH6755
- (2) For SFH6756
- (3) For SFH6747 and SFH6757

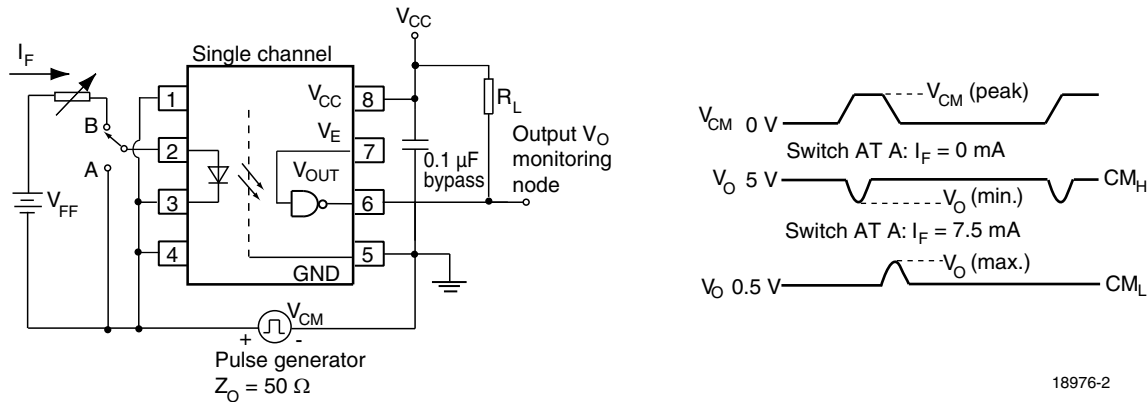


Fig. 4 - Single Channel Test Circuit for Common Mode Transient Immunity

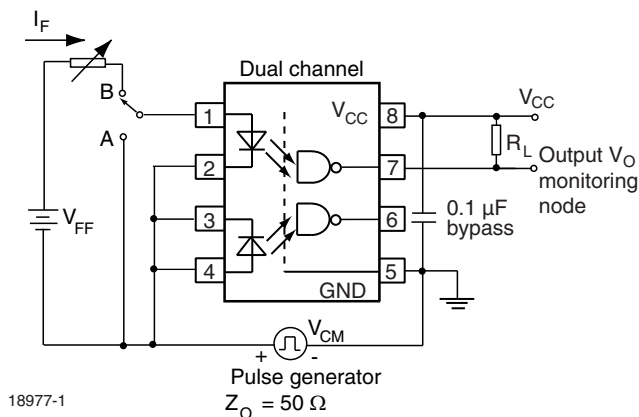


Fig. 5 - Dual Channel Test Circuit for Common Mode Transient Immunity



SAFETY AND INSULATION RATINGS						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Climatic classification	According to IEC 68 part 1		-	55 / 100 / 21	-	
Comparative tracking index		CTI	175	-	399	
P <sub>SO</sub>			-	-	350	mW
I <sub>SI</sub>			-	-	150	mA
T <sub>SI</sub>			-	-	165	°C
Creepage			4	-	-	mm
Clearance			4	-	-	mm
Insulation thickness			0.2	-	-	mm

**Note**

- As per IEC 60747-5-5, 7.4.3.8.1, this optocoupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of protective circuits.

**TYPICAL CHARACTERISTICS** (T<sub>amb</sub> = 25 °C, unless otherwise specified)

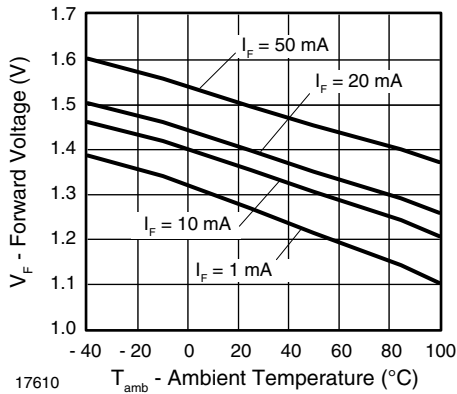


Fig. 6 - Forward Voltage vs. Ambient Temperature

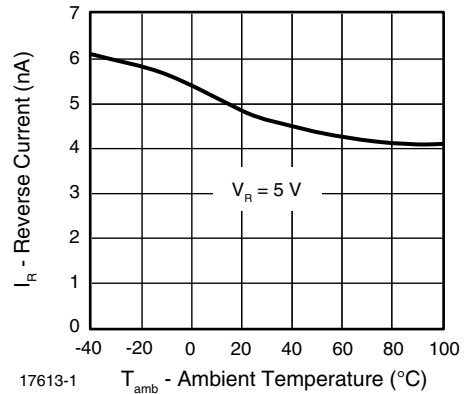


Fig. 8 - Reverse Current vs. Ambient Temperature

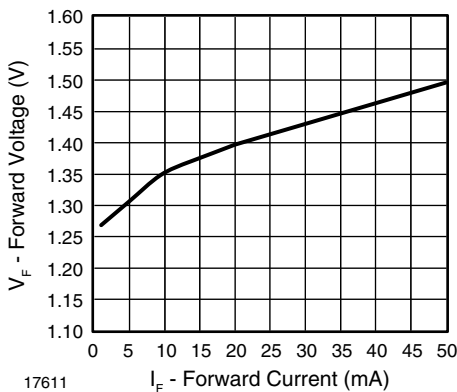


Fig. 7 - Forward Voltage vs. Forward Current

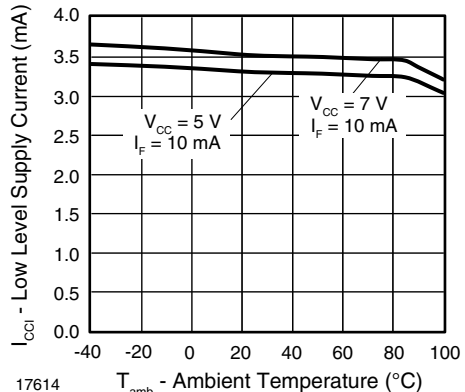


Fig. 9 - Low Level Supply Current vs. Ambient Temperature

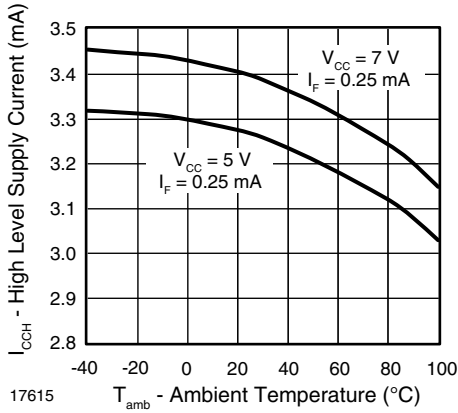


Fig. 10 - High Level Supply Current vs. Ambient Temperature

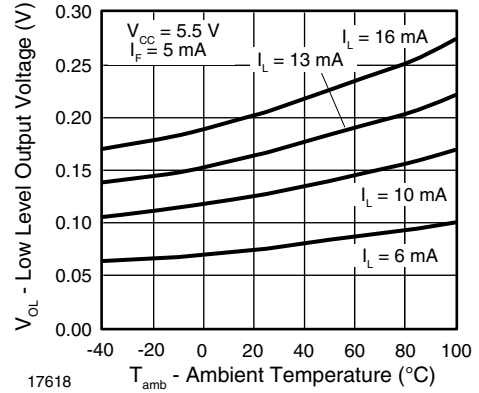


Fig. 13 - Low Level Output Voltage vs. Ambient Temperature

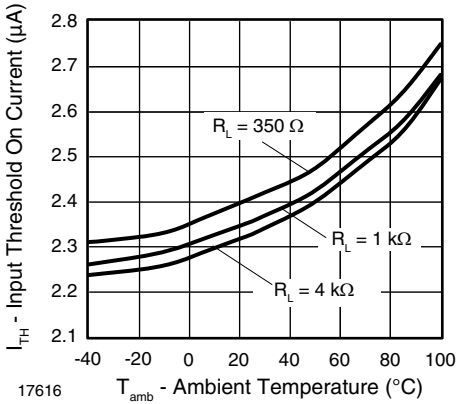


Fig. 11 - Input Threshold On Current vs. Ambient Temperature

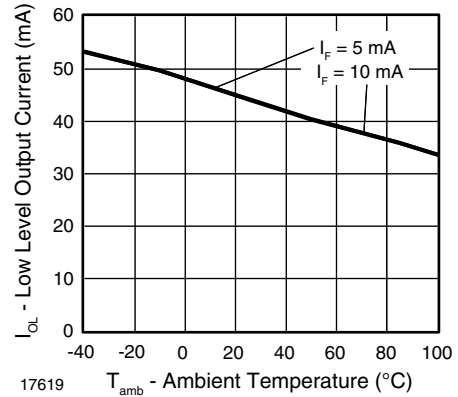


Fig. 14 - Low Level Output Current vs. Ambient Temperature

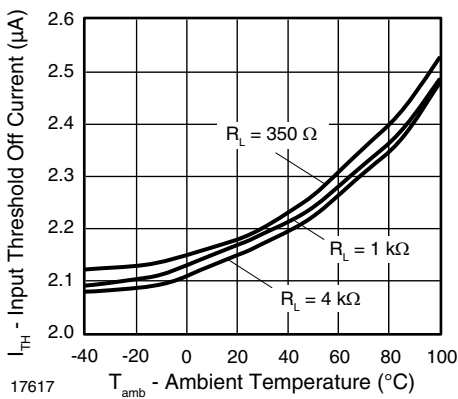


Fig. 12 - Input Threshold Off Current vs. Ambient Temperature

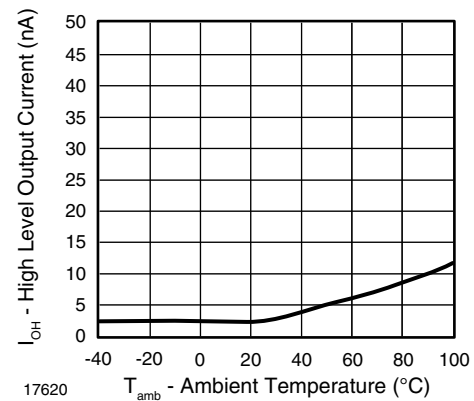


Fig. 15 - High Level Output Current vs. Ambient Temperature

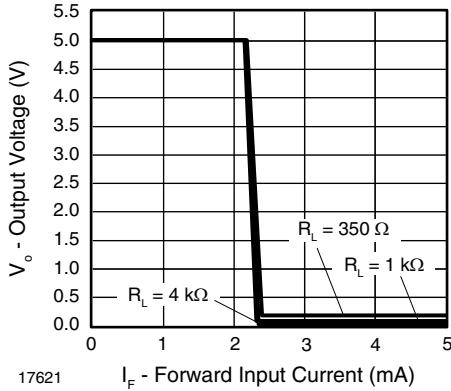


Fig. 16 - Output Voltage vs. Forward Input Current

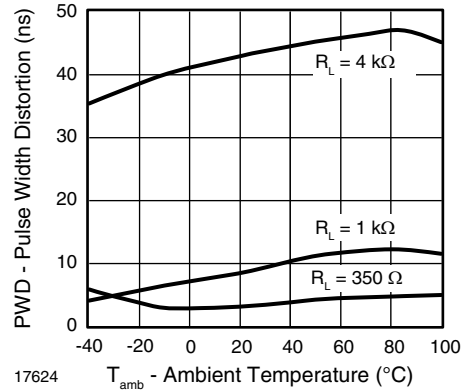


Fig. 19 - Pulse Width Distortion vs. Ambient Temperature

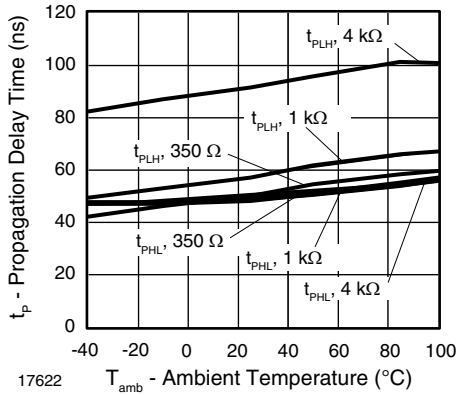


Fig. 17 - Propagation Delay vs. Ambient Temperature

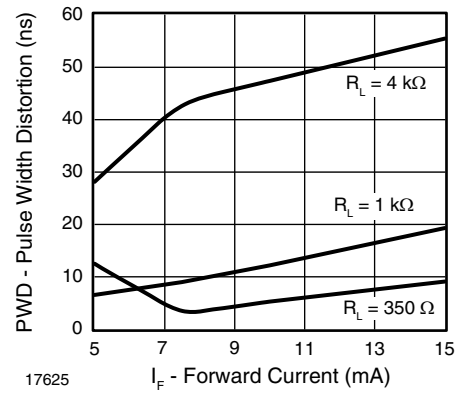


Fig. 20 - Pulse Width Distortion vs. Forward Current

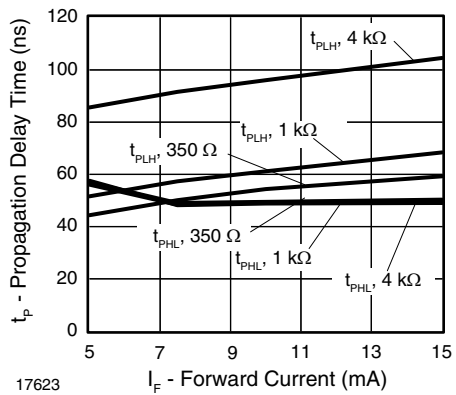


Fig. 18 - Propagation Delay vs. Forward Current

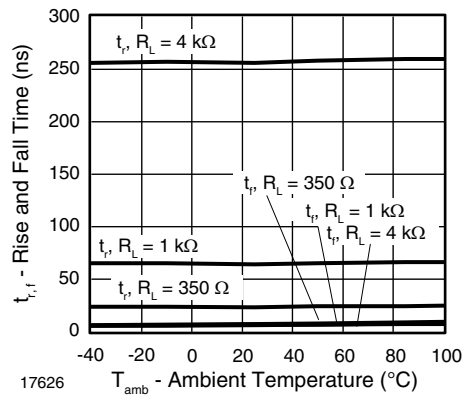


Fig. 21 - Rise and Fall Time vs. Ambient Temperature



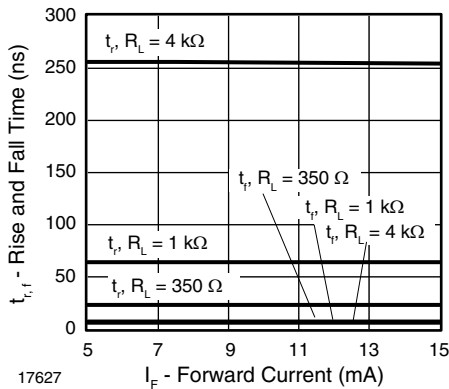


Fig. 22 - Rise and Fall Time vs. Forward Current

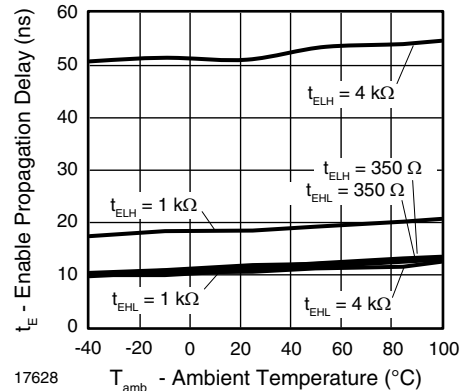
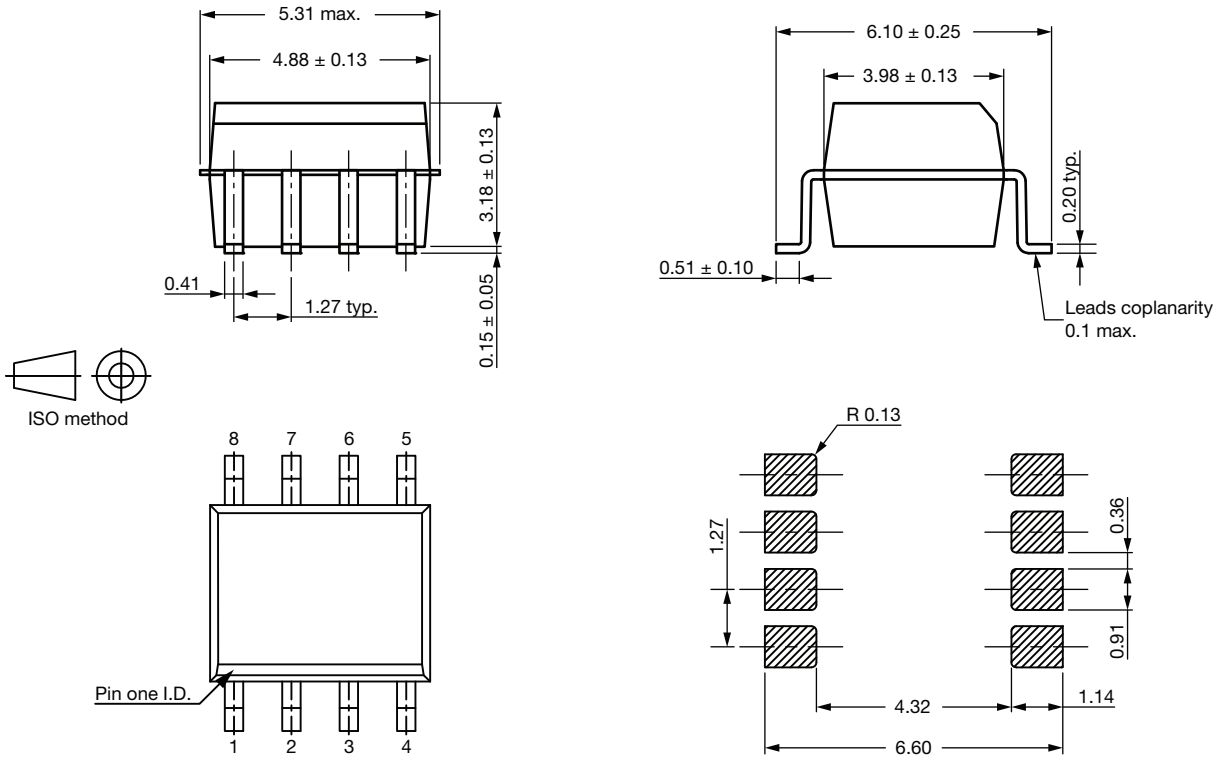


Fig. 23 - Enable Propagation Delay vs. Ambient Temperature

**PACKAGE DIMENSIONS (in millimeters)**





## PACKAGE MARKING (example of SFH6755T)

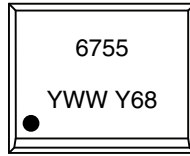


Fig. 24 - SFH6755T

### Notes

- VDE logo is only marked on option 1 parts.
- Tape and reel suffix (T) is not part of the package marking.

## SOLDER PROFILES

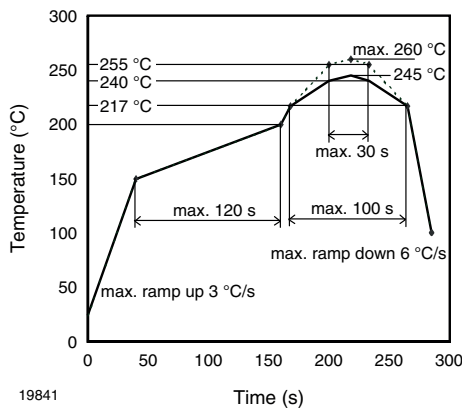


Fig. 25 - Lead (Pb)-Free Reflow Solder Profile According to J-STD-020 for SMD Devices

## HANDLING AND STORAGE CONDITIONS

ESD level: HBM class 2

Floor life: unlimited

Conditions:  $T_{amb} < 30\text{ °C}$ ,  $RH < 85\%$

Moisture sensitivity level 1, according to J-STD-020

### ESD CAUTION

This is an ESD (electro static discharge) sensitive device. Electrostatic charges accumulate on the human body and test equipment and can discharge without detection. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality. ESD withstand voltage of this device is up to 1500 V according to JESD22-A114-B.



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