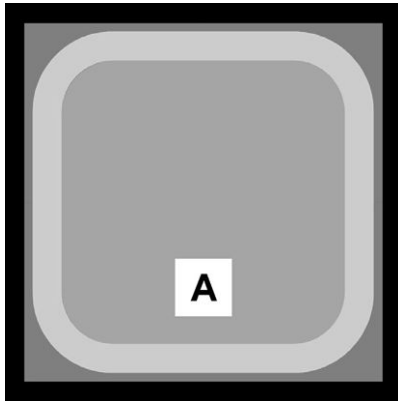


## Silicon PIN Photodiode



### DESCRIPTION

T330P chip is a PIN photodiode with 0.23 mm<sup>2</sup> sensitive area, high speed and high photo sensitivity. It is sensitive to the visible and near infrared light spectrum with a peak sensitivity at 900 nm. Anode is the bond pad on top, cathode is the backside contact.

### GENERAL INFORMATION

The datasheet is based on Vishay optoelectronics sample testing under certain predetermined and assumed conditions, and is provided for illustration purpose only. Customers are encouraged to perform testing in actual proposed packaged and used conditions. Vishay optoelectronics die products are tested using Vishay optoelectronics based quality assurance procedures and are manufactured using Vishay optoelectronics established processes. Estimates such as those described and set forth in this datasheet for semiconductor die will vary depending on a number of packaging, handling, use, and other factors. Therefore sold die may not perform on an equivalent basis to standard package products.

### FEATURES

- Package type: chip
- Package form: single chip
- Dimensions (L x W x H in mm): 0.67 x 0.67 x 0.28
- Wafer diameter (in mm): 100
- Radiant sensitive area (in mm<sup>2</sup>): 0.23
- Peak sensitivity wavelength: 900 nm
- High photo sensitivity
- High radiant sensitivity
- Suitable for visible light and near infrared radiation
- Fast response times
- Angle of half sensitivity:  $\phi = \pm 60^\circ$
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



### APPLICATIONS

- High speed photo detector

### PRODUCT SUMMARY

COMPONENT	$I_{ra}$ ( $\mu A$ )	$\phi$ (deg)	$\lambda_{0.1}$ (nm)
T330P	2.3	$\pm 60$	430 to 1100

#### Note

- Test conditions see table "Basic Characteristics"

### ORDERING INFORMATION

ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
T330P-SD-F	Wafer sawn on foil with disco frame	MOQ: 55 000 pcs	Chip

#### Note

- MOQ: minimum order quantity

### ABSOLUTE MAXIMUM RATINGS ( $T_{amb} = 25^\circ C$ , unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Reverse voltage		$V_R$	60	V
Junction temperature		$T_j$	100	$^\circ C$
Operating temperature range		$T_{amb}$	-40 to +100	$^\circ C$
Storage temperature range		$T_{stg1}$	-40 to +100	$^\circ C$
Storage temperature range on foil		$T_{stg2}$	-40 to +50	$^\circ C$

<b>BASIC CHARACTERISTICS</b> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Breakdown voltage	$I_R = 100\text{ }\mu\text{A}$ , $E = 0$	$V_{(BR)}$	60			V
Reverse dark current	$V_R = 10\text{ V}$ , $E = 0$	$I_{ro}$		0.1	3	nA
Diode capacitance	$V_R = 5\text{ V}$ , $f = 1\text{ MHz}$ , $E = 0$	$C_D$		1.3		pF
Reverse light current	$E_e = 1\text{ mW/cm}^2$ , $\lambda = 950\text{ nm}$ , $V_R = 5\text{ V}$	$I_{ra}$		2.3		$\mu\text{A}$
Angle of half sensitivity		$\varphi$		$\pm 60$		deg
Wavelength of peak sensitivity		$\lambda_p$		900		nm
Range of spectral bandwidth		$\lambda_{0.1}$		430 to 1100		nm
Rise time	$V_R = 10\text{ V}$ , $R_L = 50\text{ }\Omega$ , $\lambda = 820\text{ nm}$	$t_r$		4		ns
Fall time	$V_R = 10\text{ V}$ , $R_L = 50\text{ }\Omega$ , $\lambda = 820\text{ nm}$	$t_f$		4		ns

**Note**

- The measurements are based on samples of die which are mounted on a TO-header without resin coating

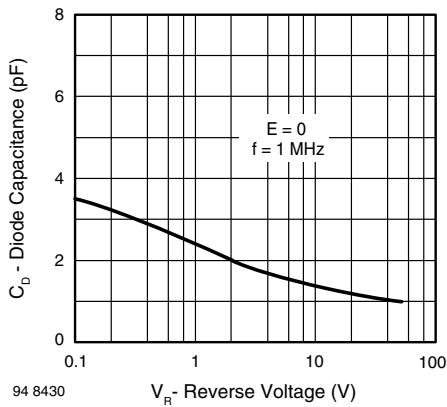
**BASIC CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)


Fig. 1 - Diode Capacitance vs. Reverse Voltage

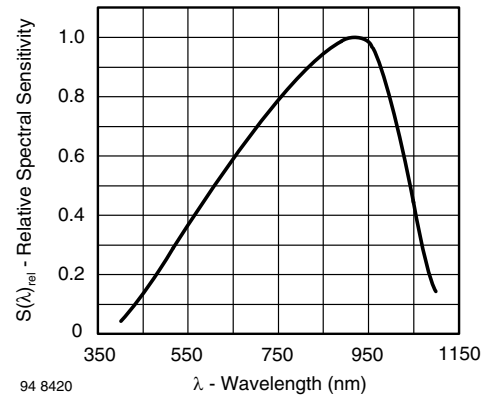


Fig. 2 - Relative Spectral Sensitivity vs. Wavelength

<b>MECHANICAL DIMENSIONS</b>					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Length of chip edge (x-direction)	$L_x$		0.67		mm
Length of chip edge (y-direction)	$L_y$		0.67		mm
Sensitive area	$A_S$		0.23		$\text{mm}^2$
Wafer diameter	D		100		mm
Die height	H	0.265	0.28	0.295	mm
Bond pad anode	$x * y$		0.1 x 0.1		$\text{mm}^2$

<b>ADDITIONAL INFORMATION</b>	
Frontside metallization, anode	AlSi
Backside metallization, cathode	NiV-Ag
Dicing	Sawing
Die bonding technology	Epoxy bonding

**Note**

- All chips are checked in accordance with the Vishay Semiconductor, specification of visual inspection FVOV6870. The visual inspection shall be made in accordance with the "specification of visual inspection as referenced". The visual inspection of chip backside is performed with stereo microscope with incident light and 40x to 80x magnification. The quality inspection (final visual inspection) is performed by production. An additional visual inspection step as special release procedure by QM is not installed.



**HANDLING AND STORAGE CONDITIONS**

- The hermetically sealed shipment lots shall be opened in temperature and moisture controlled cleanroom environment only. It is mandatory to follow the rules for disposition of material that can be hazardous for humans and environment.
- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Singulated die are not to be handled with tweezers. A vacuum wand with non metallic ESD protected tip should be used.

**PACKING**

Chips are fixed on adhesive foil. Upon request the foils can be mounted on plastic frame or disco frame. For shipment, the wafers are arranged to stacks and hermetically sealed in plastic bags to ensure protection against environmental influence (humidity and contamination).

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