INTRODUCTION

The new SFH67XX series of high-speed optocouplers is capable of transmitting data rates up to 5 Mb/s typical and 2.5 Mb/s over the full specified operating temperature range. The combination of low input current (1.6 mA) and active logic-level output is a fit for nearly all logic applications where a galvanic insulation is necessary.

The SFH67XX series features positive logic with TTL output levels. For improved noise immunity the detector incorporates a schmitt-trigger stage.

The SFH6700/19 provides an enable input, which allows switching the output into the high ohmic state for bus applications.

For applications which need an open collector output, the SFH6705 is offered. The SFH6731 and SFH6732 are the dual versions. The two channels are free of crosstalk and interference. To ensure a high common mode transient immunity of guaranteed 2.5 kV/μs at 400 V, the SFH671X/6732 series features an internal shield which consists of an additional ITO layer. The ITO (indium tin oxide) layer is an optically transparent but electrically conductive layer on top of the detector. The standard SFH670X series withstands 1.0 kV/μs at VCM = 50 V.

The SFH67XX series is also available in an SMD version (option 7 and 9 with > 8 mm creepage and clearance distance).

![Fig. 1 - Variations in the SFH67XX Family](image)

| TABLE 1 |
|----------|----------|----------|
| LED      | ENABLE   | OUTPUT   |
| SFH6700/19 |          |          |
| On       | L        | H        |
| Off      | L        | L        |
| On       | H        | Z        |
| Off      | H        | Z        |
| SFH6701/02/05/11/12/31/32 |          |          |
| On       |          | H        |
| Off      |          | L        |

Truth table (positive logic)

H = logic high level, L = logic low level, Z = high ohmic state

DESIGN CONSIDERATIONS

The circuits shown below are intended to give the design engineer a guideline for logic family interconnection.

Input Circuitry

Below are stated the most common interface circuits which work for this coupler series.

Totem Pole Drive Circuits

Figures 2 and 3 are two of the most commonly used circuits. The designer chooses R1 according to the equation:

\[ R_1 = \frac{V_{OH} - V_F}{I_F} \]  

(valid for figure 2) (1)
High-Speed/Logic Gate Optocoupler (SFH67XX Series)

\[ R_1 = \frac{V_{DD} - V_{OL} - V_F}{I_F} \]  
(valid for figure 3)  
\[ (2) \]

A good compromise between low power dissipation and symmetrical propagation delays with respect to some guard band is \( I_F = 3 \) mA. In some applications a speed-up capacitor (typically around 100 pF) across \( R_1 \) may be used to achieve faster switching times (please refer to the end of this section for details).

Due to the coupler’s typically low input current threshold of 0.50 mA and the negative temperature gradient of the input current threshold (see figure 4), the output leakage current of the driver element at high temperatures may become an issue in certain applications where the circuit is operated at the upper temperature range.

For critical applications, where a high leakage current is expected, a shunt LED circuit, as shown in figure 5, is a good solution.

The resistor \( R_1 \) determines the forward LED current, and \( R_2 \) shunts the LED. The choice of \( R_2 \) depends on power dissipation considerations and the expected leakage current. The following equations can help designers determine the appropriate resistor values:

\[ R_2 = \frac{V_{F\max(LEDoff)}}{I_{\text{Leak at Temp}}} \cdot \frac{1}{I_{\text{Leakage}}} \]  
\[ (3) \]

\[ R_1 = \frac{V_{DD} - V_F - V_{OL}}{V_F + I_F R_2} \cdot R_2 \]  
\[ (4) \]

**TABLE 2**

<table>
<thead>
<tr>
<th>FIGURE</th>
<th>LOGIC GATE (E.G.)</th>
<th>( R_1 ) VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>74LS04</td>
<td>750 ( \Omega )</td>
</tr>
<tr>
<td>3</td>
<td>74LS04</td>
<td>1.10 k( \Omega )</td>
</tr>
<tr>
<td></td>
<td>74HC04</td>
<td>1.10 k( \Omega )</td>
</tr>
</tbody>
</table>

Typical values for \( R_1 \) at \( V_{DD} = 5 \)

Both circuits are simple and feature a minimal component count with low power dissipation. A logic source drive, as shown in figure 2, is not recommended due to speed and current limitations (especially in the CMOS logic family), and lower common mode transient immunity.
Typical input circuit values to shunt around 250 μA away from the LED (according to figure 5).

A better way to handle leakage current is presented in figure 6.

This circuit provides excellent speed properties and leakage current protection. The silicon diode D1 ensures that the current is only sourced by VDD and is therefore not required for units driven by an open collector or open drain. The low forward voltage of D1 ensures that the LED stays off at logic low. The equation to choose R1 is:

\[ R_1 = \frac{V_{DD} - V_F}{I_F} \] (5)

TABLE 3

<table>
<thead>
<tr>
<th>VDD</th>
<th>I_F</th>
<th>R1 VALUE</th>
<th>R2 VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 V</td>
<td>3 mA</td>
<td>1.0 kΩ</td>
<td>4.7 kΩ</td>
</tr>
</tbody>
</table>

Open Collector Drive Circuits

A simple circuit, which also works for open collector drive circuits, has been presented in figures 3 and 5. In figure 5, the resistor R2 represents a leakage current protection path.

A more efficient but more power-dissipating solution is presented in figure 7. This drive circuit provides good speed and protection against leakage currents. The resistor R1 is chosen in accordance with

\[ R_1 = \frac{V_{DD} - V_F}{I_F} \] (6)

Refer to table 4 for some typical resistor values.

Note that leakage protection generally might only be an issue in some special applications.

Typical input circuit values for a circuit according to figure 7

Input Circuitry for Improved Switching Speeds

If switching speed is a concern, the use of a speed-up capacitor is a good solution. The resistor R2 limits the peak transient current I_{Fpeak}, whereas R1 and R2 determine the current at steady-state operation. The equations and reasonable resistor values are printed below.

A reasonable value for the speed-up capacitor C_S is 100 pF.

The equations for the resistor values are:

\[ R_1 = \frac{V_{DD} - V_{OL} - V_F}{I_{Fpeak}} \] (7)

\[ R_1 = \frac{V_{DD} - V_{OL} - V_F}{I_F} - R_2 \] (8)

The maximum I_{Fpeak} for this transient is 50 mA for the SFH67XX series.

TABLE 4

<table>
<thead>
<tr>
<th>VDD</th>
<th>I_F</th>
<th>R1 VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 V</td>
<td>3 mA</td>
<td>1.10 kΩ</td>
</tr>
<tr>
<td>10 V</td>
<td>3 mA</td>
<td>2.80 kΩ</td>
</tr>
<tr>
<td>15 V</td>
<td>3 mA</td>
<td>4.42 kΩ</td>
</tr>
</tbody>
</table>

Typical input circuit values for a circuit according to figure 7.
Typical input circuit values for a circuit according to figure 8

**Output Circuitry**

One advantage of the SFH67XX series is its easy connection to any logic system, because of the active output stage (totem pole/three state output). Either directly or via a pull-up resistor, all couplers can drive up to 16 LS TTL loads (4 TTL loads) easily. In general, a 0.1 μF bypass capacitor is strongly recommended for proper operation.

The SFH6700/19 with its three-state output fits best in bus applications because of the possibility to switch the couplers output into the high ohmic state (for a typical setup please refer to figure 28).

**Drive Circuits for the Dual-Channel Devices**

The SFH6731/32 can be driven as simply as the single channel devices.

All the above drive circuits and equations (1) to (8) can be adapted to drive the dual-channel devices. (The use of the dual-channel devices reduces the number of parts and the required board space.)

**Interfacing to TTL/TTL-Compatible Logic**

Interfacing the SFH67XX coupler to LS TTL or any other compatible logic is quite simple. The active output of this coupler eliminates the need for an external pull up resistor, and minimizes parts count and board space requirements. The typical connection is seen in figure 9. Even HCT logic can be interfaced this way.

**Interfacing to CMOS Logic**

To ensure reliable logic switching, a pull-up resistor between the output and \( V_{CC} \) is recommended (see Figures 11 and 12). For the HCT logic family, this pull-up resistor may be omitted, due to the matching switching level of the coupler’s output and the HCT input.

There are three simple ways to connect CMOS logic to the SFH67XX coupler family:

- Using SFH67XX (totem pole) and a pull-up resistor (see figure 12)
- Using SFH6705 (open collector) and a pull-up resistor (see figure 11)
- Using an HCT logic device (see figure 10)

Using an HCT device is the simplest and most convenient solution to eliminate the external pull-up resistor (see figure 10). The designer doesn’t have to worry about power consumption, rise times, or system speed.

### TABLE 5

<table>
<thead>
<tr>
<th>( V_{DD} )</th>
<th>( C_2 ) VALUE</th>
<th>( R_1 ) VALUE</th>
<th>( R_2 ) VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 V</td>
<td>100 pF</td>
<td>1.0 kΩ</td>
<td>75 Ω</td>
</tr>
</tbody>
</table>

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Using the open collector device, as in figure 11, requires an external pull-up resistor \( R_P \). To determine the correct value of this pull-up resistor, use following equations:

\[
R_{P_{\text{min}}} = \frac{V_{CC_{\text{max}}} - V_{OL_{\text{min}}}}{I_{OL_{\text{max}}} + n \cdot I_{IL}}
\]  

where \( n \cdot I_{IL} \) represents the total load current at low level \( V_{OL} \). (To ensure \( V_{OL_{\text{max}}} < 0.5 \) V over temperature \( I_{OL_{\text{max}}} \) should be set not higher than 6.4 mA).

The maximum \( R_P \) value can be determined by:

\[
R_{P_{\text{max}}} = \frac{V_{CC_{\text{min}}} - V_{IH_{\text{min}}}}{I_{OH_{\text{max}}} + n \cdot I_{IH}}
\]

In CMOS applications however, where \( I_{IH} \) is in the μA region, the limiting factor can also be determined by the maximum allowable rise time \( t_r \) (500 ns for HC logic). The equation

\[
V_H = V_{CC} \left( 1 - e^{-\frac{t_r}{R_PC_L}} \right)
\]

leads to

\[
R_{P_{\text{max}}} = \frac{-t_r}{C_L \cdot 1n\left( 1 - \frac{V_{IH_{\text{min}}}}{V_{CC_{\text{min}}}} \right)}
\]
in which $C_L$ represents the total capacitance of the load, including the coupler (which is around 6 pF).

The resistor value is a compromise between the requirement of power dissipation and switching speed. A low $R_P$ produces symmetrical and fast switching times but results in a higher power dissipation. Reasonable values are shown in table 6.

Details of the relationship between the rise time $t_r$ and the pull-up resistor $R_P$/load capacitance $C_L$ are shown in figure 14.

Note that generally the $R_P$ value has a negligible influence on the delay time $t_d$, but it strongly determines the rise time, especially for the open collector type.

**Interfacing to 3.3 V Level**

Interfacing to the 3.3 V logic families (e.g. AC, AHC, or HC) is quite easy, and presented in figure 13.

If the totem pole/three-state coupler is operated with $V_{CC} = 5$ V, then the output “high” level of the coupler, which is then typically 3.2 V, matches perfectly with the 3.3 V logic input levels. In general, the output “high” voltage can be determined by $V_{OH} = V_{CC} - 1.8$ V. (Even with $V_{CC} = 5.0$ V ± 10 %, the output voltage is within the limits, and is guaranteed to be higher than 2.4 V over temperature to fulfill the 3 V logic requirement).

**Interfacing to other Levels**

If shifting to any other level is intended (e.g. 2.5 V logic, like the ALVC or ALVT series), the SFH6705 with its open collector output is qualified. $R_P$ works as a pull-up resistor to ensure the proper logic high level. The basic principles are the same as described in the section “interfacing to CMOS logic” in equations (9) to (12).

**Pull-Up Resistor Considerations for the Open Collector Type SFH6705**

As previously mentioned above, the pull-up resistor has to be chosen in accordance with the equations (9), (10), and (12). Figure 14 plots the expected rise time $t_r$ versus the time constant $\tau = R_P \times C_L$. Unlike the rise time $t_r$, the fall time $t_f$ is mostly independent of $R_P$ and around 5 ns.

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**TABLE 6**

<table>
<thead>
<tr>
<th>$V_{CC}$</th>
<th>$R_P$ (OPEN COLLECTOR)</th>
<th>$R_P$ (TOTEM POLE)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 V</td>
<td>820 Ω</td>
<td>1.10 kΩ</td>
</tr>
</tbody>
</table>

Typical values for $R_P$ by connecting to CMOS logic (according to figures 11 and 12).
Common-Mode Transient Immunity (CMTI)

The SFH6711/12/19 feature a guaranteed common mode transient immunity (CMTI) of 2.5 kV/μs at 400 V. This is achieved by using a faraday shield which is transparent to infrared light, but electrically conducting. This shield prevents the photodiode from being turned on by common-mode transients.

In general there are some design rules to achieve a high CMTI. These recommendations are especially important for low LED drive current devices, like the SFH67XX series:

- Connect the unused pins 1 and 4 to the virtually grounded input potential (either GND or VDD).
- Minimize stray capacitance.
- Avoid long distances between LED input circuit and coupler.
- Choose an appropriate high LED forward current to improve CMH (common mode transient immunity at logic “high” level).

A layout which implements these hints is seen in figure 16. Note that this layout reduces creepage and clearance distance as well.

A circuit which enhances CMTI safety is shown in figure 17. The diode D1 is intended to sink parasitic current, which is caused by stray capacitance, away from the LED to prevent a false turn-on.

* Diode D1: Any signaling diode

Another input circuit for high CMTI is shown in figure 18. The transistor shunts the LED in the off-state and prevents a false turn on. This circuit tolerates very high common mode transients in the LED off-state. An improvement in the LED on-state can be reached by choosing a high IF current. For VDD = 5 V, R1 is typically around 1.1 kΩ.
A common way to achieve ultra-high CMTI is presented in figure 19. The balanced input impedance principle works with four resistors, $R_1 = R_2$ and $R_3 = R_4$. $R_1$ and $R_2$ are used to minimize any noticeable LED current when the transistor is on. To achieve maximum performance, the stray capacitance from anode or cathode to the output side of the coupler has to be kept as low as possible.

Reasonable values with $Q_1 = 2N2222$ are $R_3 = R_4 = 510 \, \Omega$ and $R_1 = R_2$ omitted. Note that $R_1$ and $R_2$ can be omitted, depending on the $V_{CE}$ of the transistor $Q_1$.

**Pulse Width Distortion**

Pulse width distortion (PWD) is defined as the difference between $t_{PHL}$ and $t_{PLH}$ ($PWD = |t_{PHL} - t_{PLH}|$). This value is important in applications where symmetrical switching times are required, e.g., in systems which are based on pulse width modulation. In transmission systems, the PWD should not exceed 30% of the minimum propagation delay time. At $I_F = 3.0 \, mA$ LED forward current, the SFH67xx has a typical PWD of around 20 ns over temperature, which corresponds to a maximum PWD of 20%. Note that the use of a speed up capacitor decreases $t_{PLH}$ but might increase the PWD.

**Propagation Delay Skew**

Propagation delay skew ($t_{PSK}$) is the difference between the minimum propagation delay, either $t_{PHL}$ or $t_{PLH}$, and the maximum propagation delay, either $t_{PLH}$ or $t_{PHL}$, between any SFH67XX coupler under the same operation conditions. Propagation delay skew is therefore an important value for parallel data transmission, where synchronized data is needed.
High-Speed/Logic Gate Optocoupler (SFH67XX Series)

In logic circuits, the overall PWD and $t_{PSK}$ are determined by all input and output logic gates in the signal path. To minimize the overall PWD, two identical couplers may be used as shown in figure 22. But the minimum PWD is achieved at the cost of a higher overall propagation delay.

**Eye Pattern Diagram**
A typical eye pattern diagram for 5 Mb/s data transmission is presented in figure 23. The eye pattern testing was done with a pseudo random data sequence (NRZ coding).

**DESIGN IDEAS**
Optocouplers are commonly used as an interface between two circuits, where galvanic insulation is required, either to protect humans or sensitive electronic equipment. Based on this requirement, some designs are presented below, which use the SFH67XX series.

**IGBT/IPM Driver**
The SFH67XX series can be used as a fast driver for intelligent power modules (IPMs) using IGBT or MOSFET technology. The SFH67XX optocoupler series provide level shifting and galvanic insulation and is therefore the ideal interface to the control logic. With its guaranteed minimum 2.5 kV/μs at 400 V common mode transient immunity, the SFH671X also fulfills enhanced switching requirements.

**Switching Loads**
The SFH67XX series can easily handle currents up to 25 mA$_{DC}$ and voltages up to 15 V. Figures 26 and 27 show how it can handle loads which are beyond these limits. In figure 26, R$_1$ is used as a pull-up resistor and the load current is handled and limited by the external transistor Q$_1$. Unlike figure 27, the schematic in figure 26 is qualified to support both high voltages and currents. The 5 V power supply might be raised up to 15 V to achieve a proper $V_{GS}$ voltage to turn the transistor fully on.

The combination of the SFH67XX series with logic level power transistors provides a fast-switching solution that helps to reduce parts count.
High-Speed/Logic Gate Optocoupler (SFH67XX Series)

Time Multiplexed Bus Line Access with Optical Insulation Barrier
The schematic in figure 28 shows the use of a common data bus line with 4 independent data lines in time multiplexing mode. The 2-line to 4-line address decoder selects one of the 4 data lines by enabling the output, whereas all the other outputs remain in the high ohmic state.

Opto-Insulated DAC Interface
When galvanic insulation in digital-to-analog-conversion or analog-to-digital-conversion systems is required, the SFH67XX series is a good choice for an interface.

Setups like the one in figure 29 provide a fast and part saving insulation barrier. The low propagation delay skew of the SFH67XX devices makes them ideal for use in parallel data transfer. The SFH67XX series provide an optimal interface solution for the SAB 80 C167/C165 micro-controllers by supporting the 5 Mb/s data rate at a 20 MHz CPU clock.

* Transistor Q1: Any n-channel enhancement-mode transistor
** Resistor R1: R1 might be omitted, depending on the necessary VGS of Q1 to turn Q1 fully on
High-Speed/Logic Gate Optocoupler (SFH67XX Series)

Fig. 28 - Typical Setup for a Common Bus Line with 4 Different Lines in Time Multiplex Mode

<table>
<thead>
<tr>
<th>Select Inputs</th>
<th>Enable</th>
<th>G</th>
<th>B</th>
<th>A</th>
<th>Active on Bus Line</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>None (all high ohmic)</td>
</tr>
<tr>
<td>Y1 74HCT139</td>
<td>Y2</td>
<td></td>
<td></td>
<td></td>
<td>Data Line 1</td>
</tr>
<tr>
<td>Y3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Data Line 2</td>
</tr>
</tbody>
</table>

<p>| | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td></td>
<td>Data Line 1</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td></td>
<td></td>
<td>Data Line 2</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td></td>
<td></td>
<td>Data Line 3</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td></td>
<td></td>
<td>Data Line 4</td>
<td></td>
</tr>
</tbody>
</table>
Fig. 29 - Fully Galvanic Insulated Digital-to-Analog-Conversion System (4 Channel DAC)

* Inverter 74HCT04 is used to allow 3 mA LED current

** Any C16X micro-controller can be used