High Speed Optocoupler, 10 MBd

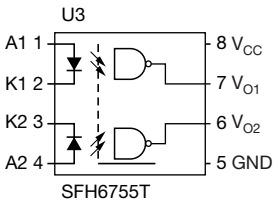
DESCRIPTION

This 10 MBd family is an industry standard optocoupler, utilizing a high efficient input LED coupled with an integrated optical photodiode IC detector. The detector output is open drain NMOS-transistor.

The SFH6755T, SFH6756T, SFH6757T are dual channel without enable pin.

Their PSpice models are written from device characterization data for simulation. All symbols are in the symbol library file SFH6755T.olb. All model data are in the PSpice model library file SFH6755T.lib.

This document is intended as a PSpice modeling guideline and does not constitute a commercial product, neither a substitute to datasheet.

PART	MODEL DESCRIPTION	SYMBOL FILE	MODEL FILE
SFH6755T	Dual channel high speed, 10 MBd	 SFH6755T.olb	SFH6755T.lib

RECOMMENDED USE OF THE MODEL

- This model is designed only for use at 25 °C and should be used as is.
- This model has been created and tested with OrCAD version 16.6.
- The olb file (symbol) is not down-compatible. Users of the earlier versions need to create the symbols on their platform and associate with relative PSpice model data.

TRUTH TABLE (positive logic)

LED	ENABLE (V_E)	OUTPUT (V_O)
On	H	L
Off	H	H
On	L	H
Off	L	H
On	NC	L
Off	NC	H

NETLIST OF MODEL

Following list shows the netlist of the model:

```
**************************************************
* Library of 10MBd HighSpeed Optocoupler SFH6755T
* Copyright VISHAY, Inc. 2016 All Rights Reserved.
**************************************************
**************************************************
** PSpice Models of Vishay optocouplers
** High speed 10 MBd
** SFH6755T, SFH6756T, SFH6757T
**************************************************
**************************************************
**  dual channel, NMOS output
**  --  SFH6755T, SFH6756T, SFH6757T ---
**************************************************
**
** Model Node - Symbol - Pin
** 1 (A1)       A1        1
** 2 (K1)       C1        2
** 3 (K2)       C2        3
** 4 (A2)       A2        4
** 5 (GND)      GND       5
** 6 (VO2)      VO2       6
** 7 (VO1)      VO1       7
** 8 (VCC)      VCC       8
**
.SUBCKT SFH6755T A1 K1 K2 A2 GND VO2 VO1 VCC
** CHANNEL 1 **
DD1 A1 61        DEMIT
vV1 61 K1  DC 0
wW1  VCC 71  vV1  I_SW1
rR13  71 GND  1K
xU11 71  81 $G_DPWR $G_DGND BUF
rR41  81  91 5K
MQ11 VO1 91 GND GND MOST1 W=9.7M L=2U  ;NMOS OUTPUT
** CHANNEL 2 **
DD2 A2 62        DEMIT
vV2 62 K2  DC 0
wW2  VCC 72  vV2  I_SW1
rR23  72 GND  1K
xU12 72  82 $G_DPWR $G_DGND BUF
rR24  82  92 5K
MQ1 VO2 92 GND GND MOST1 W=9.7M L=2U  ;NMOS OUTPUT
**
.MODEL    DEMIT   D
+IS=1.69341E-12 RS=2.5 N=2.4  XTI=4
+EG=1.52436 CJO=1.80001E-11 VJ=0.75 M=0.5 FC=0.5
.MODEL MOST1 NMOS (LEVEL=3 KP=25U VTO=2 RD=45)
.MODEL I_SW1 ISWITCH (Roff=1e6 Ron=1 IT=4.9m IH=0.1m TD=20ns)
.ENDS
*$
**$
```

```
***-------------------------------------------------------------------
**  1 INPUT BUFFER
**
.SUBCKT BUF  I0  O  optional: DPWR=$G_DPWR DGND=$G_DGND
U1 BUF DPWR  DGND I0  O
+  D_PLD_GATE IO_PLD
.ENDS
*$
***-------------------------------------------------------------------
**  1 INPUT INVERTER
**
.SUBCKT INV  I0  O  optional: DPWR=$G_DPWR DGND=$G_DGND
*
U1 INV DPWR  DGND I0  O
+  D_PLD_GATE IO_PLD
*
.ENDS
*$
***-------------------------------------------------------------------
** ENABLE HIGH BUFFER WITH TRI-STATE OUTPUT
**
.SUBCKT BUFTH  I0 OE  O  optional: DPWR=$G_DPWR DGND=$G_DGND
U1 BUF3  DPWR  DGND I0 OE  O
+  D_PLD_TGATE IO_PLD
.ENDS
*$
***-------------------------------------------------------------------
** ENABLE LOW BUFFER WITH TRI-STATE OUTPUT
**
.SUBCKT BUFTL  I0 OE  O optional: DPWR=$G_DPWR DGND=$G_DGND
U1 INV DPWR DGND OE OEBAR
+  D_PLD_GATE IO_PLD
*
U2 BUF3 DPWR DGND I0 OEBAR  O
+  D_PLD_TGATE IO_PLD
.ENDS
*$
***-------------------------------------------------------------------
* 2 INPUT AND GATE
*
.SUBCKT AND2 I0 I1 O  optional: DPWR=$G_DPWR DGND=$G_DGND
U1 AND(2) DPWR  DGND I0 I1  O  D_PLD_GATE IO_PLD
.ENDS
*$
*-------------------------------------------------------------------
.MODEL D_PLD_GATE  UGATE
*$
.MODEL D_PLD_TGATE  UTGATE
*$
.MODEL D_PLD_EFF  UEFF
*$
.MODEL D_PLD_GFF  UGFF
*$
.MODEL IO_PLD  UIO
```

```
*$
**====================================================================*
* Note:                                                              *
* Altough models can be a useful tool in evaluating device           *
* performance, they cannot model exact device performance            *
* under all conditions, nor are they intended to replace             *
* breadboarding for final verification!                              *
*                                                                    *
* Models provided by VISHAY Semiconductors GmbH are not              *
* as fully representing all of the specifications and operating      *
* characteristics of the semiconductor product to which the          *
* model relates.                                                     *
* The models describe the characteristics of typical devices.        *
* In all cases, the current data sheet information for a given       *
* device is the final design guideline and the only actual           *
* performance specification.                                         *
* VISHAY Semiconductors does not assume any liability arising        *
* from the model use. VISHAY Semiconductors reserves the right to    *
* change models without prior notice.                                *
**====================================================================*
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SIMULATED PARAMETERS (T_{amb} = 25 °C, unless otherwise specified)				
PARAMETER	**TEST CONDITION**	**SYMBOL**	**SIMULATION DATA**	**UNIT**
OUTPUT				
Input threshold current	$V_E = V_O = 5$ V, $R_L = 350\ \Omega$	I_{TH}	5	mA
SWITCHING (1)				
Propagation delay time to high output level	$R_L = 350\ \Omega$, $C_L = 15$ pF	t_{pLH}	53	ns
Propagation delay time to low output level		t_{pHL}	42	

Note

(1) See Switching Time and Timing Simulation Setup for switching parameters.

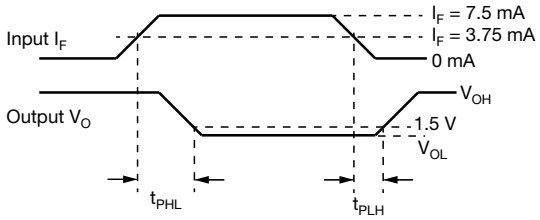

Fig. 1 - Switching Times

EXAMPLE SIMULATION PLOTS USING OrCAD

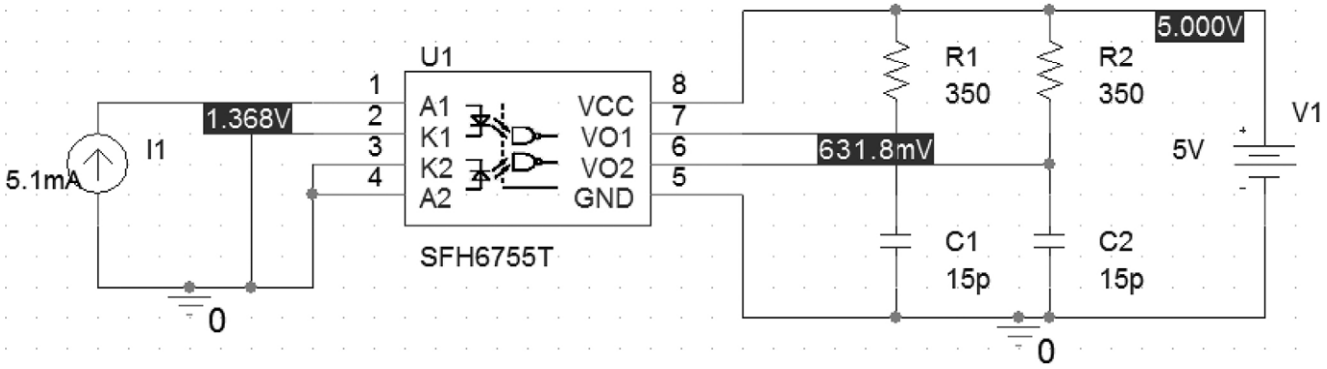

Fig. 2 - Simulation Setup for DC Characteristics

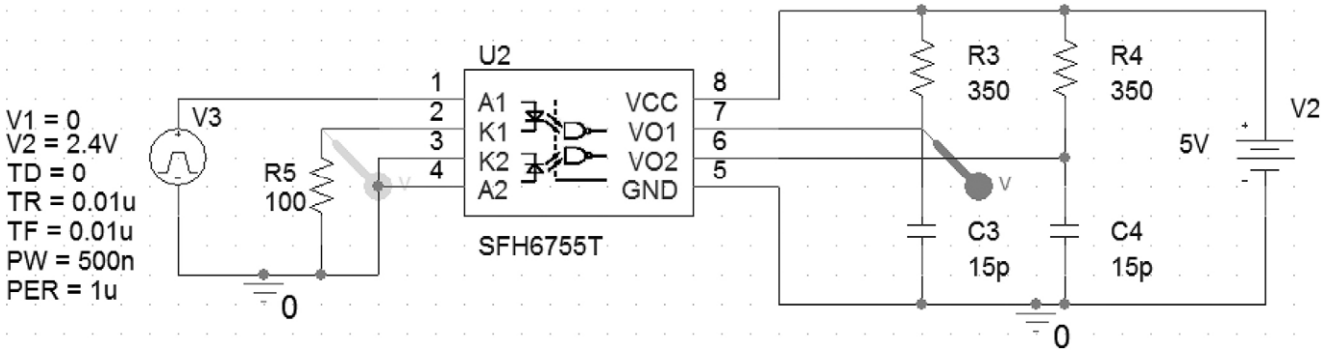

Fig. 3 - Timing Simulation Setup of SFH6755T (V_{CC} = 5 V, R_L = 350 Ω, C_L = 15 pF)

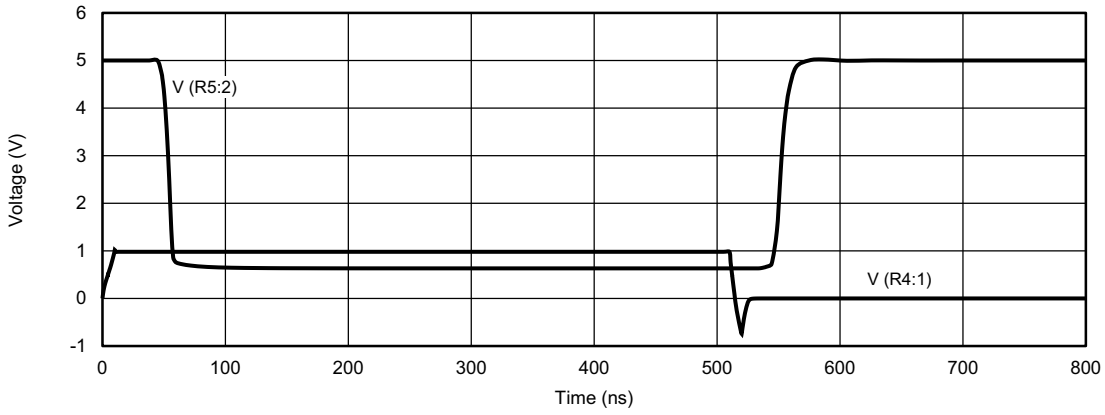

Fig. 4 - Timing Simulation Output of SFH6755T