

Vishay

Soldering Process

VISHAY DIODES RECOMMENDED SOLDERING PROCESS

Through hole device (THD) and surface mount device (SMD) imply different soldering technologies leading to different constraints.

In THD, the package body is exposed to relatively low temperatures (< 150 °C) because the lead extremeties are only dipped in the soldering alloy, whereas in SMD the whole package body is exposed to a very high temperature (> 240 °C) during reflow soldering process.

In addition, molding compounds used for encapsulation absorb moisture from the ambient medium. During rapid heating in solder reflow process; this absorbed moisture can vaporize, generating pressure at lead frame pad/silicon to plastic interfaces in the package, with a risk of package cracking and potential degradation of device reliability.

Wave soldering with SMD packages is not recommended because the thermal shock associated with package body solder dipping may induce internal structural damage to the package (interface delamination) that may affect long term reliability.

SMD package characterizations performed as a standard by Vishay only induce Solder Reflow Resistance assessment.

JEDEC[®] JESD A111 recommends that wave soldering of SMD packages should be evaluated by the USER, because the stress induced inside the package is very dependant of solder process parameters.

Due to the higher melting point of lead (Pb)-free alloys, the temperature of the solder pot will also increase to improve solderability and shorten contact times. For AgSnCu with melting point of 217 °C, the solder pot temperature will be between 250 °C to 270 °C or as high as 260 °C to 280 °C for SnCu.

RECOMMENDED WAVE SOLDERING PROFILE FOR THROUGH HOLE COMPONENTS



Fig. 1



Notes

• Temperature jump from T_2 to T_3 (w1): 150 °C max.

• Time from 25 °C to T₃ (wave temp.): 8 min max.

Fig. 2



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REFLOW FOR SURFACE MOUNTED COMPONENTS

TABLE 1 - CLASSIFICATION REFLOW PROFILE					
PROFILE FEATURE	Sn-Pb EUTECTIC ASSEMBLY	LEAD (Pb)-FREE ASSEMBLY			
Preheat and soak					
Temperature min. (T _{Smin.})	100 °C 150 °C				
Temperature max. (T _{Smax.})	150 °C	200 °C			
Time (T _{Smin.} to T _{Smax.}) (t _S)	60 s to 120 s	60 s to 120 s			
Average ramp-up rate (T _{Smax.} to T _p)	3 °C/s maximum				
Liquidus temperature (TL)	183 °C	217 °C			
Time to liquidus (t _L)	60 s to 150 s	60 s to 150 s			
Peak package temperature $(T_p)^{(1)}$	See classification temperature in table 2	See classification temperature in table 3			
Time $(t_p)^{(2)}$ with 5 °C of the specified classification temperature (T_C)	20 s ⁽²⁾ 30 s ⁽²⁾				
Average ramp-down rate (T_p to T_{Smax})	6 °C/s maximum				
Time 25 °C to peak temperature	6 min maximum 8 min maximum				

Notes

 $^{(1)}$ Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and user maximum

 $^{(2)}$ Tolerance for time at peak profile temperature (T₀) is defined as a supplier minimum and user maximum

REFLOW PROFILE





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TABLE 2 - Sn-Pb EUTECTIC PROCESS PACKAGE PEAK REFLOW TEMPERATURES				
PACKAGE THICKNESS	VOLUME mm ³ < 350	VOLUME mm ³ ≥ 350		
< 2.5 mm	235 °C	220 °C		
≥ 2.5 mm	220 °C	220 °C		

TABLE 3 - LEAD (Pb) - FREE PROCESS PACKAGE CLASSIFICATION REFLOW TEMPERATURES					
PACKAGE THICKNESS	VOLUME mm ³ < 350	VOLUME mm ³ 350 to 2000	VOLUME mm ³ > 2000		
< 1.6 mm	260 °C	260 °C	260 °C		
1.6 mm to 2.5 mm	260 °C	250 °C	245 °C		
≥ 2.5 mm	250 °C	245 °C	245 °C		

Tolerance: The device manufacturer / supplier shall assure process compatibility up to and including the stated classification temperature at the rated MSL level.

Notes

Package volume excludes external terminals (balls, bumps, lands, leads) and/or non-integral heatsinks

• The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist

• Recommended soldering process is accordance with IPD / JEDEC® J-STD-020E. Copyright 2014