Zero-Voltage Switching Full-Bridge Converter: Operation, FOM, and Guidelines for MOSFET Selection

By Philip Zuk and Sanjay Havanur

There are two categories of switching topologies used in power conversion design, referred to as hard and soft switching topologies. The main difference between hard and soft switching is that in hard switching during turn ON, a voltage equal to at least the supply voltage is impressed upon the MOSFET and the current tends to flow from drain to source, resulting in high turn ON losses. In soft switching, the current at turn ON is oriented from source to drain, which discharges the MOSFET's output capacitance (C_{OSS}) before turning the device on, thereby eliminating turn ON losses. Initially, the parasitic MOSFET body diode conducts and when the MOSFET is activated the current commutates to the channel. Figures 1a and 1b show the difference between a hard-switched waveform with turn ON and turn OFF crossover losses versus turn OFF losses for zero-voltage switching (ZVS). One characteristics of soft switching is that the gate voltage will begin to rise only after drain-source voltage comes down very close to zero. As operating frequencies continue to climb, more designs are being converted into soft switching modes to save the switching losses.

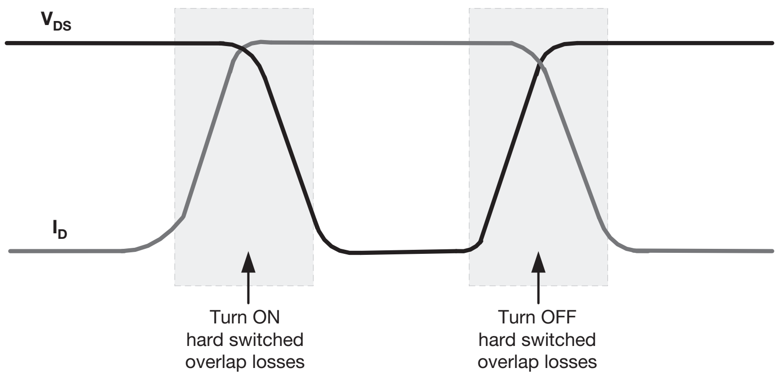

Fig. 1a - Standard Hard-Switched Waveforms

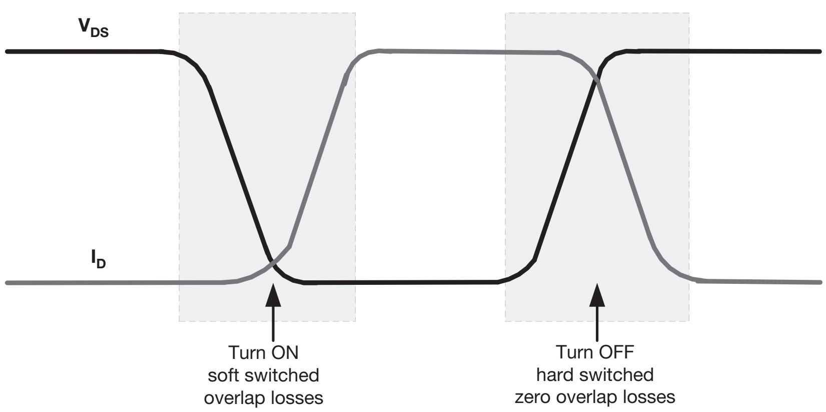

Fig. 1b - ZVS Waveforms

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There are several topologies used in the soft switching category. On the primary side the most common configurations are active reset, LLC, and ZVS full bridge (ZVSFB), and SSR on the secondary side. This design guide will focus specifically on the ZVSFB arrangement shown in Figure 2, which is typically found in telecom bricks and AC/DC power supplies. The ZVS topology is often referred to as a "phase-shifted full bridge," meaning a full bridge that invokes phase shifting between the two arms in order to achieve ZVS. The phase-shifted full-bridge converter clamps and recycles the energy stored in the power transformer's leakage inductance to softly turn ON each of the four power MOSFETs. This improves efficiency, reduces switching-related EMI, and eliminates the need for primary-side snubbers.

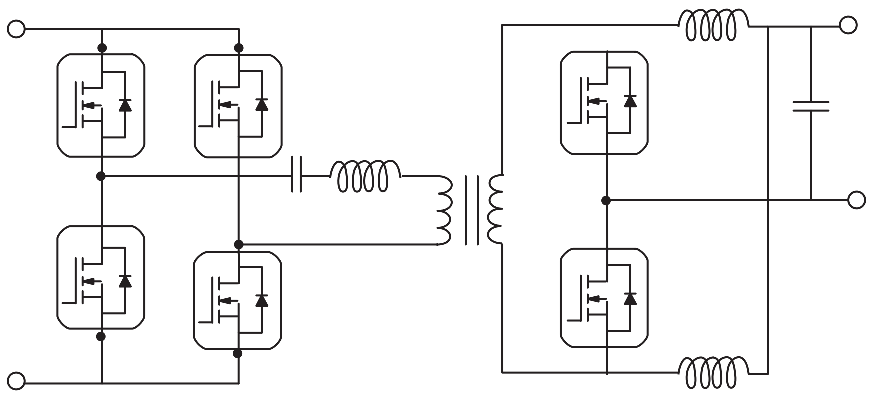
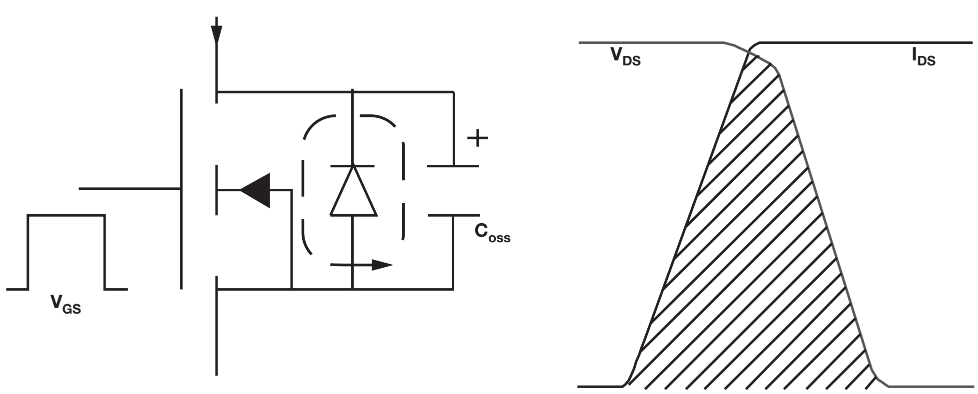


Fig. 2 - Typical ZVSFB Circuit

WHY ZERO-VOLTAGE SWITCHING

When a MOSFET turns on, there are losses due to voltage and current overlap (Figure 3) and the discharge of stored energy in its C_{OSS} capacitor. In ZVS the C_{OSS} is tricked into discharging its energy prior to turning on the MOSFET. Usually the MOSFET's body diode goes into conduction in the process. It should be noted that ZVS operation eliminates only turn ON losses; switching losses during turn OFF, both due to overlap and C_{OSS} charging, will still be incurred.



Turn ON switching loss in a MOSFET

Fig. 3 - Turn ON Switching Losses

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TYPICAL OPERATION OF ZVS PHASE-SHIFTED FULL BRIDGE

Figures 4a to 4f show the typical operation of a standard phase-shifted ZVSFB. Starting at the upper left with the basic bridge circuit and following the arrows we have the following:

- Figure 4b: MOSFETs Q1 / Q2 are turned on and Q3 / Q4 are off. Primary current (blue) flows, delivering power to the secondary through transformer T1.
- Figure 4b: Q2 turns off, primary current flows through output capacitance C_{oss} of Q3 and discharges it. Load current now flows through the output rectifiers and there is no power transfer from primary to secondary.
- Figure 4d: Once the C_{oss} of Q3 is discharged, the magnetizing current continues to flow through the body diode of Q3, which is now turned on with zero voltage across it. The magnetizing current now flows through the channel and not the body diode. The duration of this interval may be varied by the controller to maintain output regulation.
- Figure 4e: Q1 is turned off and the magnetizing current finds its path through Q4, discharging its C_{oss}. Once C_{oss} is fully discharged the magnetizing current forward biases its body diode.
- Figure 4f: Q4 can now be turned on with ZVS. Power transfer to the secondary is resumed. At the end of this interval Q3 is turned off and the sequence is repeated.

IMPORTANCE OF MOSFET BODY DIODE IN ZVS CIRCUITS

Although the MOSFET body diodes conduct during every transition, it is evident that they are not subject to hard commutation. The diode current is commutated softly by the channel of the parent MOSFET. However, this does not mean that reverse recovery of the diode may be ignored in ZVS applications. In the interval of Figure 4f, the body diode of Q3 needs to regain its ability to block high voltage before Q3 is turned off. If the Q3 body diode does not recover or start blocking the rail or main voltage, the bridge may be subject to what is commonly known as “shoot through,” resulting in high currents through Q2 and the body diode of Q3. Q2 / Q3 may not fail immediately, but over time they will continue to dissipate heat which leads to failure. Failures may also happen unexpectedly during line and load transients.

The problems associated with body diode recovery increase exponentially with the voltage rating of the device. For example, the Q_{rr} of a 100 V MOSFET used in 48 V telecom systems is in the range of tens of nC, whereas for standard 600 V superjunction devices it will be several μC. Most low-voltage MOSFETs can be used in ZVS mode up to several hundred kHz. However, fast body diode (FBD) versions of high-voltage power MOSFETs are recommended in ZVS topologies. Typically, the FBD MOSFETs are designed to have a 5 x to 10 x reduction in the reverse recovery charge Q_{rr} for their body diodes. Looking at the Q_{rr} of the SiHG47N60E-GE3 (standard MOSFET) versus the SiHG47N60EF-GE3 (FBD MOSFET), one would see a Q_{rr} of 11 μC versus 1.1 μC, respectively, which also results in a 4 x reduction in t_{rr}. The lower Q_{rr} results in a faster recovery time during soft commutation. The ability of the MOSFET’s body diode to block high voltage, which is crucial to the safe operation of any ZVS topology, is greatly enhanced in the FBD MOSFETs.

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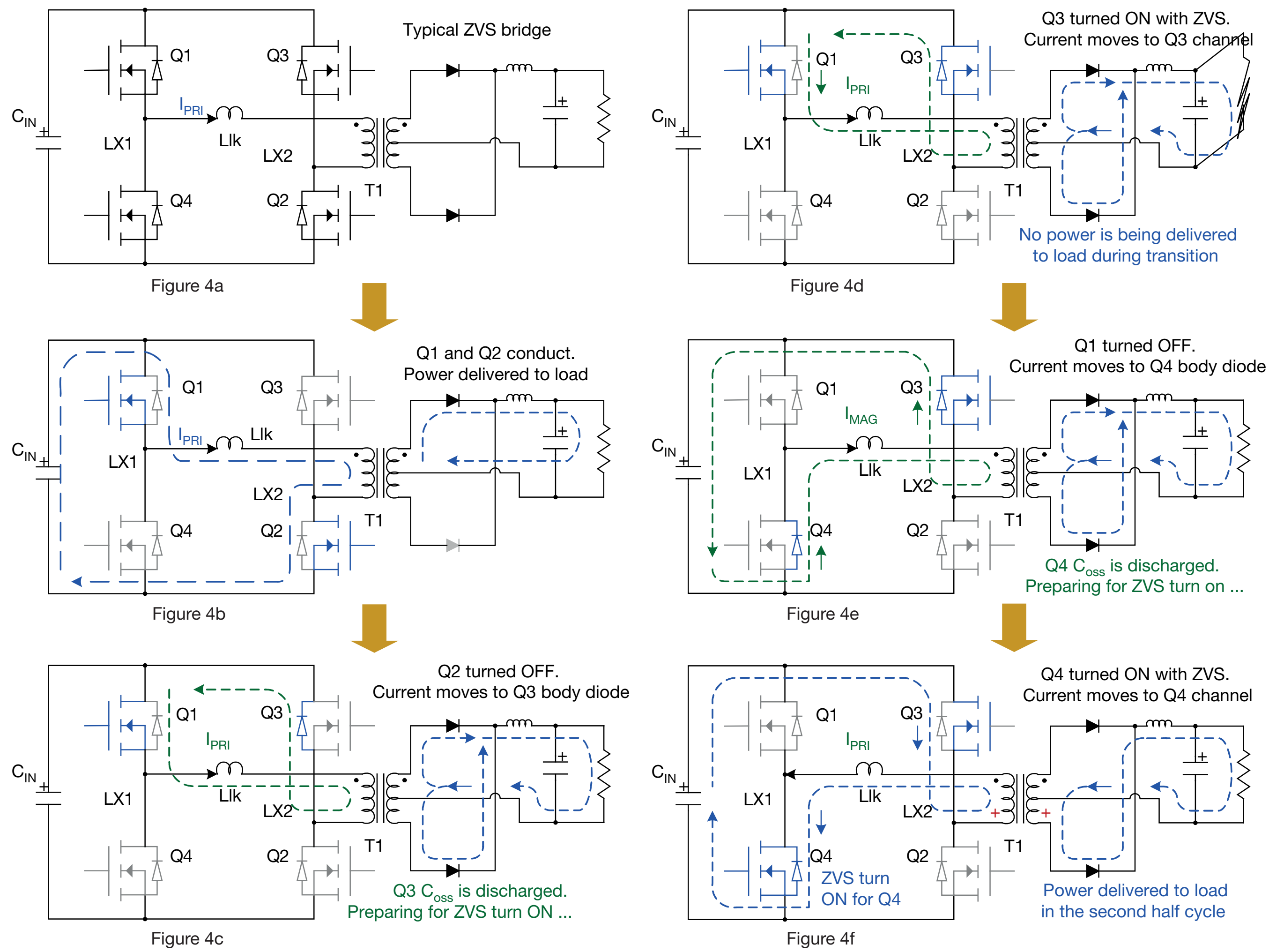

Fig. 4 - Operating Sequence of a ZVS Phase-Shifted Full Bridge

LOSS ANALYSIS FOR MOSFETs IN A ZVS FULL BRIDGE

Vishay strongly recommends that MOSFET selection for any topology should be made based on application-specific power losses, rather than generic figures like $R_{DS(on)}$ x Q_g product. Towards that end, several design and MOSFET selection guides have been published covering different topologies. The power loss for a phase-shift ZVSFB is shown below. You can see that the equation takes into account conduction, switching, output, gate drive and body diode losses. The following represent the definition of each variable used in the power loss equation below:

P_{IN} - input power to the power supply

TCR - temperature coefficient of resistance (typically Figure 4 within Vishay's HVM datasheets)

R_{DS} - typical on-resistance value of the device

Q_{sw} - switching change, being a combination / ratio of Q_{gs} and Q_{gd}

I_{goff} - MOSFET gate drive turn OFF current

f_{sw} - switching frequency of the phase-shifted ZVSFB

Q_{oss} - output charge

V_{DR} - output voltage of the gate driver that drives the MOSFET

Q_g - gate charge

V_{fwd} - forward voltage drop of the MOSFET body diode

t_{dead} - dead time for the MOSFET body diode to recover before turning the MOSFET on

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$$P_d = \underbrace{\left(\frac{P_{IN}}{V_{IN}}\right)^2 \times \frac{TCR}{2} \times R_{DS}}_{\text{Conduction loss}} + \underbrace{\frac{P_{IN}}{2} \times \frac{Q_{sw}}{I_{goff}} \times f_{sw}}_{\text{Switching loss}} + \underbrace{\frac{1}{2} \times V_{IN} \times Q_{oss} \times f_{sw}}_{\text{Output loss}} + \underbrace{V_{drv} \times Q_g \times f_{sw}}_{\text{Gate drive loss}} + \underbrace{\frac{P_{IN}}{V_{IN}} \times V_{fwd} \times t_{dead} \times f_{sw}}_{\text{Body diode loss}}$$

With ZVS, the conduction losses dominate, followed by the C_{oss}-related losses. As a result, the application-specific figure of merit (FOM) gets biased towards $R_{DS(on)}$ and Q_{rr} / Q_{oss} (C_{oss} losses in a MOSFET come from a combination of Q_{rr} / Q_{oss}). The switching losses from volt-ampere crossover are relatively low, since turn ON losses are nullified, leaving only turn OFF.

HVM SELECTION RULES AND GUIDE

With this in mind, we have developed a list of components that we feel will achieve the highest efficiency for a ZVSFB converter - based on typical operating conditions - to ensure the most efficient design possible. Table 1 illustrates the operating conditions assumed for such a power supply.

TABLE 1 - TYPICAL PHASE-SHIFTED ZVSFB CONVERTER OPERATING CONDITIONS

Input Voltage	390 V
Input Power	200 W to 3000 W
ZVS Switching Frequency	200 kHz
MOSFET Drive Voltage	12 V
ON / OFF Gate Current Range	0.5 A (200 W) to 2.5 A (3000 W)

With many package options available, Table 2 lists the recommended package as a function of maximum power rating of the converter. The power rating is quadruple that used for a single-ended topology like power factor correction (PFC) or flyback. The reason is that, for a given power level, PFC stages are designed for input voltages from 100 V_{AC} to 264 V_{AC}, whereas the ZVSFB downstream operates from a near constant input of 400 V_{DC}. The full bridge also has two legs, further splitting the current in half.

TABLE 2 - RECOMMENDED PACKAGE TYPES BASED ON POWER LEVELS

RECOMMENDED PACKAGES	MAAXIMUM POWER RATINGS
D^2PAK (TO-263) / TO-220	Up to 1800 W (1)
TO-220F / Thin Lead TO-220F	Up to 1800 W (1)
TO-247AC	Up to 3000 W (1)
Super TO-247	Up to 3000 W (1)

Note

(1) Limited by single-phase power rating, no paralleling, and based on largest die size available in 600 V and 650 V

Figure 5 defines the packages, current rating, voltage, and device technology of the different part numbers in the EF series.

The final list of recommended device part numbers includes an "x" in the "Package" location. For the same set of electrical characteristics, a number of package options may be available per device. The packages used will depend on the power level as well as the MOSFET real estate allowed.

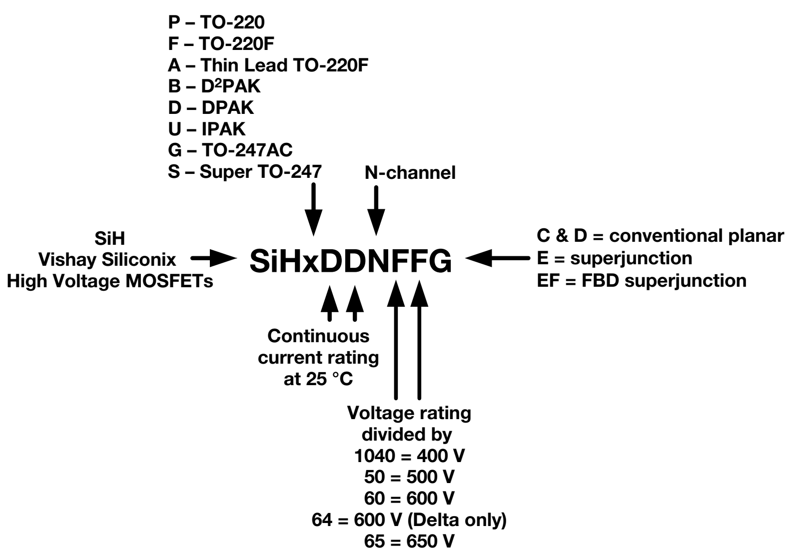

Fig. 5 - Part Numbers Definition

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ESTIMATION EXAMPLE USING CONDUCTION AND SWITCHING LOSSES AS 50/50

This example will use the case of a ZVSFB converter in a 2 kW power supply. We can fix a loss target of less than 0.5 % of the total converter loss for each MOSFET and also aim for equal distribution of conduction and switching losses. For our 2 kW switch mode power supply, the losses would have to be less than 10 W per device, with no more than 5 W coming from conduction losses. The bridge operates with 65 % duty cycle in order to allow for holdup time at low line under brown-out conditions. This translates to an effective duty ratio of 32.5 % per MOSFET in each arm.

Effective duty cycle = t_{on}/t = 3.2 μs/5 μs = 65 %, which translates to 32.5 % per arm.

Average current: $I_{avg} = P_{IN}/V_{IN}$ = 2000 W/390 V = 5.12 A

Peak current: $I_{pk} = I_{avg}$/duty = 5.12 A/0.65 = 7.88 A

RMS current: $I_{RMS} = I_{pk}$ x duty^{½} = 7.88 A x 0.325^{½} = 4.49 A (per device)

Solving the conduction power loss equation for on-resistance (shown below):

5 W = $R_{DS(on)}$ x 2.0 x 4.492 = 124 mΩ

With this design, the RMS current in each MOSFET will be 4.49 A. When the conduction losses are calculated ($P_{cond} = R_{DS(on)}$ x TCR at 100 °C x I_{RMS}^2) and equated to 5 W, we arrive at an upper limit of 124 mΩ for $R_{DS(on)}$. The nearest device is the SiHP28N60EF-GE3, with a typical $R_{DS(on)}$ of 107 mΩ. The total power dissipation would be close to the limit of ~10 W that many designers set for the TO-220 package. So for 2000 W - depending on the application, derating rules, and system thermal design - one may want to move to the TO-247AC version, which will be the SiHG28N60EF-GE3.

After reviewing the design conditions, maximum recommended power level per package type, and an understanding of the part numbering system, Table 3 has been generated to show the recommended devices for the different power levels in high-voltage ZVS bridge applications. As our new FBD MOSFET family evolves, many more devices will become available within these ranges. Depending on whether voltage, efficiency, or price is a higher concern, designers can pick the device that best fits their application.

TABLE 3 - DEVICE SELECTION TOOL BASED ON PFC OUTPUT POWER LEVELS
ZVSFB FBD SELECTOR GUIDE

OUTPUT POWER			
≤ 1000 W	> 1000 W	≥ 2000 W	≥ 3000 W
SiHx21N60EF	SiHx28N60EF	SiHx33N60EF	SiHG47N60EF