SPICE Device Model SiHF15N65E



Vishay Siliconix

E Series Power MOSFET

DESCRIPTION

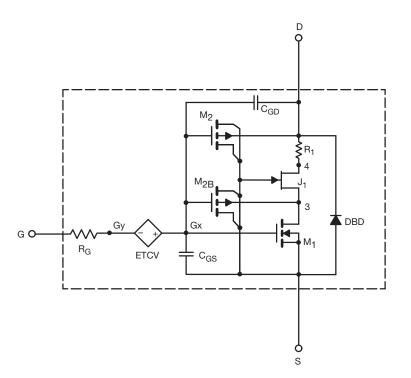
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over 25 °C to 150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{gd}\xspace$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over 25 °C to 150 °C temperature range
- · Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

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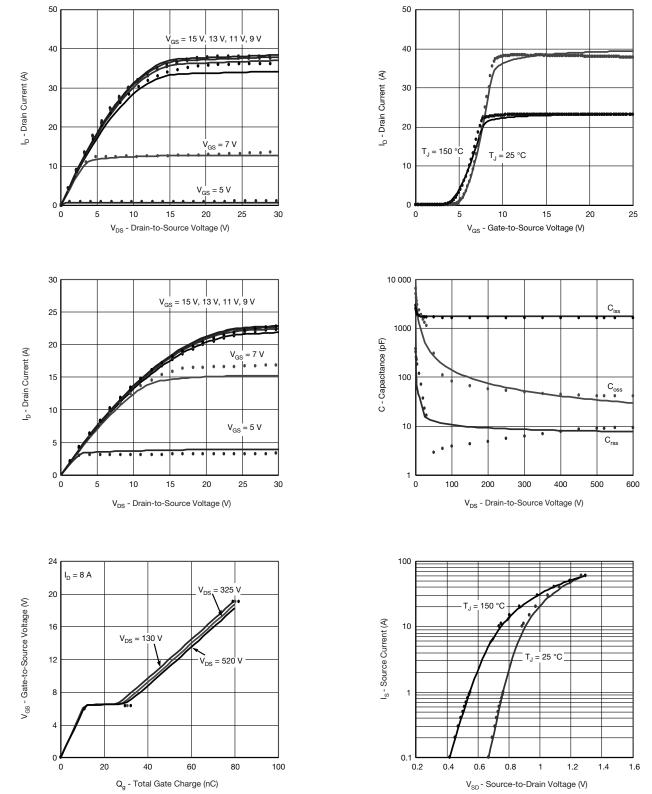
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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	3	-	V
Drain-Source On-State Resistance	R _{DS(on)}	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 8 \text{ A}$	0.25	0.23	Ω
Forward Transconductance	g fs	$V_{DS} = 30 \text{ V}, \text{ I}_{D} = 8 \text{ A}$	7.4	5.6	S
Dynamic					
Input Capacitance	C _{iss}	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, \text{ f} = 1 \text{ MHz}$	1640	1640	pF
Output Capacitance	C _{oss}		80	80	
Reverse Transfer Capacitance	C _{rss}		4	4	
Total Gate Charge	Qg	$V_{DS} = 480 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 8 \text{ A}$	48	48	nC
Gate-Source Charge	Q _{gs}		11	11	
Gate-Drain Charge	Q _{gd}		21	21	
Drain-Source Body Diode Characteristics					
Diode Forward Voltage	V _{SD}	$T_J = 25 \ ^{\circ}C, \ I_S = 8 \ A, \ V_{GS} = 0 \ V$	0.9	-	V
Reverse Recovery Time	t _{rr}	$T_J = 25 \text{ °C}, I_F = I_S = 8 \text{ A},$ dI/dt = 100 A/µs, V _R = 25 V	320	325	ns
Reverse Recovery Charge	Q _{rr}		4.9	4.6	μC



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COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)



Note

• Dots and squares represent measured data. Copyright: Vishay Intertechnology, Inc.

S16-1397-Rev. B, 18-Jul-16

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