Power MOSFET

FEATURES
- Surface-mount
- Available in tape and reel
- Dynamic dv/dt rating
- Repetitive avalanche rated
- 175 °C operating temperature
- Fast switching
- Ease of paralleling
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note
* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION
Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface-mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface-mount application.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>LIMIT</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source voltage</td>
<td>V_DS</td>
<td>100</td>
<td>V</td>
</tr>
<tr>
<td>Gate-source voltage</td>
<td>V_GS</td>
<td>±20</td>
<td>V</td>
</tr>
<tr>
<td>Continuous drain current</td>
<td>I_D</td>
<td>28</td>
<td>A</td>
</tr>
<tr>
<td>Pulsed drain current</td>
<td>I_DM</td>
<td>110</td>
<td>A</td>
</tr>
<tr>
<td>Linear derating factor</td>
<td>1.0</td>
<td></td>
<td>W/°C</td>
</tr>
<tr>
<td>Linear derating factor (PCB mount)</td>
<td>0.025</td>
<td></td>
<td>A/°C</td>
</tr>
<tr>
<td>Single pulse avalanche energy</td>
<td>E_AS</td>
<td>230</td>
<td>mJ</td>
</tr>
<tr>
<td>Avalanche current</td>
<td>I_AR</td>
<td>28</td>
<td>A</td>
</tr>
<tr>
<td>Repetitive avalanche energy</td>
<td>E_AR</td>
<td>15</td>
<td>mJ</td>
</tr>
<tr>
<td>Maximum power dissipation</td>
<td>P_D</td>
<td>150</td>
<td>W</td>
</tr>
<tr>
<td>Peak diode recovery dv/dt</td>
<td>dv/dt</td>
<td>5.5</td>
<td>V/ns</td>
</tr>
<tr>
<td>Operating junction and storage temperature range</td>
<td>T_J, T_stg</td>
<td>-55 to +175</td>
<td>°C</td>
</tr>
</tbody>
</table>

Notes
a. Repetitive rating: pulse width limited by maximum junction temperature (see fig. 11)
b. V_DS = 25 V, starting T_J = 25 °C, L = 440 μH, R_s = 25 Ω, I_PS = 28 A (see fig. 12)
c. I_D ≤ 28 A, dv/dt ≤ 170 A/μs, V_DS ≤ V_GS, T_J ≤ 175 °C
d. 1.6 mm from case
e. When mounted on 1” square PCB (FR-4 or G-10 material)
**THERMAL RESISTANCE RATINGS**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum junction-to-ambient</td>
<td>RthJA</td>
<td>-</td>
<td>62</td>
<td>°C/W</td>
</tr>
<tr>
<td>Maximum junction-to-ambient (PCB mount) a</td>
<td>RthJA</td>
<td>-</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>Maximum junction-to-case (drain)</td>
<td>RthJC</td>
<td>-</td>
<td>1.0</td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

a. When mounted on 1" square PCB (FR-4 or G-10 material)

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**SPECIFICATIONS** *(TJ = 25 °C, unless otherwise noted)*

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain-source breakdown voltage</td>
<td>VDS</td>
<td>VGS = 0, IGS = 250 μA</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>VDS temperature coefficient</td>
<td>ΔVDS/TJ</td>
<td>Reference to 25 °C, IGS = 1 mA</td>
<td>-</td>
<td>0.13</td>
<td>-</td>
<td>V/°C</td>
</tr>
<tr>
<td>Gate-source threshold voltage</td>
<td>VGS(th)</td>
<td>VDS = VGS, IGS = 250 μA</td>
<td>2.0</td>
<td>-</td>
<td>4.0</td>
<td>V</td>
</tr>
<tr>
<td>Gate-source leakage</td>
<td>ISG</td>
<td>VGS = ± 20 V</td>
<td>-</td>
<td>-</td>
<td>± 100 nA</td>
<td></td>
</tr>
<tr>
<td>Zero gate voltage drain current</td>
<td>IGD</td>
<td>VDS = 100 V, VGS = 0 V</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td>μA</td>
</tr>
<tr>
<td>Drain-source on-state resistance</td>
<td>RDS(on)</td>
<td>VGS = 10 V</td>
<td>I0 = 17 A b</td>
<td>-</td>
<td>-</td>
<td>0.077 Ω</td>
</tr>
<tr>
<td>Forward transconductance</td>
<td>gfs</td>
<td>VDS = 50 V, I0 = 17 A b</td>
<td>8.7</td>
<td>-</td>
<td>-</td>
<td>Ω</td>
</tr>
<tr>
<td><strong>Dynamic</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input capacitance</td>
<td>Ciss</td>
<td>f = 1 MHz, see fig. 5</td>
<td>-</td>
<td>1700</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Output capacitance</td>
<td>Coss</td>
<td>f = 1 MHz, see fig. 5</td>
<td>-</td>
<td>560</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Reverse transfer capacitance</td>
<td>Crss</td>
<td>f = 1 MHz, see fig. 5</td>
<td>-</td>
<td>120</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Total gate charge</td>
<td>Qg</td>
<td>VGS = 10 V</td>
<td>I0 = 17 A, VDS = 80 V, see figs. 6 and 13 b</td>
<td>-</td>
<td>-</td>
<td>72</td>
</tr>
<tr>
<td>Gate-source charge</td>
<td>Qgs</td>
<td>VGS = 10 V</td>
<td>I0 = 17 A</td>
<td>-</td>
<td>-</td>
<td>11</td>
</tr>
<tr>
<td>Gate-drain charge</td>
<td>Qgd</td>
<td>f = 1 MHz, open drain</td>
<td>-</td>
<td>-</td>
<td>32</td>
<td>nC</td>
</tr>
<tr>
<td>Turn-on delay time</td>
<td>t(on)</td>
<td>VDD = 50 V, I0 = 17 A, Rg = 9.1 Ω, Rd = 2.9 Ω, see fig. 10 b</td>
<td>-</td>
<td>11</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Rise time</td>
<td>tr</td>
<td>f = 1 MHz, open drain</td>
<td>-</td>
<td>-</td>
<td>44</td>
<td>ns</td>
</tr>
<tr>
<td>Turn-off delay time</td>
<td>t(off)</td>
<td>f = 1 MHz, open drain</td>
<td>-</td>
<td>53</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Fall time</td>
<td>tf</td>
<td>f = 1 MHz, open drain</td>
<td>-</td>
<td>43</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Gate input resistance</td>
<td>Rg</td>
<td>Between lead, 6 mm (0.25&quot;) from package and center of die contact</td>
<td>0.5</td>
<td>-</td>
<td>3.6</td>
<td>Ω</td>
</tr>
<tr>
<td><strong>Drain-Source Body Diode Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Continuous source-drain diode current</td>
<td>IS</td>
<td>MOSFET symbol showing the integral reverse p-n junction diode</td>
<td>-</td>
<td>-</td>
<td>28</td>
<td>A</td>
</tr>
<tr>
<td>Pulsed diode forward current a</td>
<td>ISM</td>
<td></td>
<td>-</td>
<td>-</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td>Body diode voltage</td>
<td>VDS</td>
<td>TJ = 25 °C, I0 = 28 A, VGS = 0 V b</td>
<td>-</td>
<td>-</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>Body diode reverse recovery time</td>
<td>trr</td>
<td>TJ = 25 °C, I0 = 17 A, dI/dt = 100 A/μs b</td>
<td>-</td>
<td>180</td>
<td>360</td>
<td>ns</td>
</tr>
<tr>
<td>Body diode reverse recovery charge</td>
<td>Qrr</td>
<td>TJ = 25 °C, I0 = 17 A, dI/dt = 100 A/μs b</td>
<td>-</td>
<td>1.3</td>
<td>2.8</td>
<td>μC</td>
</tr>
<tr>
<td>Forward turn-on time</td>
<td>ton</td>
<td>Intrinsic turn-on time is negligible (turn-on is dominated by Ls and Lo)</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics, \( T_C = 25 \, ^\circ C \)**

**Fig. 2 - Typical Output Characteristics, \( T_C = 175 \, ^\circ C \)**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**
IRF540S, SiHF540S
Vishay Siliconix

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 8 - Maximum Safe Operating Area

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case
Vary $t_p$ to obtain required $I_{AS}$

**Fig. 12a - Unclamped Inductive Test Circuit**

**Fig. 12b - Unclamped Inductive Waveforms**

**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

$E_{AS}$, Single Pulse Energy (mJ)

Starting $T_J$, Junction Temperature (°C)

**Fig. 13a - Basic Gate Charge Waveform**

**Fig. 13b - Gate Charge Test Circuit**
Peak Diode Recovery dV/dt Test Circuit

- Circuit layout considerations
  - Low stray inductance
  - Ground plane
  - Low leakage inductance
current transformer
- dV/dt controlled by $R_g$
- Driver same type as D.U.T.
- $I_{SD}$ controlled by duty factor “D”
- D.U.T. - device under test

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Driver gate drive

D.U.T. $I_{SD}$ waveform

Reverse recovery current

D.U.T. $V_{DS}$ waveform

Re-applied voltage

Inductor current

Body diode forward drop

Ripple ≤ 5 %

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Note

a. $V_{GS} = 5$ V for logic level devices

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Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg91022.
**Package Information**

Vishay Siliconix

**TO-263AB (HIGH VOLTAGE)**

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**Notes**

2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

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**DIM.** | **MIN.** | **MAX.** | **DIM.** | **MIN.** | **MAX.**
---|---|---|---|---|
A | 4.06 | 4.83 | D1 | 6.86 | -
A1 | 0.00 | 0.25 | E | 9.65 | 10.67
b | 0.51 | 0.99 | E1 | 6.22 | -
b1 | 0.51 | 0.89 | e | 2.54 BSC | 0.100 BSC
b2 | 1.14 | 1.78 | H | 14.61 | 15.88
b3 | 1.14 | 1.73 | L | 1.78 | 2.79
C | 0.38 | 0.74 | L1 | - | 1.65
C1 | 0.38 | 0.58 | L2 | - | 1.78
C2 | 1.14 | 1.65 | L3 | 0.25 BSC | 0.010 BSC
D | 8.38 | 9.65 | L4 | 4.78 | 5.28

**ECN:** S-82110-Rev. A, 15-Sep-08

**DWG:** 5970
RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead

Recommended Minimum Pads
Dimensions in Inches/(mm)

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