Power MOSFET

FEATURES
• Dynamic dV/dt rating
• Repetitive avalanche rated
• Fast switching
• Ease of paralleling
• Simple drive requirements
• Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note
* This datasheet provides information about parts that are RoHS-compliant and/or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

PRODUCT SUMMARY

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>LIMIT</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source voltage</td>
<td>VDS</td>
<td>250</td>
<td>V</td>
</tr>
<tr>
<td>Gate-source voltage</td>
<td>VGS</td>
<td>± 20</td>
<td>V</td>
</tr>
<tr>
<td>Continuous drain current</td>
<td>VG at 10V</td>
<td>TC = 25°C</td>
<td>ID</td>
</tr>
<tr>
<td>Continuous drain current</td>
<td>VG at 100°C</td>
<td>TC = 100°C</td>
<td>ID</td>
</tr>
<tr>
<td>Pulsed drain current</td>
<td>IDM</td>
<td>14</td>
<td>A</td>
</tr>
<tr>
<td>Linear derating factor</td>
<td></td>
<td>0.40</td>
<td>W/°C</td>
</tr>
<tr>
<td>Single pulse avalanche energy</td>
<td>EAS</td>
<td>100</td>
<td>mJ</td>
</tr>
<tr>
<td>Repetitive avalanche energy</td>
<td>IAR</td>
<td>4.4</td>
<td>A</td>
</tr>
<tr>
<td>Repetitive avalanche energy</td>
<td>EAR</td>
<td>5.0</td>
<td>mJ</td>
</tr>
<tr>
<td>Maximum power dissipation</td>
<td>PD</td>
<td>50</td>
<td>W</td>
</tr>
<tr>
<td>Peak diode recovery dV/dt</td>
<td></td>
<td>4.8</td>
<td>V/ns</td>
</tr>
<tr>
<td>Operating junction and storage temperature range</td>
<td>TJ, Tstg</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Soldering recommendations (peak temperature)</td>
<td>For 10 s</td>
<td>300</td>
<td>lbf · in</td>
</tr>
<tr>
<td>Mounting torque</td>
<td>6-32 or M3 screw</td>
<td>10</td>
<td>lbf · in</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.1</td>
<td>N · m</td>
</tr>
</tbody>
</table>

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. VDD = 50 V, starting TJ = 25 °C, L = 8.3 mH, Rg = 25 Ω, IAS = 4.4 A (see fig. 12)
c. ISD ≤ 4.4 A, dv/dt ≤ 90 A/μs, VDD ≤ VDS, TJ ≤ 150 °C
d. 1.6 mm from case
## THERMAL RESISTANCE RATINGS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum junction-to-ambient</td>
<td>R_{thJA}</td>
<td>-</td>
<td>62</td>
<td>°C/W</td>
</tr>
<tr>
<td>Case-to-sink, flat, greased surface</td>
<td>R_{thCS}</td>
<td>0.50</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Maximum junction-to-case (drain)</td>
<td>R_{thJC}</td>
<td>-</td>
<td>2.5</td>
<td>-</td>
</tr>
</tbody>
</table>

## SPECIFICATIONS  
(T\_J = 25 °C, unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain-source breakdown voltage</td>
<td>V_{DS}</td>
<td>V_{GS} = 0 V, I_D = 250 μA</td>
<td>250</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>V_{DS} temperature coefficient</td>
<td>ΔV_{DS}/T_J</td>
<td>Reference to 25 °C, I_D = 1 mA</td>
<td>-</td>
<td>0.36</td>
<td>-</td>
<td>V/°C</td>
</tr>
<tr>
<td>Gate-source threshold voltage</td>
<td>V_{GS(th)}</td>
<td>V_{DS} = V_{GS}, I_D = 250 μA</td>
<td>2.0</td>
<td>-</td>
<td>4.0</td>
<td>V</td>
</tr>
<tr>
<td>Gate-source leakage</td>
<td>I_{GSS}</td>
<td>V_{DS} = ± 20 V</td>
<td>-</td>
<td>-</td>
<td>± 100</td>
<td>nA</td>
</tr>
<tr>
<td>Zero gate voltage drain current</td>
<td>I_{DSS}</td>
<td>V_{DS} = 250 V, V_{GS} = 0 V</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td>μA</td>
</tr>
<tr>
<td>Drain-source on-state resistance</td>
<td>R_{D(on)}</td>
<td>V_{GS} = 10 V, I_D = 2.6 A^b</td>
<td>-</td>
<td>-</td>
<td>1.1</td>
<td>Ω</td>
</tr>
<tr>
<td>Forward transconductance</td>
<td>g_{fs}</td>
<td>V_{DS} = 50 V, I_D = 2.6 A^b</td>
<td>1.5</td>
<td>-</td>
<td>-</td>
<td>S</td>
</tr>
<tr>
<td><strong>Dynamic</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input capacitance</td>
<td>C_{iss}</td>
<td>V_{GS} = 0 V, f = 1.0 MHz, see fig. 5</td>
<td>-</td>
<td>260</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Output capacitance</td>
<td>C_{oss}</td>
<td>V_{GS} = 25 V, V_{DS} = 25 V, f = 1.0 MHz</td>
<td>-</td>
<td>77</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Reverse transfer capacitance</td>
<td>C_{rss}</td>
<td>V_{GS} = 10 V</td>
<td>-</td>
<td>15</td>
<td>-</td>
<td>pF</td>
</tr>
</tbody>
</table>
| Total gate charge                 | Q_{g}   | V_{DS} = 125 V, I_D = 4.4 A, 
                                 |        | R_{g} = 18 Ω, R_{D} = 28 Ω | -    | -    | 14   | nC   |
| Gate-source charge                | Q_{gs}  | V_{DS} = 125 V, I_D = 4.4 A, 
                                 |        | see fig. 6 and 13 | -    | -    | 2.7  | nC   |
| Gate-drain charge                 | Q_{gd}  | V_{GS} = 10 V, I_D = 4.4 A, 
                                 |        | see fig. 10 | -    | -    | 7.8  | nC   |
| Turn-on delay time                | t_{on}  | V_{DD} = 125 V, I_D = 4.4 A, 
                                 |        | R_{g} = 18 Ω, R_{D} = 28 Ω | -    | 7.0  | -    | ns   |
| Rise time                         | t_{r}   | f = 1 MHz, open drain | -    | 13   | -    | ns   |
| Turn-off delay time               | t_{off} | f = 1 MHz, open drain | -    | 20   | -    | ns   |
| Fall time                         | t_{f}   | f = 1 MHz, open drain | -    | 12   | -    | ns   |
| Gate input resistance             | R_{g}   | f = 1 MHz, open drain | 0.7  | 5.4  | -    | Ω    |
| Internal drain inductance         | L_{D}   | Between lead, 6 mm (0.25") from 
                                 |        | package and center of 
                                 |        | die contact | -    | 4.5  | -    | nH   |
| Internal source inductance        | L_{S}   | Between lead, 6 mm (0.25") from 
                                 |        | package and center of 
                                 |        | die contact | -    | 7.5  | -    | nH   |

### Drain-Source Body Diode Characteristics

| Continuous source-drain diode current | I_{S}   | MOSFET symbol showing the integral reverse p - n junction diode | -    | -    | 4.4  | A    |
| Pulsed diode forward current a       | I_{SM}  | -    | -    | 14   | A    |
| Body diode voltage                  | V_{SD}  | T_J = 25 °C, I_S = 4.4 A, V_{GS} = 0 V^b  | -    | -    | 1.8  | V    |
| Body diode reverse recovery time     | t_{rr}  | T_J = 25 °C, I_F = 4.4 A, di/dt = 100 A/μs^b | -    | 200  | 400  | ns   |
| Body diode reverse recovery charge   | Q_{rr}  | -    | 0.93 | 1.9  | μC   |
| Forward turn-on time                 | t_{on}  | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | -    | -    | -    | -    |

### Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics, T_C = 25 °C**

**Fig. 2 - Typical Output Characteristics, T_C = 150 °C**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**
Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 8 - Maximum Safe Operating Area

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms
Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current
Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

Circuit layout considerations:
- Low stray inductance
- Ground plane
- Low leakage inductance
- Current transformer

- dV/dt controlled by Rg
- Driver same type as D.U.T.
- Igd controlled by duty factor “D”
- D.U.T. - device under test

Driver gate drive

Reverse recovery current

Re-applied voltage

Inductor current

Body diode forward drop

Ripple ≤ 5 %

Note:
- a. Vgs = 5 V for logic level devices

Fig. 14 - For N-Channel

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