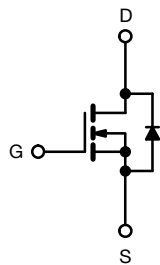
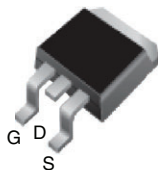


Power MOSFET

D²PAK (TO-263)

N-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	200	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.40
Q_g max. (nC)	43	
Q_{gs} (nC)	7.0	
Q_{gd} (nC)	23	
Configuration	Single	

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dv/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details



RoHS*
Available
HALOGEN
FREE
Available

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface-mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface-mount application.

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHF630S-GE3	SiHF630STRL-GE3 a	SiHF630STRR-GE3 a
Lead (Pb)-free	IRF630SPbF	IRF630STRLPbF a	IRF630STRRPbF a

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	200	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed drain current ^a	I_{DM}	36	W/ $^\circ\text{C}$
Linear derating factor		0.59	
Linear derating factor (PCB mount) ^e		0.025	mJ
Single pulse avalanche energy ^b	E_{AS}	250	
Repetitive avalanche current ^a	I_{AR}	9.0	A
Repetitive avalanche energy ^a	E_{AR}	7.4	mJ
Maximum power dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	W
Maximum power dissipation (PCB mount) ^e		$T_A = 25\text{ }^\circ\text{C}$	
Peak diode recovery dv/dt ^c	dv/dt	5.0	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) ^d	for 10 s	300	

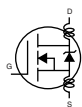

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 4.6\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 9.0\text{ A}$ (see fig. 12)
- $I_{SD} \leq 9.0\text{ A}$, $di/dt \leq 120\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum junction-to-ambient (PCB mount) ^c	R_{thJA}	-	-	40	°C/W
Maximum junction-to-ambient	R_{thJA}	-	-	62	
Maximum junction-to-case (drain)	R_{thJC}	-	-	1.7	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

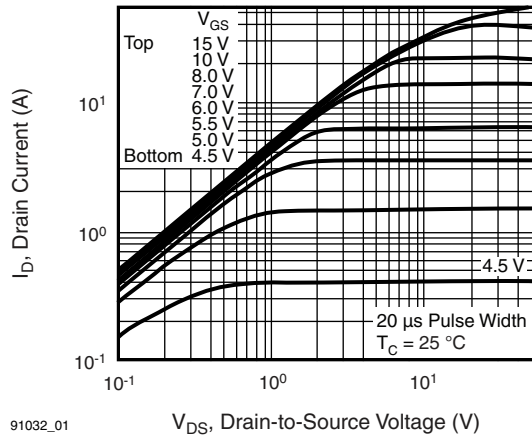
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		200	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.24	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 200 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 160V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 5.4 A ^b	-	-	0.40	Ω
Forward transconductance	g _{fs}	V _{DS} = 50 V, I _D = 5.4 A ^b		3.8	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	800	-	pF
Output capacitance	C _{oss}			-	240	-	
Reverse transfer capacitance	C _{rss}			-	76	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 5.9 A, V _{DS} = 160 V see fig. 6 and 13 ^b	-	-	43	nC
Gate-source charge	Q _{gs}			-	-	7.0	
Gate-drain charge	Q _{gd}			-	-	23	
Turn-on delay time	t _{d(on)}	V _{DD} = 100 V, I _D = 5.9 A R _g = 12 Ω, R _D = 16 Ω see fig. 10 ^b		-	9.4	-	ns
Rise time	t _r			-	28	-	
Turn-off delay time	t _{d(off)}			-	39	-	
Fall time	t _f			-	20	-	
Gate input resistance	R _g	f = 1 MHz, open drain		0.6	-	3.3	Ω
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal source inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	9.0	A
Pulsed diode forward current ^a	I _{SM}			-	-	36	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 9.0 A, V _{GS} = 0 V ^b		-	-	2.0	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 5.9 A, di/dt = 100 A/μs ^b		-	170	340	ns
Body diode reverse recovery charge	Q _{rr}			-	1.1	2.2	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$
- When mounted on 1" square PCB (FR-4 or G-10 material)

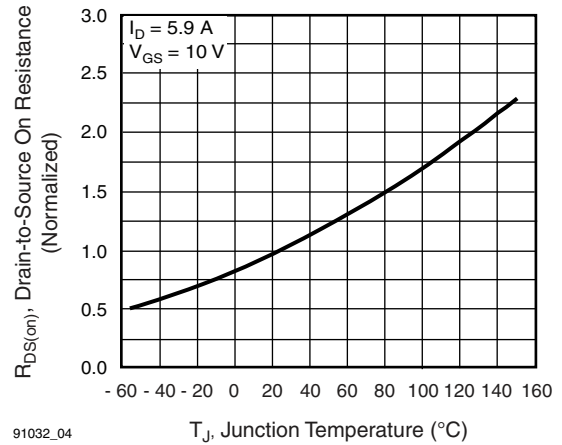


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



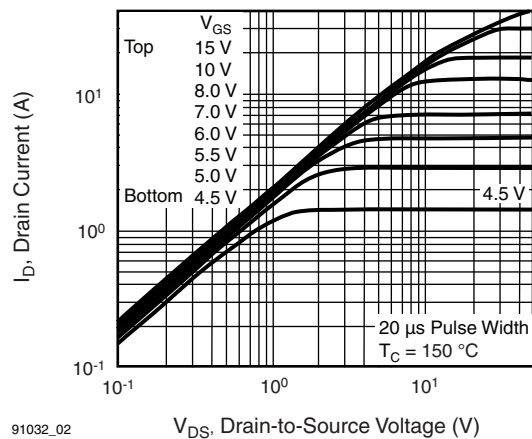
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Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ °C}$



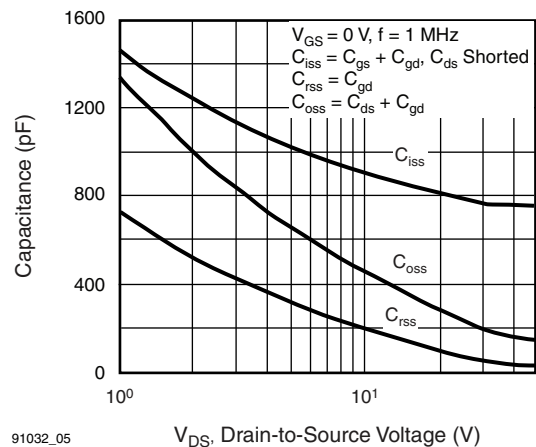
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Fig. 4 - Normalized On-Resistance vs. Temperature



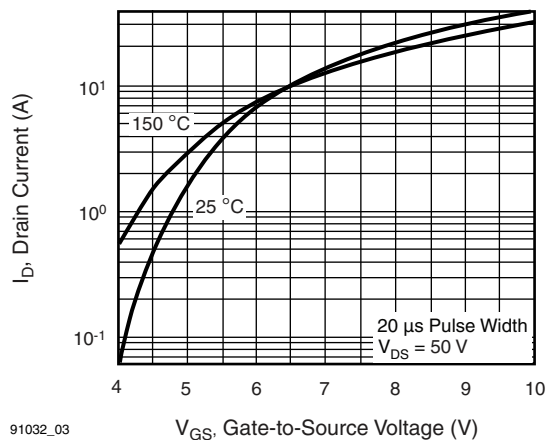
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Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ °C}$



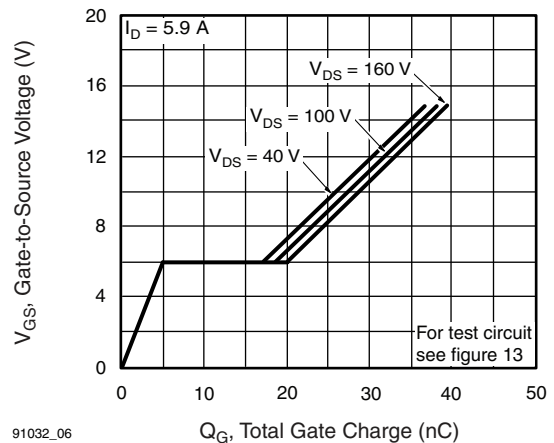
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



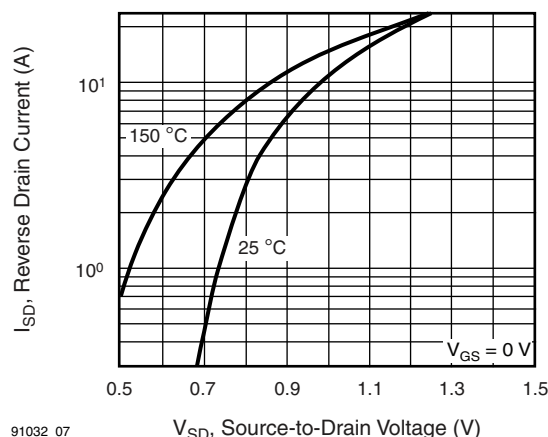
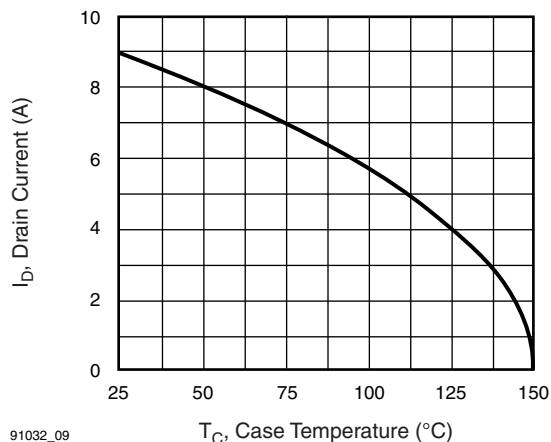
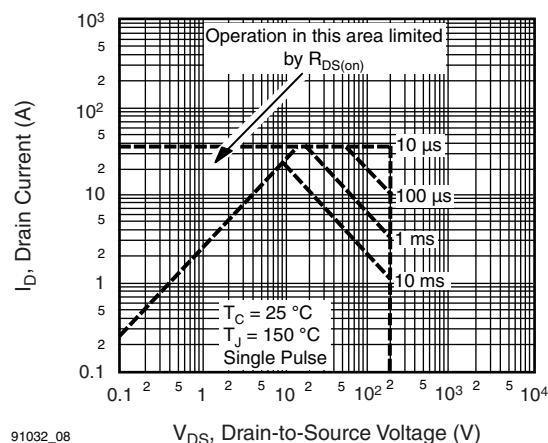
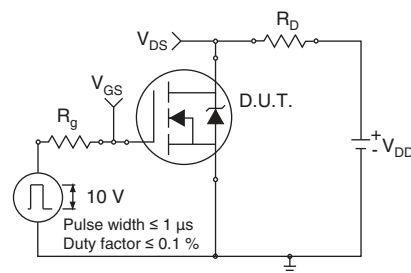
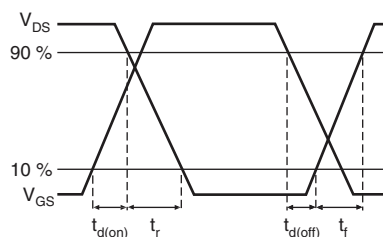
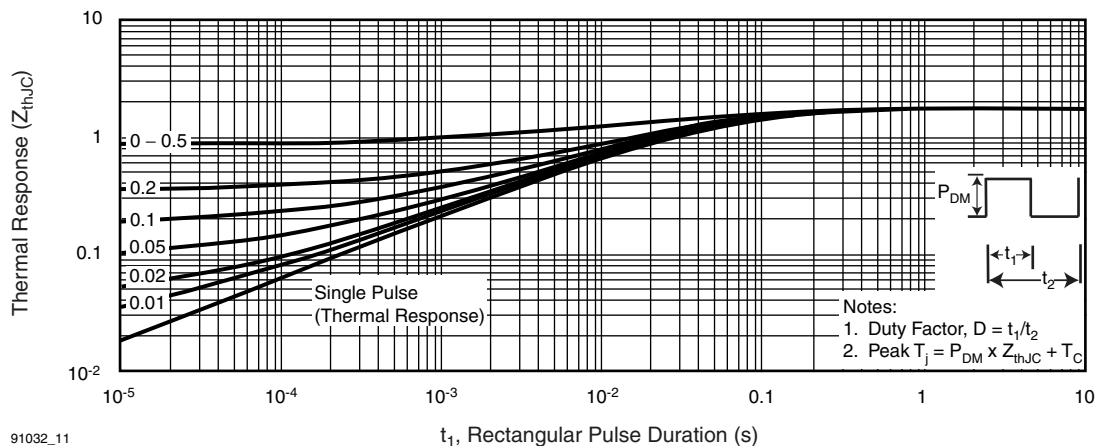
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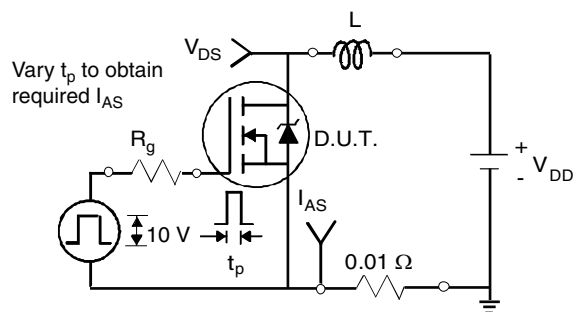
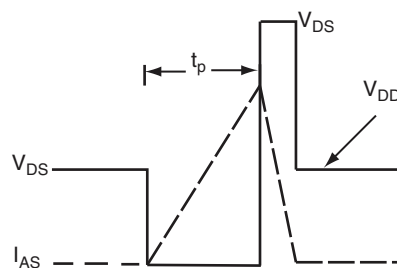
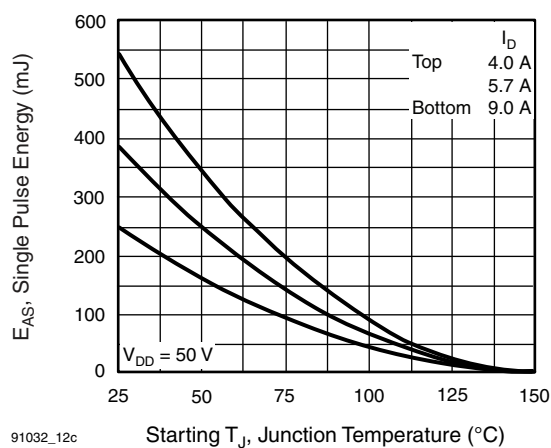
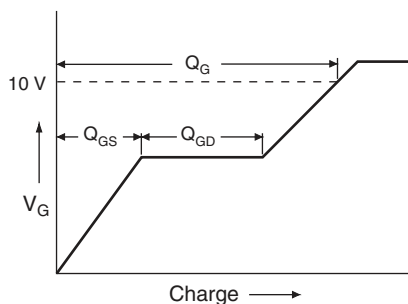
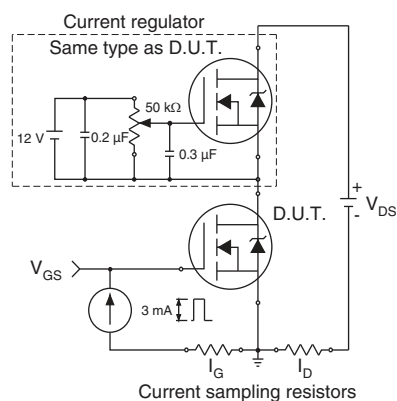
Fig. 3 - Typical Transfer Characteristics

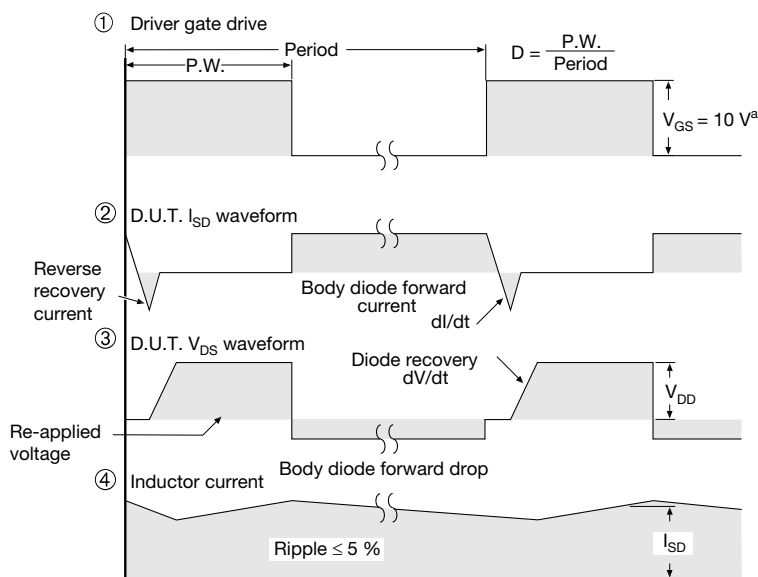
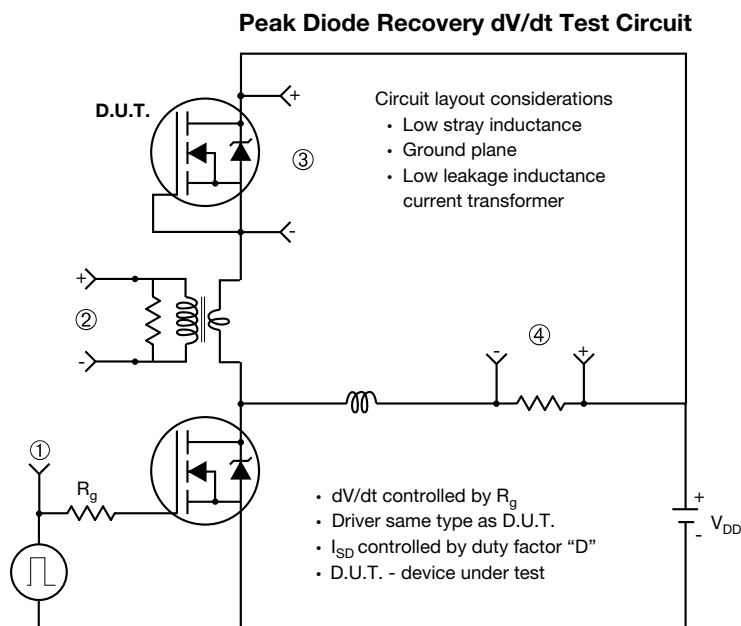


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Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Maximum Safe Operating Area

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

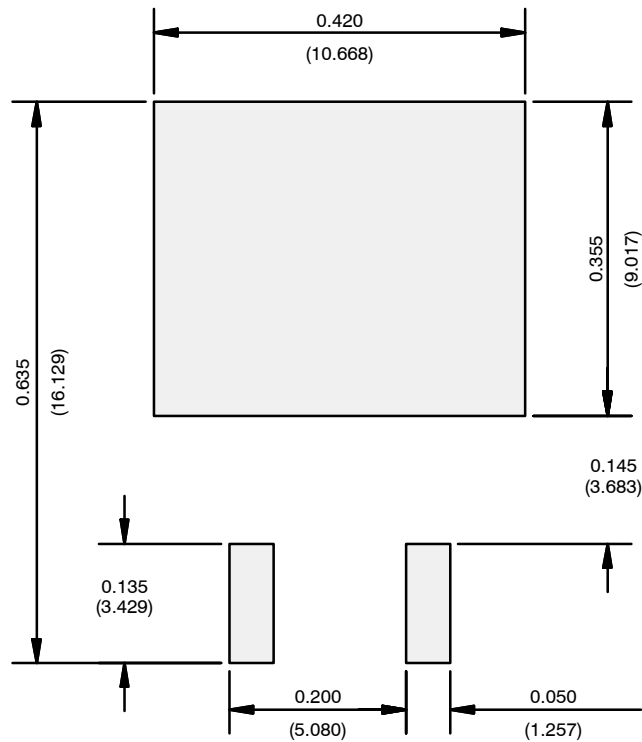

Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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