

# Power MOSFET

**TO-220AB**


N-Channel MOSFET

## FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS\***  
Available

## Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

## DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

## PRODUCT SUMMARY

$V_{DS}$ (V)	250
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$ 0.45
$Q_g$ max. (nC)	41
$Q_{gs}$ (nC)	6.5
$Q_{gd}$ (nC)	22
Configuration	Single

## ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF634PbF

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	250	V
Gate-source voltage	$V_{GS}$	$\pm 20$	
Continuous drain current	$I_D$	$T_C = 25\text{ }^\circ\text{C}$ 8.1	A
		$T_C = 100\text{ }^\circ\text{C}$ 5.1	
Pulsed drain current <sup>a</sup>	$I_{DM}$	32	
Linear derating factor		0.59	W/ $^\circ\text{C}$
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	300	mJ
Repetitive avalanche current <sup>a</sup>	$I_{AR}$	8.1	A
Repetitive avalanche energy <sup>a</sup>	$E_{AR}$	7.4	mJ
Maximum power dissipation	$P_D$	74	W
Peak diode recovery dV/dt <sup>c</sup>	dV/dt	4.8	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s	300	
Mounting torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

## Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 7.3\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 8.1\text{ A}$  (see fig. 12)
- $I_{SD} \leq 8.1\text{ A}$ ,  $dI/dt \leq 120\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

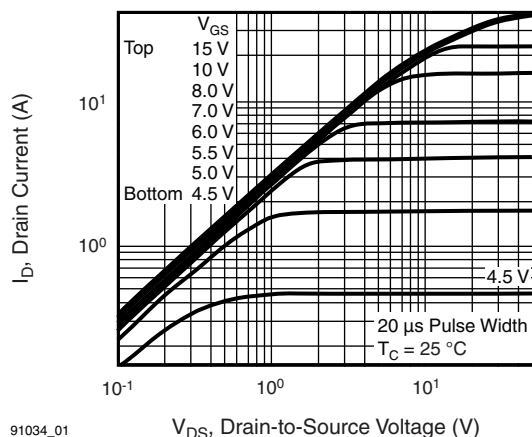
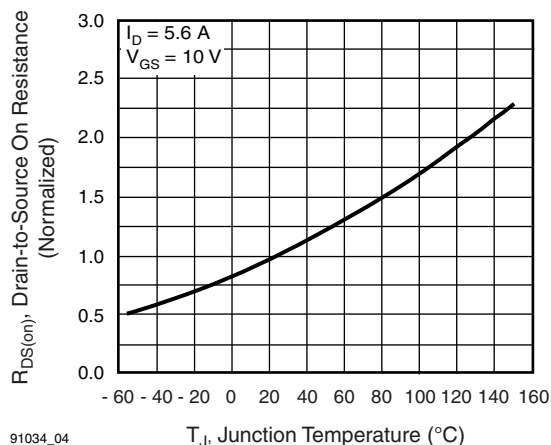
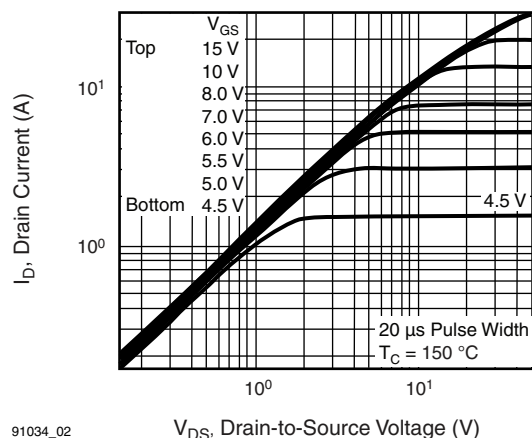
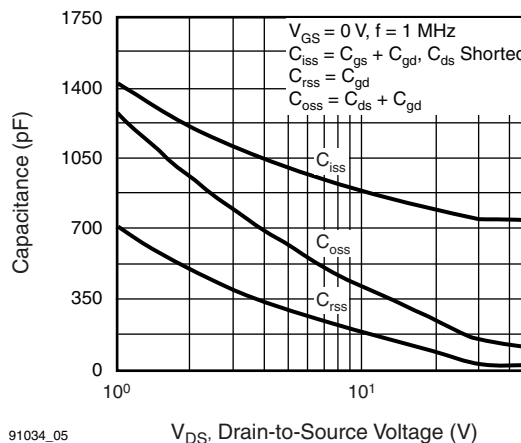
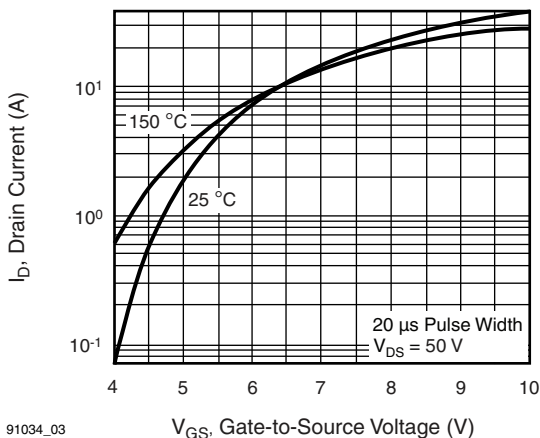
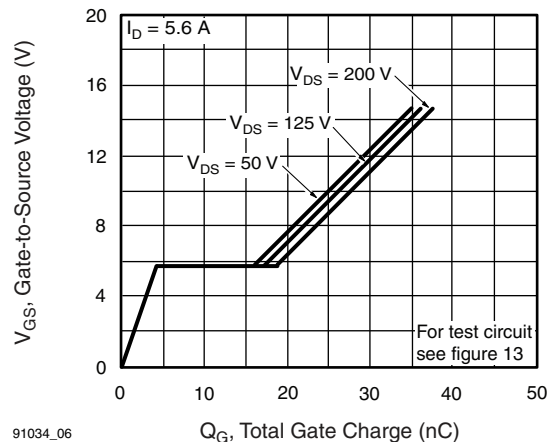
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	62	°C/W
Case-to-sink, flat, greased surface	$R_{thCS}$	0.50	-	
Maximum junction-to-case (drain)	$R_{thJC}$	-	1.7	

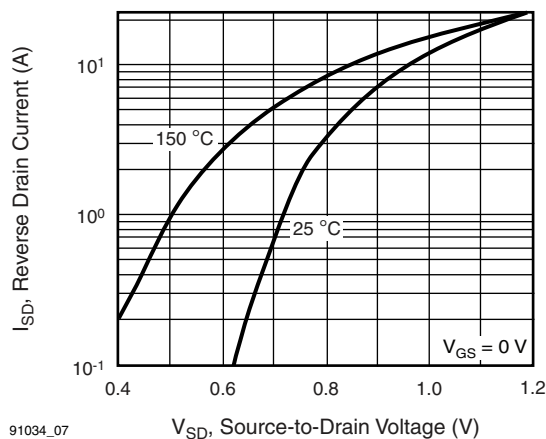
**SPECIFICATIONS** ( $T_J = 25\text{ °C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		250	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.37	-	V/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 250 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 5.1 A <sup>b</sup>	-	-	0.45	Ω
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 5.1 A <sup>b</sup>		1.6	-	-	S
Dynamic							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	770	-	pF
Output capacitance	C <sub>oss</sub>			-	190	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	52	-	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 5.6 A, V <sub>DS</sub> = 200 V, see fig. 6 and 13 <sup>b</sup>	-	-	41	nC
Gate-source charge	Q <sub>gs</sub>			-	-	6.5	
Gate-drain charge	Q <sub>gd</sub>			-	-	22	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 125 V, I <sub>D</sub> = 5.6 A, R <sub>g</sub> = 12 Ω, R <sub>D</sub> = 22 Ω, see fig. 10 <sup>b</sup>		-	9.6	-	ns
Rise time	t <sub>r</sub>			-	21	-	
Turn-off delay time	t <sub>d(off)</sub>			-	42	-	
Fall time	t <sub>f</sub>			-	19	-	
Gate input resistance	R <sub>g</sub>	f = 1 MHz, open drain		0.6	-	2.9	Ω
Internal drain inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal source inductance	L <sub>S</sub>			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	8.1	A
Pulsed diode forward current <sup>a</sup>	I <sub>SM</sub>			-	-	32	
Body diode voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 8.1 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	2.0	V
Body diode reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 5.6 A, dI/dt = 100 A/μs <sup>b</sup>		-	220	440	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	1.2	2.4	μC
Forward turn-on time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

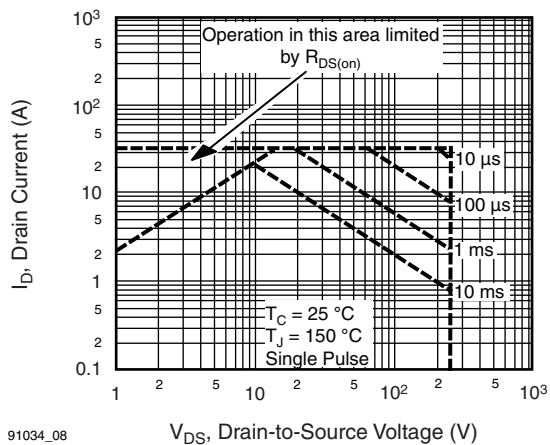
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$

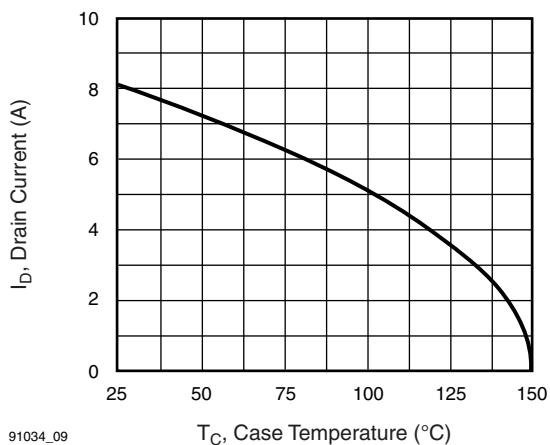
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$** 

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



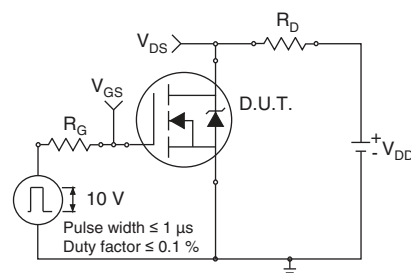
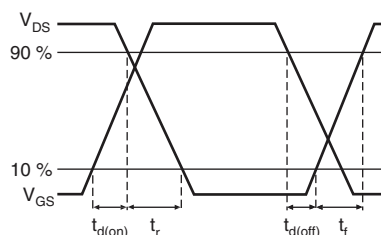
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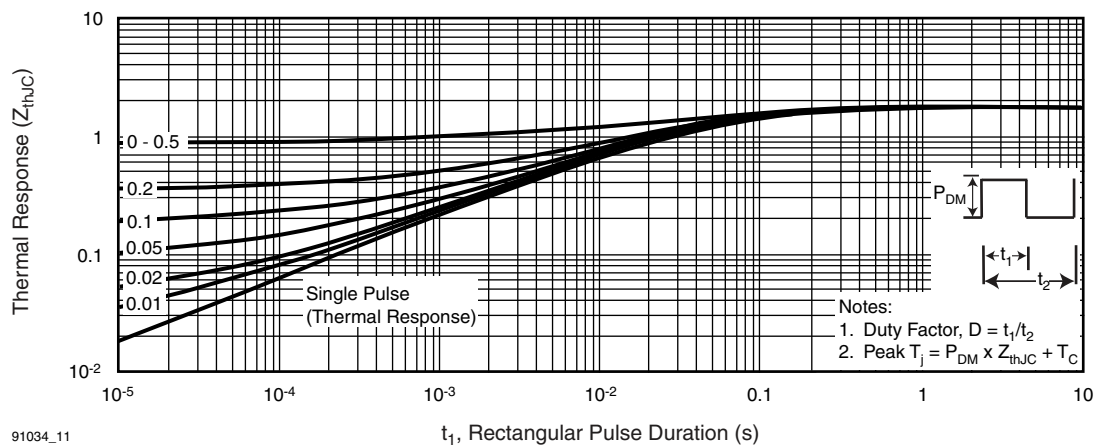
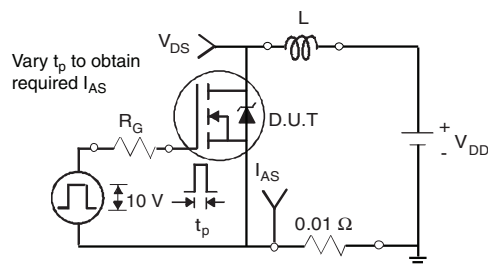
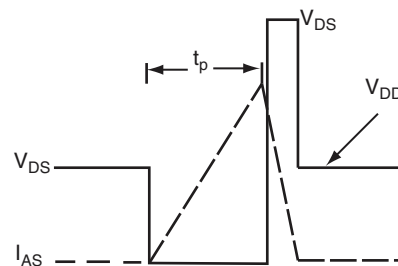
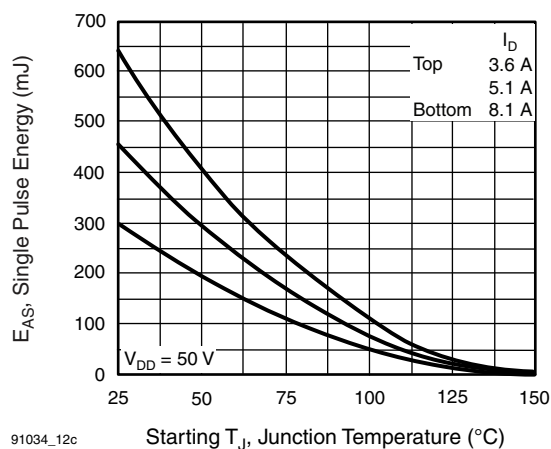
**Fig. 7 - Typical Source-Drain Diode Forward Voltage**


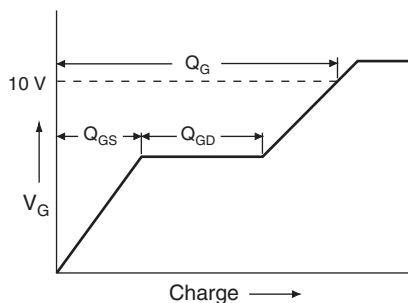
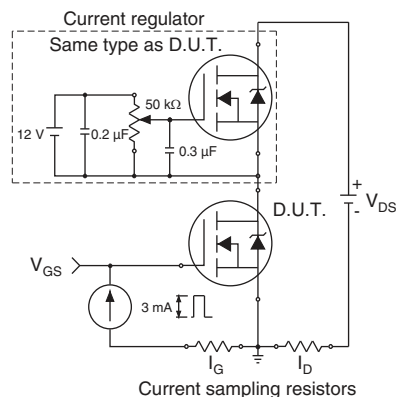
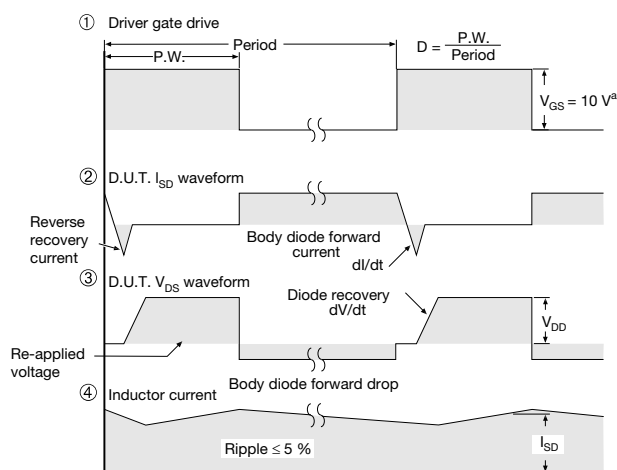
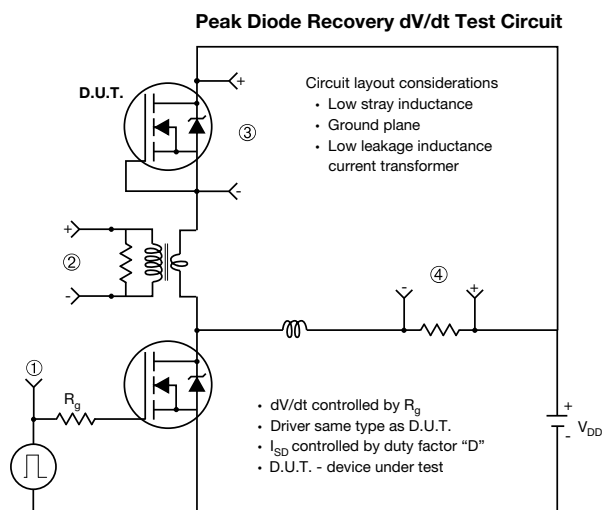
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**Fig. 8 - Maximum Safe Operating Area**


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**Fig. 9 - Maximum Drain Current vs. Case Temperature**

**Fig. 10a - Switching Time Test Circuit**

**Fig. 10b - Switching Time Waveforms**


**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig. 12a - Unclamped Inductive Test Circuit**

**Fig. 12b - Unclamped Inductive Waveforms**

**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**


**Fig. 13a - Basic Gate Charge Waveform**

**Fig. 13b - Gate Charge Test Circuit**

**Note**

a.  $V_{GS} = 5V$  for logic level devices

**Fig. 14 - For N-Channel**

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