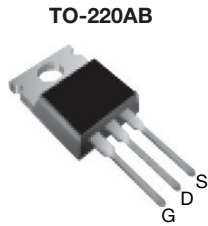


Power MOSFET



N-Channel MOSFET

FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective C_{oss} specified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


 Available
RoHS*
 Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching

TYPICAL SMPS TOPOLOGIES

- Single transistor flyback Xfmr. reset
- Single transistor forward Xfmr. reset (both US line input only)

PRODUCT SUMMARY	
V_{DS} (V)	400
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 1.0
Q_g max. (nC)	22
Q_{gs} (nC)	5.8
Q_{gd} (nC)	9.3
Configuration	Single


ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF730APbF
Lead (Pb)-free and halogen-free	IRF730APbF-BE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	400	V	
Gate-source voltage	V_{GS}	± 30		
Continuous drain current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A	
		$T_C = 100\text{ }^\circ\text{C}$		
Pulsed drain current ^a	I_{DM}	22		
Linear derating factor		0.6	W/ $^\circ\text{C}$	
Single pulse avalanche energy ^b	E_{AS}	290	mJ	
Repetitive avalanche current ^a	I_{AR}	5.5	A	
Repetitive avalanche energy ^a	E_{AR}	7.4	mJ	
Maximum power dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	74	W
Peak diode recovery dV/dt ^c	dV/dt	4.6	V/ns	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
Soldering recommendations (peak temperature) ^d	For 10 s	300		
Mounting torque	6-32 or M3 screw		10	lbf · in
			1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 19\text{ mH}$, $R_g = 25\text{ }^\circ\Omega$, $I_{AS} = 5.5\text{ A}$ (see fig. 12)
- $I_{SD} \leq 5.5\text{ A}$, $dI/dt \leq 90\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case

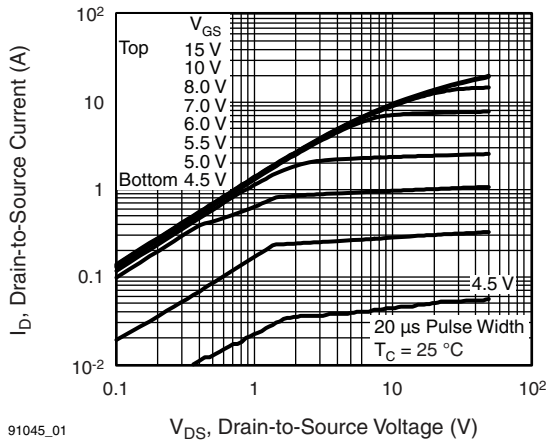
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJC}	-	1.70	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJA}	-	62	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	400	-	-	V	
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.5	-	V/°C	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.5	V	
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 400\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	25	μA	
		$V_{DS} = 320\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	250		
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 3.3\text{ A}^b$	-	-	1.0	Ω	
Forward transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 3.3\text{ A}$	3.1	-	-	S	
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5	-	600	-	pF	
Output capacitance	C_{oss}		-	103	-		
Reverse transfer capacitance	C_{rss}		-	4.0	-		
Output capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}$, $f = 1.0\text{ MHz}$	-	890	-	
Effective output capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 320\text{ V}$, $f = 1.0\text{ MHz}$	-	30	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$V_{DS} = 0\text{ V to } 320\text{ V}^c$	-	45	-	
Gate-source charge	Q_{gs}		$I_D = 3.5\text{ A}$, $V_{DS} = 320\text{ V}$ see fig. 6 and 13 ^b	-	-	22	nC
Gate-drain charge	Q_{gd}			-	-	5.8	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 200\text{ V}$, $I_D = 3.5\text{ A}$ $R_g = 12\text{ }\Omega$, $R_D = 57\text{ }\Omega$, see fig. 10 ^b	-	10	-	ns	
Rise time	t_r		-	22	-		
Turn-off delay time	$t_{d(off)}$		-	20	-		
Fall time	t_f		-	16	-		
Gate input resistance	R_g	$f = 1\text{ MHz}$, open drain	2.7	-	10.9	Ω	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	5.5	A	
Pulsed diode forward current ^a	I_{SM}		-	-	22		
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 5.5\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	1.6	V	
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 3.5\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	370	550	ns	
Body diode reverse recovery charge	Q_{rr}		-	1.6	2.4	μC	
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

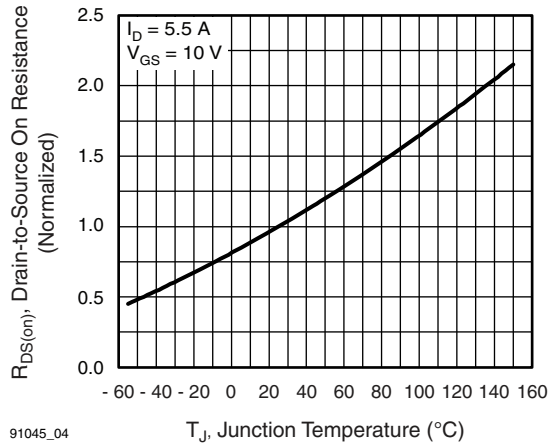
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



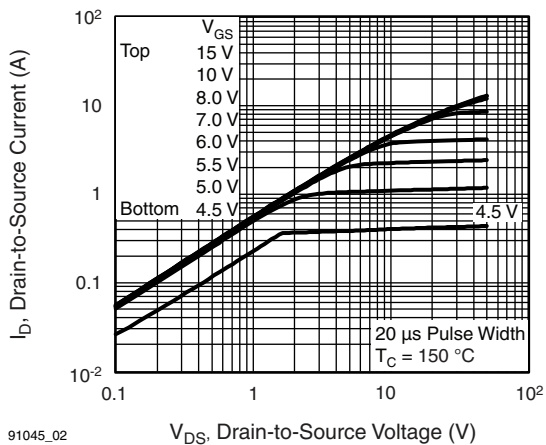
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Fig. 1 - Typical Output Characteristics



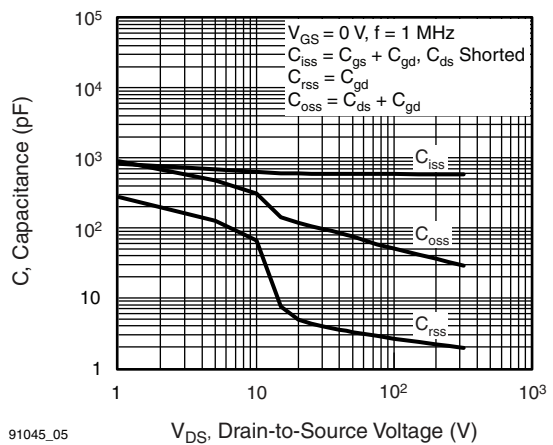
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Fig. 4 - Normalized On-Resistance vs. Temperature



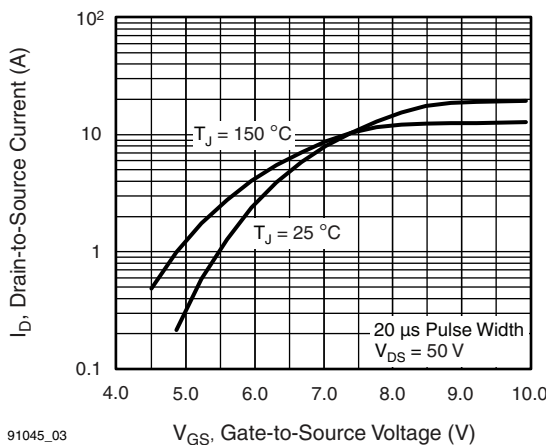
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Fig. 2 - Typical Output Characteristics



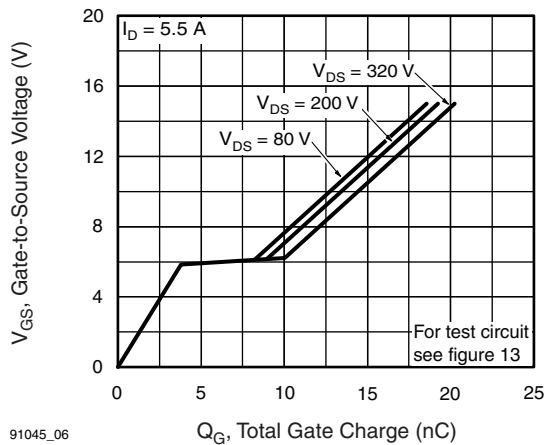
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



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Fig. 3 - Typical Transfer Characteristics



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Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

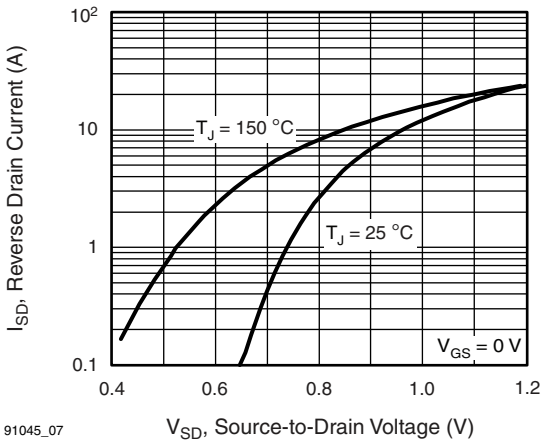


Fig. 7 - Typical Source-Drain Diode Forward Voltage

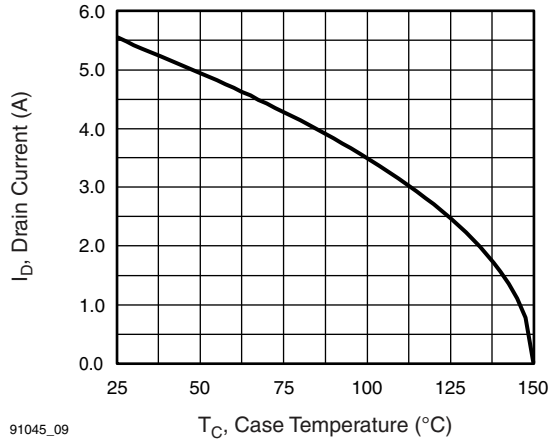


Fig. 9 - Maximum Drain Current vs. Case Temperature

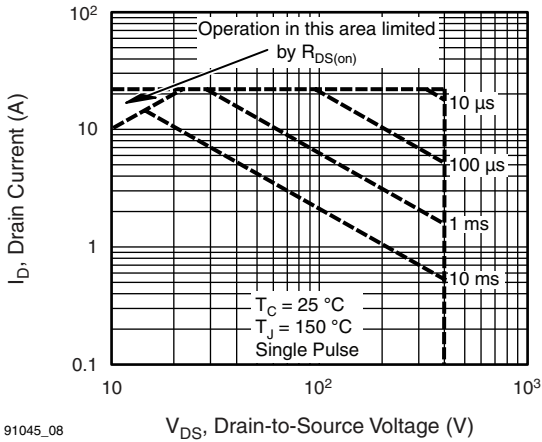


Fig. 8 - Maximum Safe Operating Area

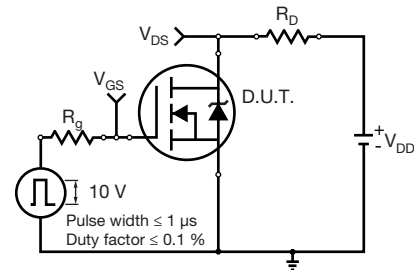


Fig. 10 - Switching Time Test Circuit

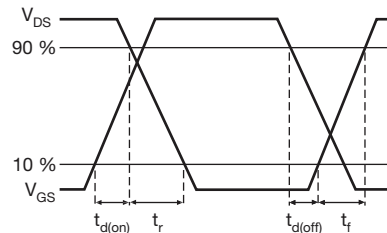


Fig. 11 - Switching Time Waveforms

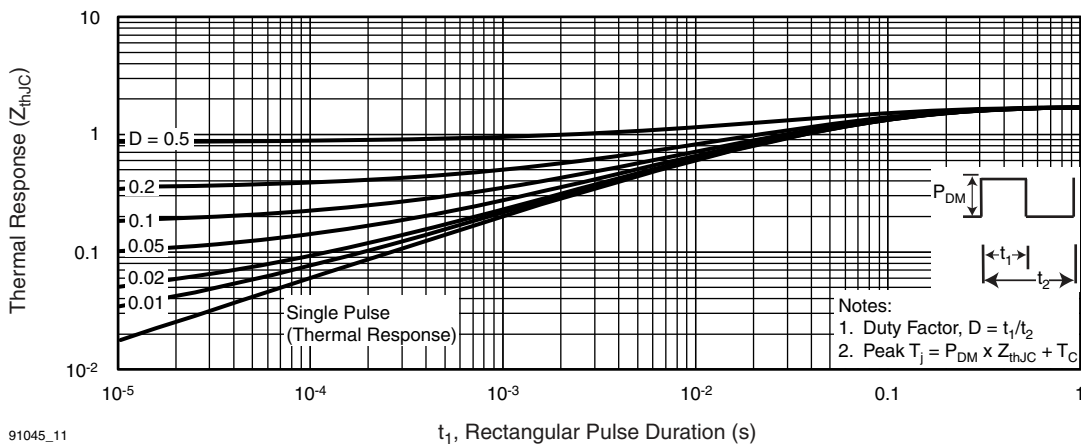


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

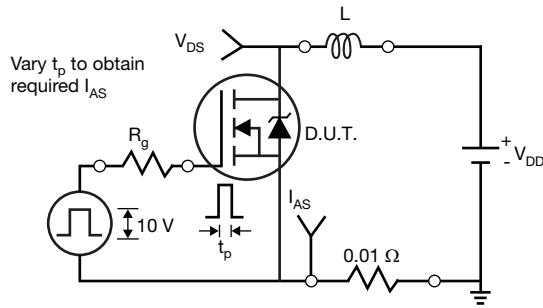


Fig. 13 - Unclamped Inductive Test Circuit

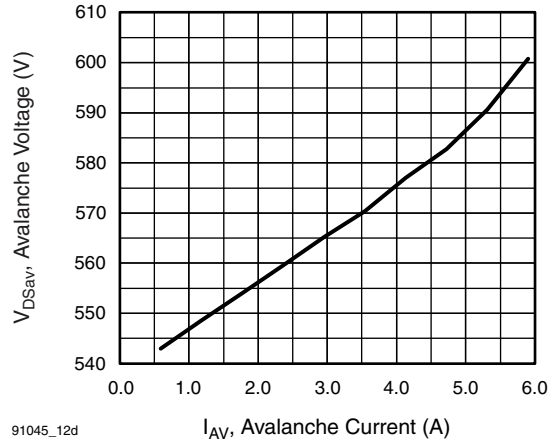


Fig. 16 - Typical Drain Source Voltage vs. Avalanche Current

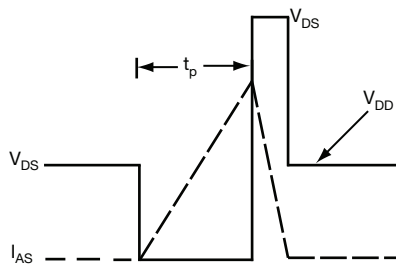


Fig. 14 - Unclamped Inductive Waveforms

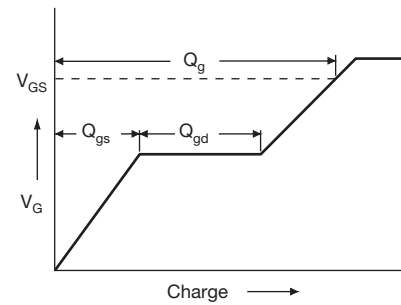


Fig. 17 - Basic Gate Charge Waveform

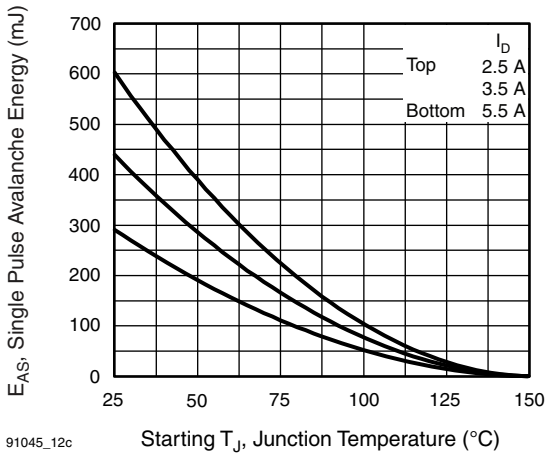


Fig. 15 - Maximum Avalanche Energy vs. Drain Current

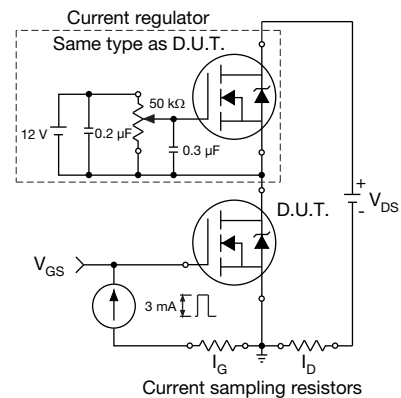


Fig. 18 - Gate Charge Test Circuit

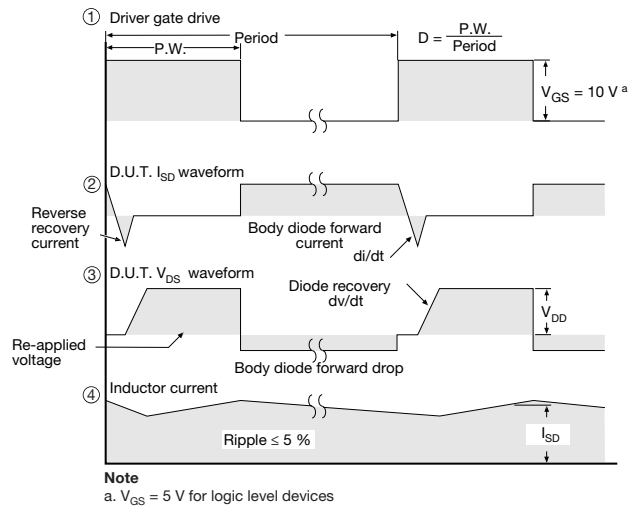
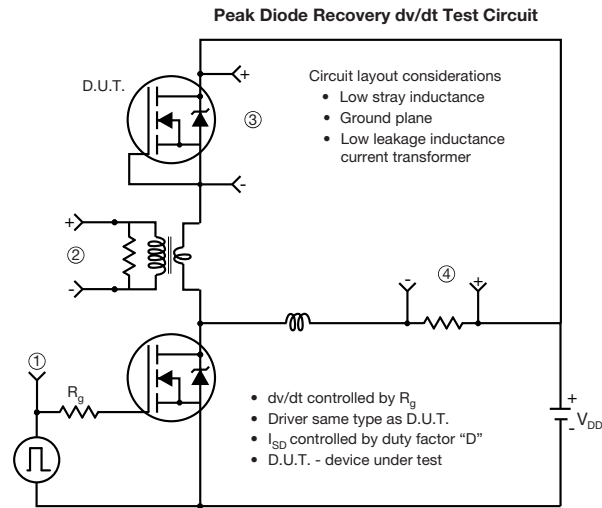


Fig. 19 - For N-Channel

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