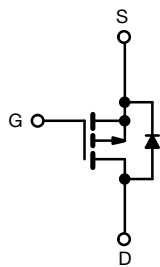
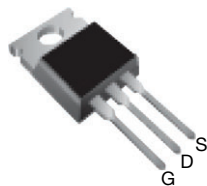


# Power MOSFET

**TO-220AB**


P-Channel MOSFET

## FEATURES

- Dynamic dV/dt rating
- P-channel
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS\***  
Available

## Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

## DESCRIPTION

The power MOSFETs technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of the Power MOSFETs design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

## PRODUCT SUMMARY

$V_{DS}$ (V)	-200	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = -10$ V	3.0
$Q_g$ max. (nC)	11	
$Q_{gs}$ (nC)	7.0	
$Q_{gd}$ (nC)	4.0	
Configuration	Single	

## ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF9610PbF
Lead (Pb)-free and halogen-free	IRF9610PbF-BE3

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V <sub>DS</sub>	-200	V
Gate-source voltage			V <sub>GS</sub>	± 20	
Continuous drain current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	-1.8	A
		T <sub>C</sub> = 100 °C		-1.0	
Pulsed drain current <sup>a</sup>			I <sub>DM</sub>	-7.0	
Linear derating factor				0.16	W/°C
Single pulse avalanche energy <sup>b</sup>			P <sub>D</sub>	20	W
Repetitive avalanche current <sup>a</sup>			I <sub>LM</sub>	-7.0	A
Repetitive avalanche energy <sup>a</sup>			dV/dt	-5.0	V/ns
Maximum power dissipation	T <sub>C</sub> = 25 °C		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Peak diode recovery dV/dt <sup>c</sup>				300	
Operating junction and storage temperature range				10	lbf · in
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s			1.1	N · m

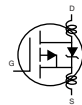

## Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5)
- Not applicable
- $I_{SD} \leq -1.8$  A,  $dI/dt \leq 70$  A/ $\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150^\circ\text{C}$
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

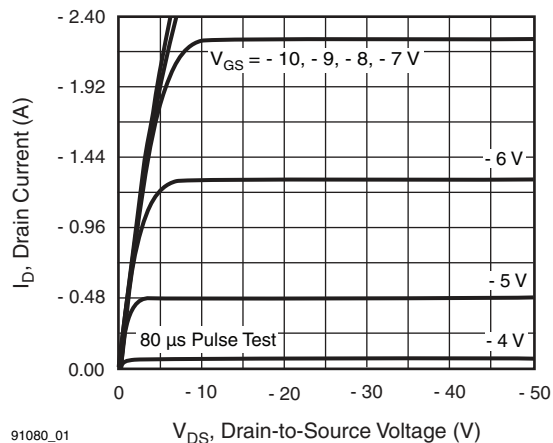
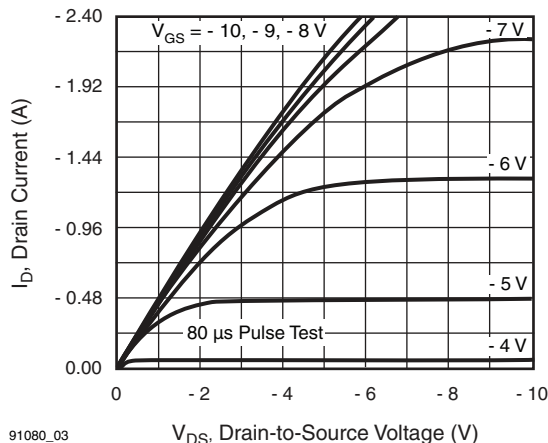
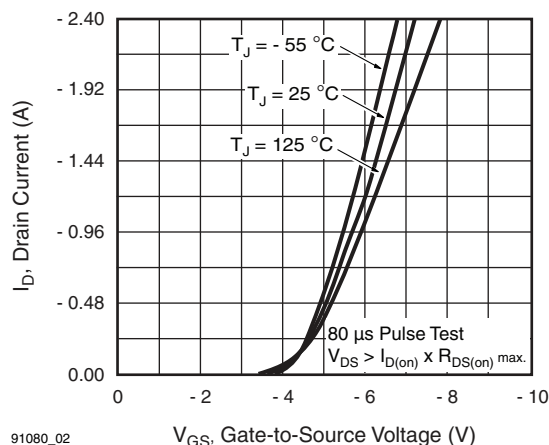
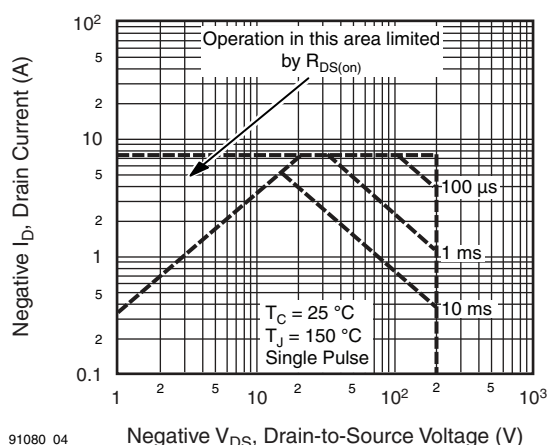
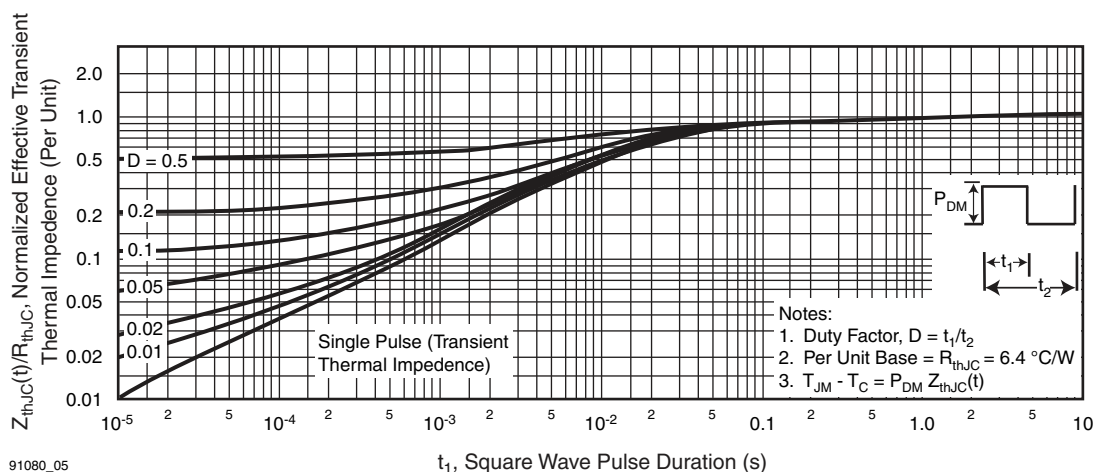
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	62	°C/W
Case-to-sink, flat, greased surface	$R_{thCS}$	0.50	-	
Maximum junction-to-case (drain)	$R_{thJC}$	-	6.4	

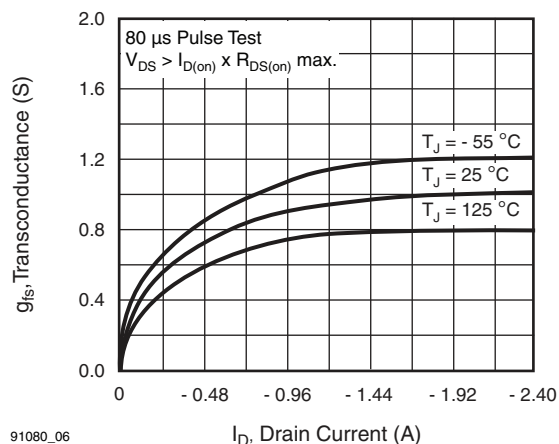
**SPECIFICATIONS** ( $T_J = 25\text{ °C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = -250\text{ }\mu\text{A}$		-200	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = -1\text{ mA}$		-	-0.23	-	V/ $^\circ\text{C}$
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = -250\text{ }\mu\text{A}$		-2.0	-	-4.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = -200\text{ V}$ , $V_{GS} = 0\text{ V}$		-	-	-100	$\mu\text{A}$
		$V_{DS} = -160\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$		-	-	-500	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -0.90\text{ A}^b$	-	-	3.0	$\Omega$
Forward transconductance	$g_{fs}$	$V_{DS} = -50\text{ V}$ , $I_D = -0.90\text{ A}^b$		0.90	-	-	S
Dynamic							
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = -25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 10		-	170	-	pF
Output capacitance	$C_{oss}$			-	50	-	
Reverse transfer capacitance	$C_{rss}$			-	15	-	
Total gate charge	$Q_g$	$V_{GS} = -10\text{ V}$	$I_D = -3.5\text{ A}$ , $V_{DS} = -160\text{ V}$ , see fig. 11 and 18 <sup>b</sup>	-	-	11	nC
Gate-source charge	$Q_{gs}$			-	-	7.0	
Gate-drain charge	$Q_{gd}$			-	-	4.0	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -100\text{ V}$ , $I_D = -0.90\text{ A}$ , $R_g = 50\text{ }\Omega$ , $R_D = 110\text{ }\Omega$ , see fig. 17 <sup>b</sup>		-	8.0	-	ns
Rise time	$t_r$			-	15	-	
Turn-off delay time	$t_{d(off)}$			-	10	-	
Fall time	$t_f$			-	8.0	-	
Gate input resistance	$R_g$	$f = 1\text{ MHz}$ , open drain		2.5	-	14.3	$\Omega$
Internal drain inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal source inductance	$L_S$			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	-1.8	A
Pulsed diode forward current <sup>a</sup>	$I_{SM}$			-	-	-7.0	
Body diode voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_S = -1.8\text{ A}$ , $V_{GS} = 0\text{ V}^b$		-	-	-5.8	V
Body diode reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_F = -1.8\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	240	360	ns
Body diode reverse recovery charge	$Q_{rr}$			-	1.7	2.6	$\mu\text{C}$
Forward turn-on time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

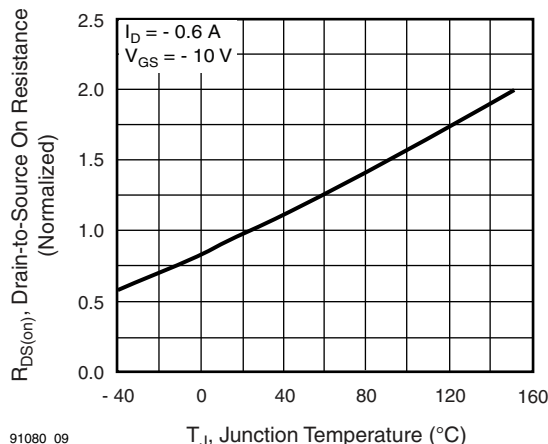
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5)  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$

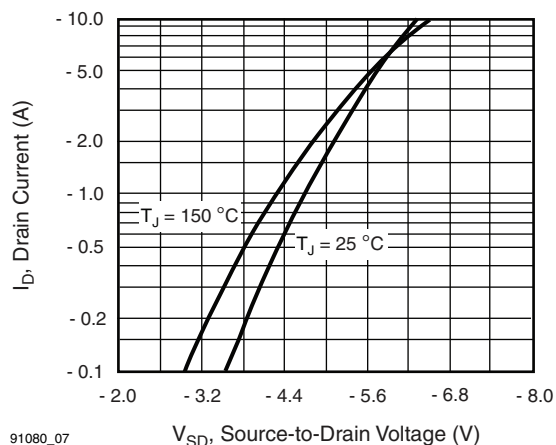
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 3 - Typical Saturation Characteristics**

**Fig. 2 - Typical Transfer Characteristics**

**Fig. 4 - Maximum Safe Operating Area**

**Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration**



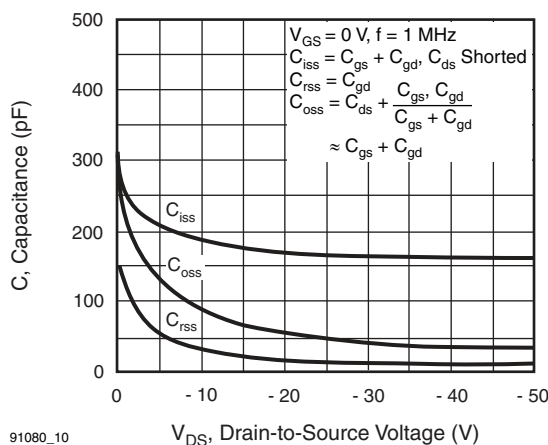
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**Fig. 6 - Typical Transconductance vs. Drain Current**


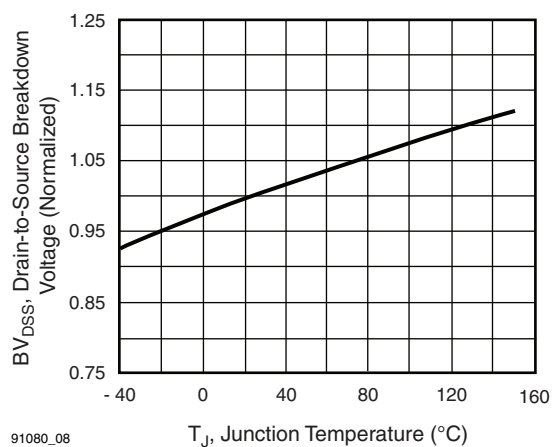
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**Fig. 9 - Normalized On-Resistance vs. Temperature**


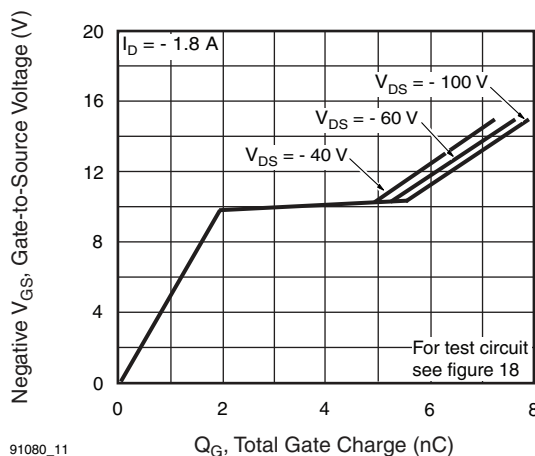
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**Fig. 7 - Typical Source-Drain Diode Forward Voltage**


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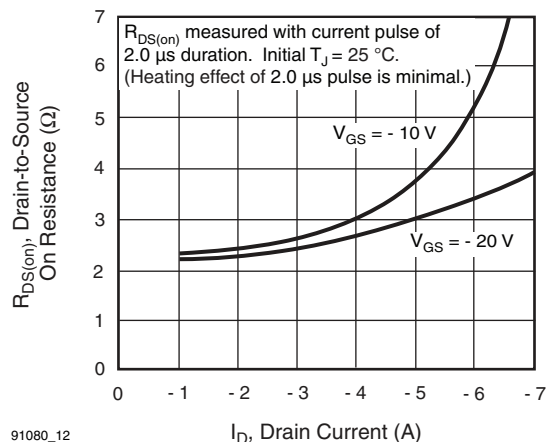
**Fig. 10 - Typical Capacitance vs. Drain-to-Source Voltage**


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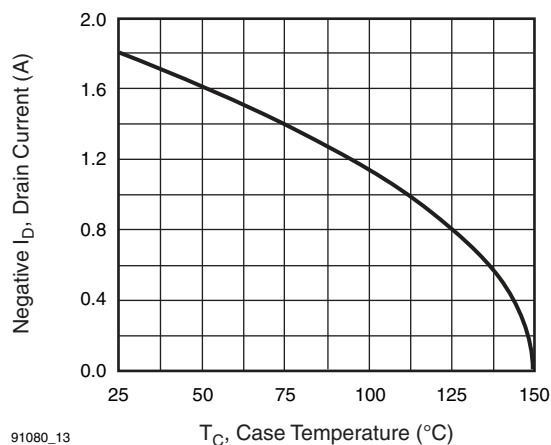
**Fig. 8 - Breakdown Voltage vs. Temperature**


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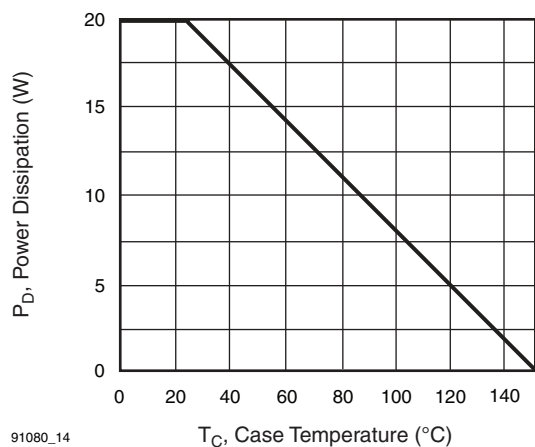
**Fig. 11 - Typical Gate Charge vs. Gate-to-Source Voltage**



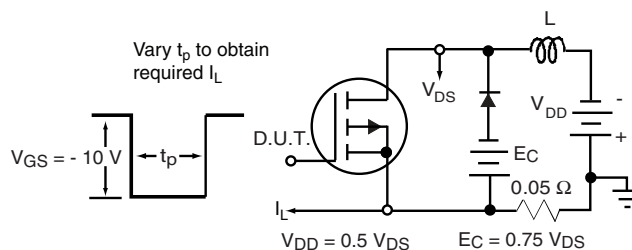
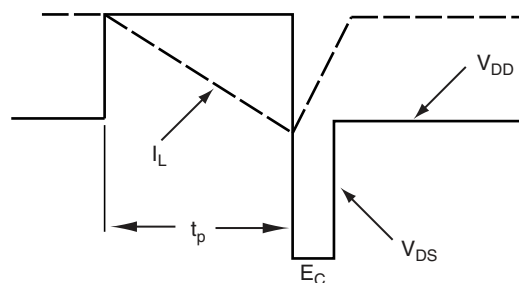
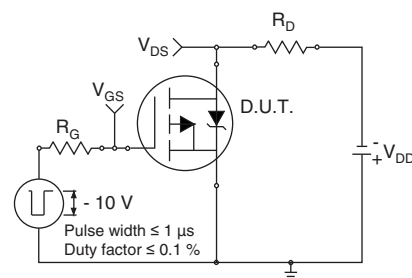
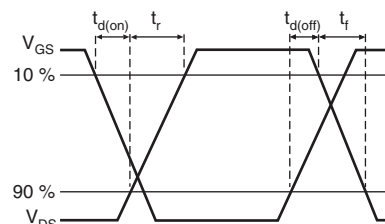
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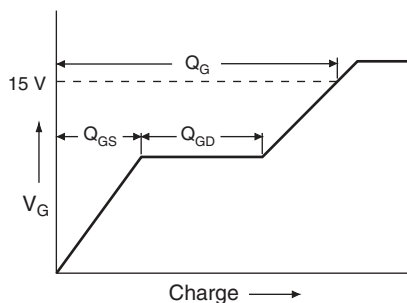
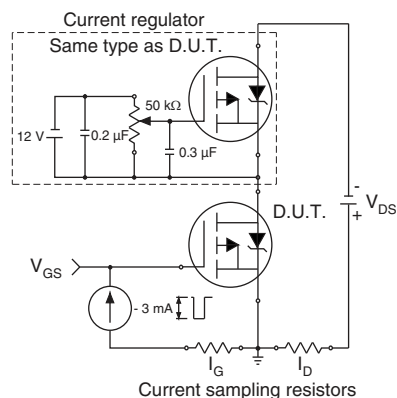
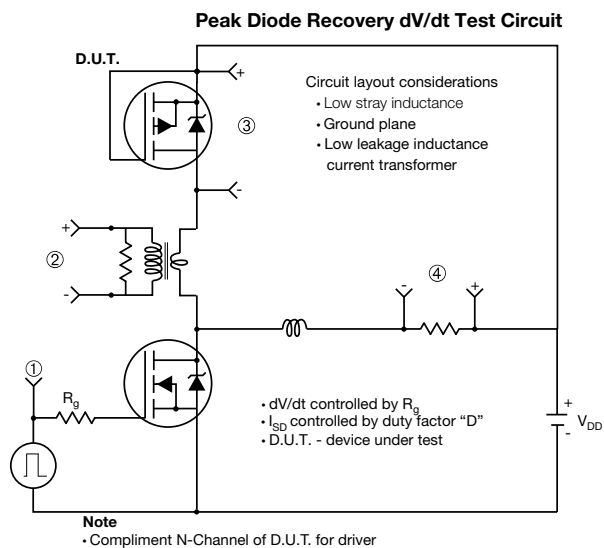
**Fig. 12 - Typical On-Resistance vs. Drain Current**


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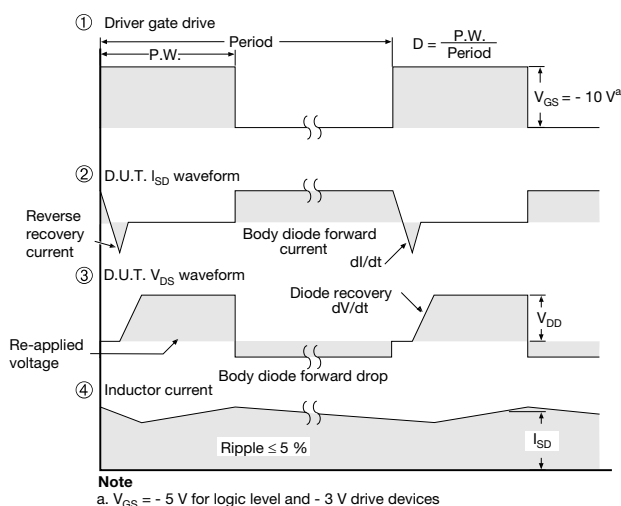
**Fig. 13 - Maximum Drain Current vs. Case Temperature**


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**Fig. 14 - Power vs. Temperature Derating Curve**

**Fig. 15 - Clamped Inductive Test Circuit**

**Fig. 16 - Clamped Inductive Waveforms**

**Fig. 17a - Switching Time Test Circuit**

**Fig. 17b - Switching Time Waveforms**


**Fig. 18a - Basic Gate Charge Waveform**

**Fig. 18b - Gate Charge Test Circuit**


**Note**  
• Compliment N-Channel of D.U.T. for driver



**Note**  
a.  $V_{GS} = -5 V$  for logic level and  $-3 V$  drive devices

**Fig. 19 - For P-Channel**

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