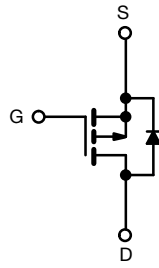


Power MOSFET

TO-220AB


P-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- P-channel
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS*
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

PRODUCT SUMMARY

V_{DS} (V)	-200	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	0.50
Q_g max. (nC)	44	
Q_{gs} (nC)	7.1	
Q_{gd} (nC)	27	
Configuration	Single	

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF9640PbF
Lead (Pb)-free and halogen-free	IRF9640PbF-BE3

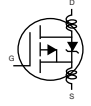

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	-200	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current	V_{GS} at 10 V	$T_C = 25$ °C	-11
		$T_C = 100$ °C	-6.8
Pulsed drain current ^a	I_{DM}	-44	A
Linear derating factor		1.0	W/°C
Single pulse avalanche energy ^b	E_{AS}	700	mJ
Repetitive avalanche current ^a	I_{AR}	-11	A
Repetitive avalanche energy ^a	E_{AR}	13	mJ
Maximum power dissipation	$T_C = 25$ °C	P_D	125
Peak diode recovery dV/dt ^c	dV/dt	-5.0	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^d	For 10 s	300	
Mounting torque	6-32 or M3 screw		10
			1.1

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = -50$ V, starting $T_J = 25$ °C, $L = 8.7$ mH, $R_g = 25$ Ω , $I_{AS} = -11$ A (see fig. 12)
- $I_{SD} \leq -11$ A, $di/dt \leq 150$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C
- 1.6 mm from case

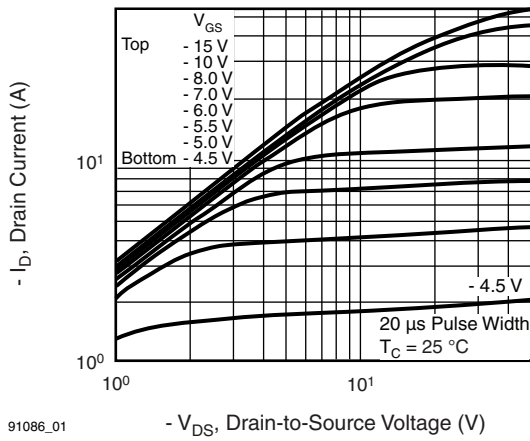
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	1.0	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-200	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = -1\text{ mA}$	-	-0.2	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-2.0	-	-4.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}$	-	-	-100	μA
		$V_{DS} = -160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	-500	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -6.6\text{ A}^b$	-	-	0.50	Ω
Forward transconductance	g_{fs}	$V_{DS} = -50\text{ V}, I_D = -6.6\text{ A}^b$	4.1	-	-	S
Dynamic						
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5	-	1200	-	pF
Output capacitance	C_{oss}		-	370	-	
Reverse transfer capacitance	C_{rss}		-	81	-	
Total gate charge	Q_g	$V_{GS} = -10\text{ V}, I_D = -11\text{ A}, V_{DS} = -160\text{ V}$, see fig. 6 and 13 ^b	-	-	44	nC
Gate-source charge	Q_{gs}		-	-	7.1	
Gate-drain charge	Q_{gd}		-	-	27	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -100\text{ V}, I_D = -11\text{ A}, R_g = 9.1\text{ }\Omega, R_D = 8.6\text{ }\Omega$, see fig. 10 ^b	-	14	-	ns
Rise time	t_r		-	43	-	
Turn-off delay time	$t_{d(off)}$		-	39	-	
Fall time	t_f		-	38	-	
Gate input resistance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal drain inductance	L_S		-	7.5	-	
Internal source inductance	R_g	$f = 1\text{ MHz}$, open drain	0.3	-	1.7	Ω
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p-n junction diode 	-	-	-11	A
Pulsed diode forward current ^a	I_{SM}		-	-	-44	
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = -11\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	-5	V
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = -11\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	250	300	ns
Body diode reverse recovery charge	Q_{rr}		-	2.9	3.6	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

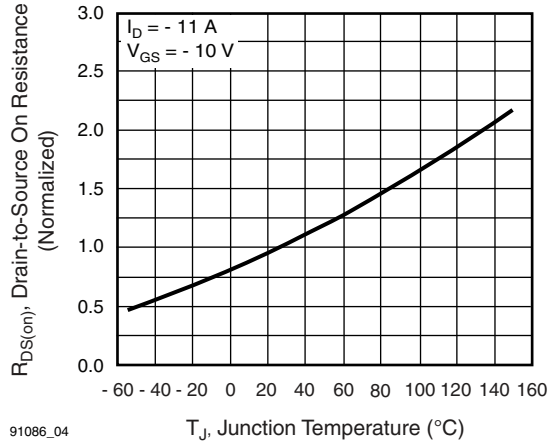
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



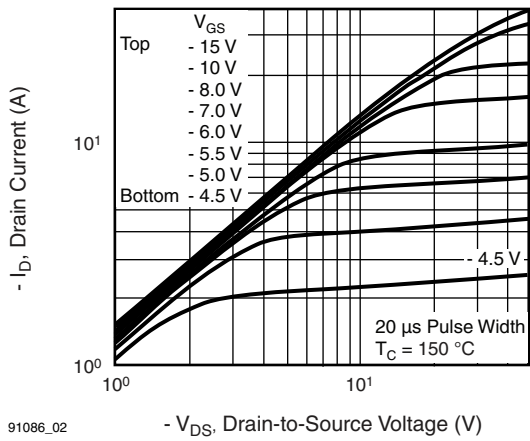
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Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$



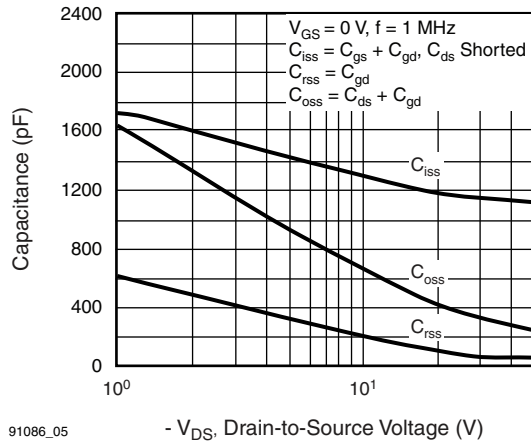
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Fig. 4 - Normalized On-Resistance vs. Temperature



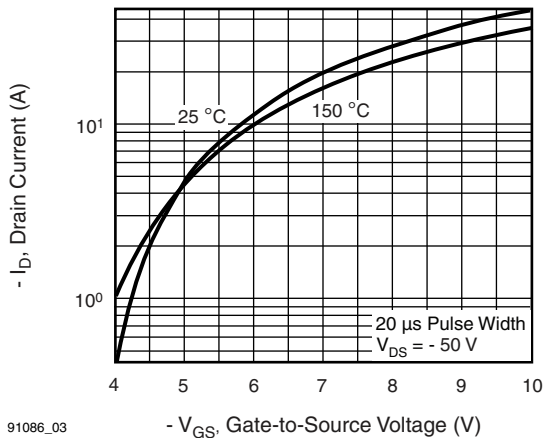
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Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$



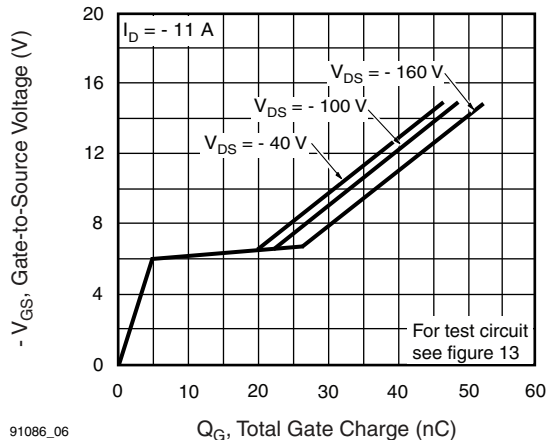
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



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Fig. 3 - Typical Transfer Characteristics



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Fig. 6 - Typical Gate Charge vs. Drain-to-Source Voltage

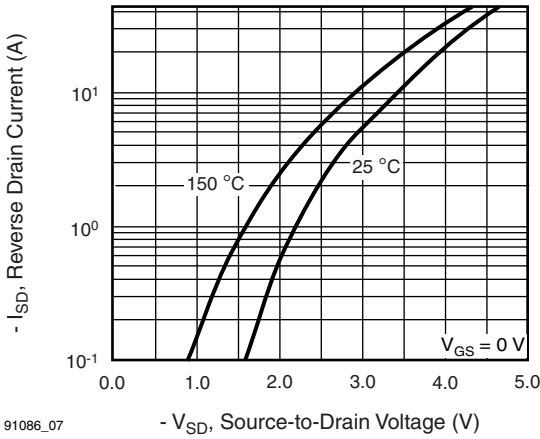


Fig. 7 - Typical Source-Drain Diode Forward Voltage

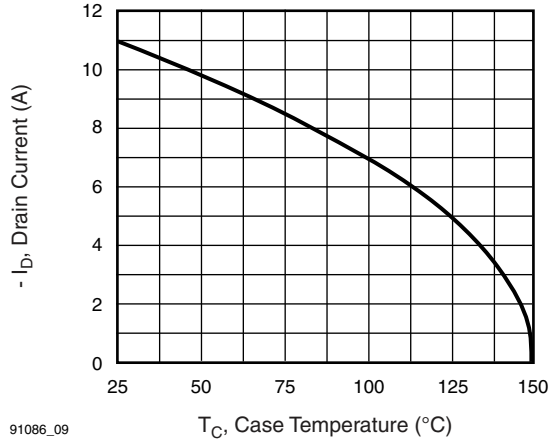


Fig. 9 - Maximum Drain Current vs. Case Temperature

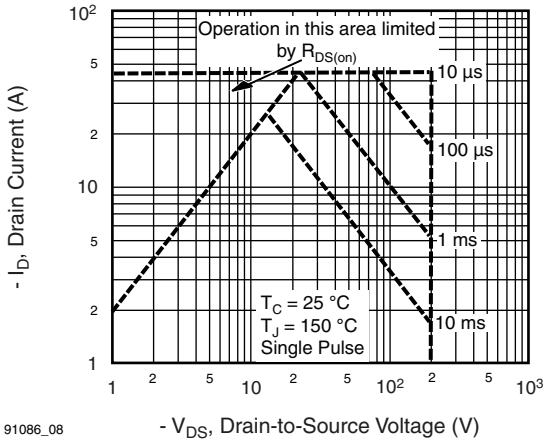


Fig. 8 - Maximum Safe Operating Area

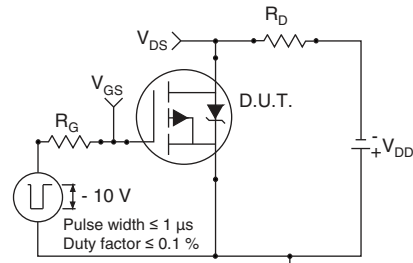


Fig. 10a - Switching Time Test Circuit

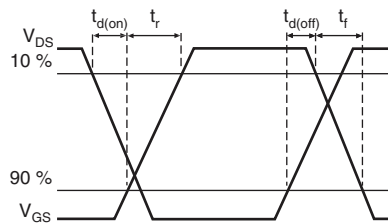


Fig. 10b - Switching Time Waveforms

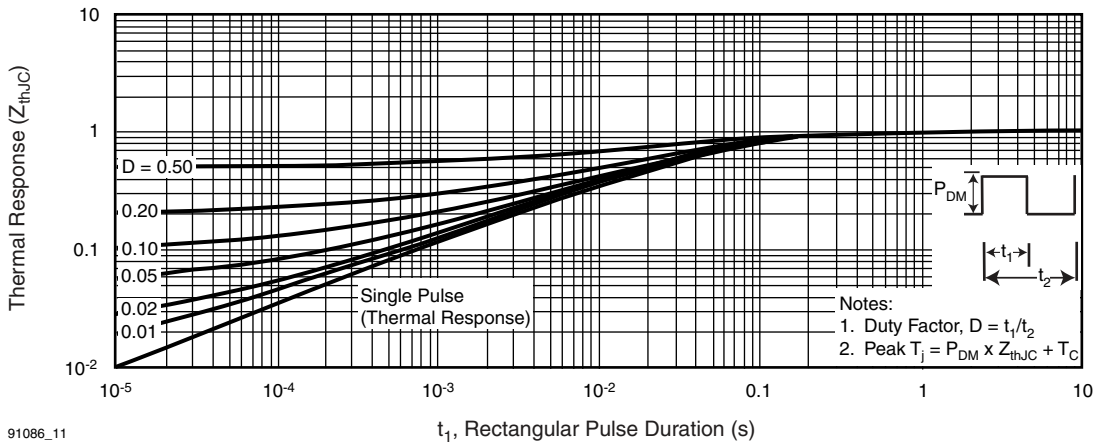


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

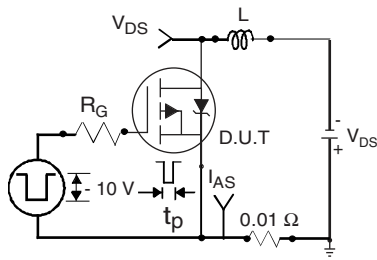


Fig. 12a - Unclamped Inductive Test Circuit

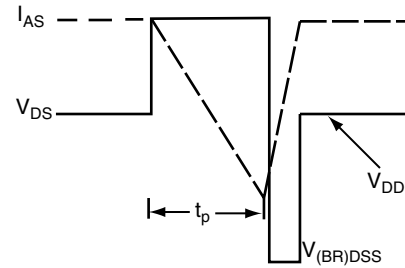


Fig. 12b - Unclamped Inductive Waveforms

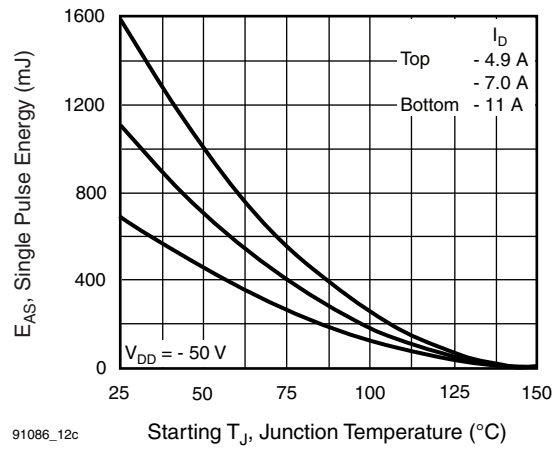


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

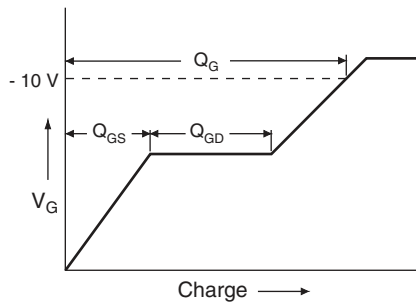


Fig. 13a - Basic Gate Charge Waveform

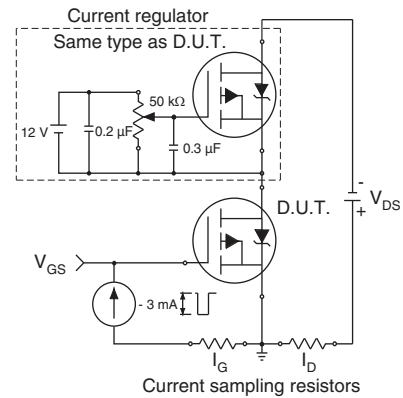
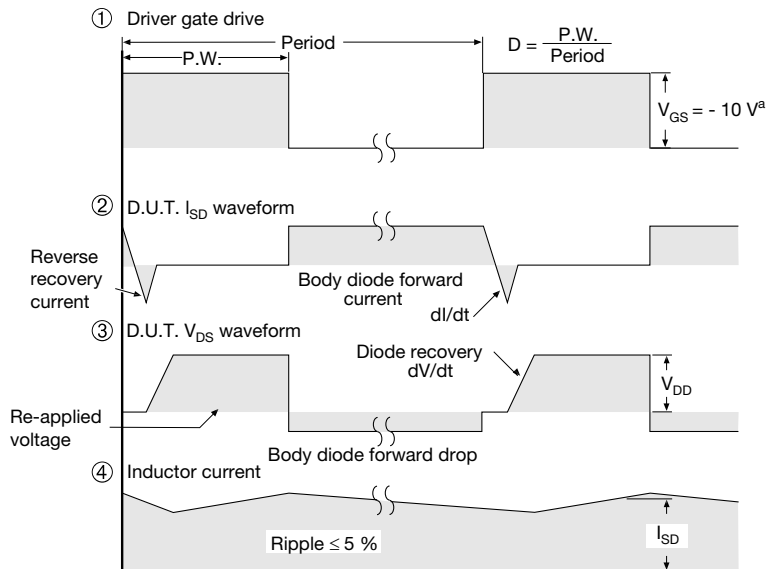
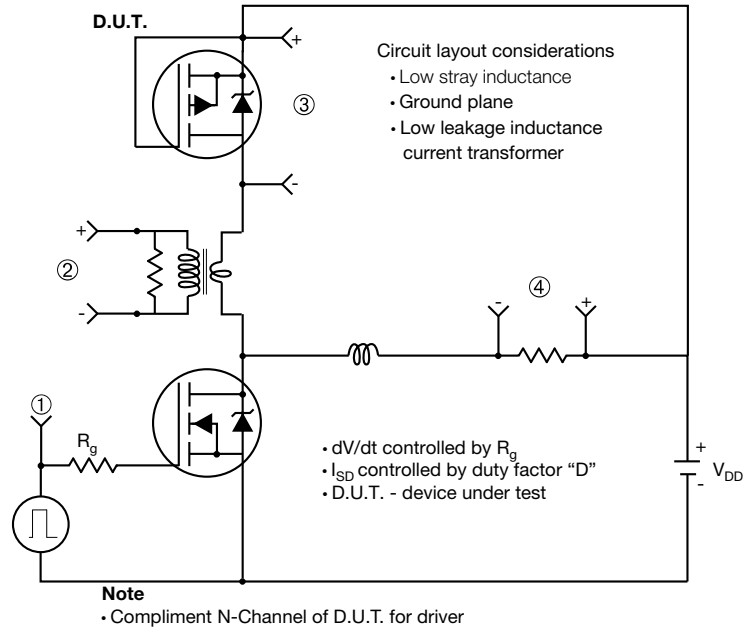


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note
 a. $V_{GS} = -5\text{ V}$ for logic level and -3 V drive devices

Fig. 14 - For P-Channel

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