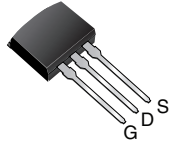
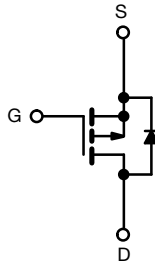
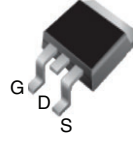


Power MOSFET

I²PAK (TO-262)

D²PAK (TO-263)


P-Channel MOSFET

FEATURES

- Advanced process technology
- Surface-mount (IRF9Z14S, SiHF9Z14S)
- Low-profile through-hole (IRF9Z14L, SiHF9Z14L)
- 175 °C operating temperature
- Fast switching
- P-channel
- Fully avalanche rated
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN FREE
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

PRODUCT SUMMARY

V _{DS} (V)	-60	
R _{DS(on)} (Ω)	V _{GS} = -10 V	0.50
Q _g max. (nC)	12	
Q _{gs} (nC)	3.8	
Q _{gd} (nC)	5.1	
Configuration	Single	

DESCRIPTION

Third generation power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²PAK is a surface-mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

The through-hole version (IRF9Z14L, SiHF9Z14L) is available for low-profile applications.

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHF9Z14S-GE3	SiHF9Z14STRL-GE3 ^a	SiHF9Z14L-GE3
Lead (Pb)-free	IRF9Z14SPbF	IRF9Z14STRLPbF ^a	IRF9Z14LPbF
	IRF9Z14STRRPbF	-	-

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	-60	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current ^e	V _{GS} at -10 V	T _C = 25 °C	-6.7
		T _C = 100 °C	-4.7
Pulsed Drain Current ^{a, e}	I _{DM}	-27	A
Linear Derating Factor		0.29	W/°C
Single Pulse Avalanche Energy ^{b, e}	E _{AS}	140	mJ
Avalanche Current ^a	I _{AR}	-6.7	A
Repetitive Avalanche Energy ^a	E _{AR}	4.3	mJ
Maximum Power Dissipation	P _D	T _C = 25 °C	43
		T _A = 25 °C	3.7
Peak Diode Recovery dV/dt ^{c, e}	dV/dt	-4.5	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C
Soldering Recommendations (Peak temperature) ^d	For 10 s	300	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. V_{DD} = -25 V, starting T_J = 25 °C, L = 3.6 mH, R_θ = 25 Ω, I_{AS} = -6.7 A (see fig. 12)

c. I_{SP} ≤ -6.7 A, dI/dt ≤ 90 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C

d. 1.6 mm from case


e. Uses IRF9Z14, SiHF9Z14 data and test conditions



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, steady-state) ^a	R _{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	3.5	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = -250 μA	-60	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = -1 mA ^c	-	-0.06	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-2.0	-	-4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V	-	-	-100	μA
		V _{DS} = -48 V, V _{GS} = 0 V, T _J = 150 °C	-	-	-500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = -10 V, I _D = -4.0 A ^b	-	-	0.5	Ω
Forward Transconductance	g _{fs}	V _{DS} = -25 V, I _D = -4.0 A ^c	1.4	-	-	S
Dynamic						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = -25 V, f = 1.0 MHz, see fig. 5 ^c	-	270	-	pF
Output Capacitance	C _{oss}		-	170	-	
Reverse Transfer Capacitance	C _{rss}		-	31	-	
Total Gate Charge	Q _g	V _{GS} = -10 V, I _D = -6.7 A, V _{DS} = -48 V, see fig. 6 and 13 ^{b, c}	-	-	12	nC
Gate-Source Charge	Q _{gs}		-	-	3.8	
Gate-Drain Charge	Q _{gd}		-	-	5.1	
Turn-On Delay Time	t _{d(on)}	V _{DD} = -30 V, I _D = -6.7 A, R _g = 24 Ω, R _D = 4.0 Ω, see fig. 10 ^b	-	11	-	ns
Rise Time	t _r		-	63	-	
Turn-Off Delay Time	t _{d(off)}		-	10	-	
Fall Time	t _f		-	31	-	
Gate Input Resistance	R _g	f = 1 MHz, open drain	1.4	-	8.7	Ω
Internal Source Inductance	L _S	Between lead, and center of die contact	-	7.5	-	nH
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	-6.7	A
Pulsed Diode Forward Current ^a	I _{SM}		-	-	-27	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = -6.7 A, V _{GS} = 0 V ^b	-	-	-5.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = -6.7 A, dI/dt = 100 A/μs ^{b, c}	-	80	160	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	96	190	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %
- c. Uses IRF9Z14, SiHF9Z14 data and test conditions



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

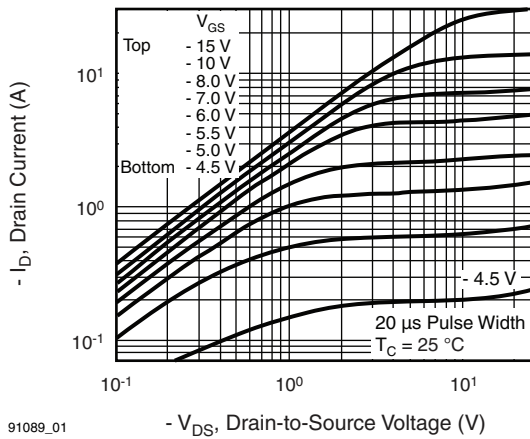


Fig. 1 - Typical Output Characteristics

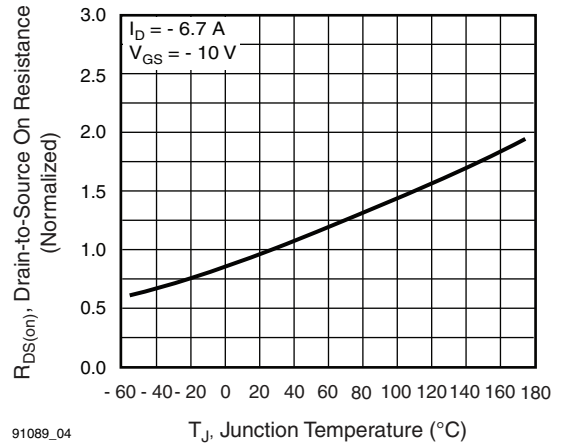


Fig. 4 - Normalized On-Resistance vs. Temperature

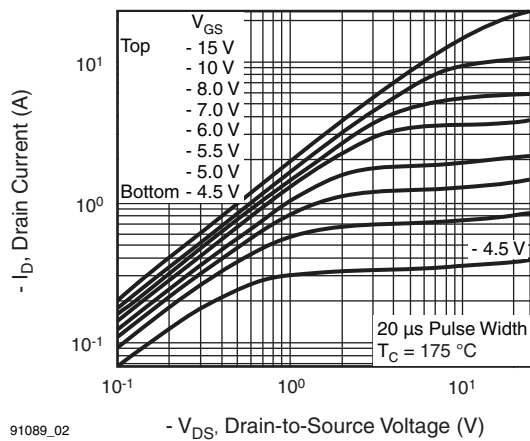


Fig. 2 - Typical Output Characteristics

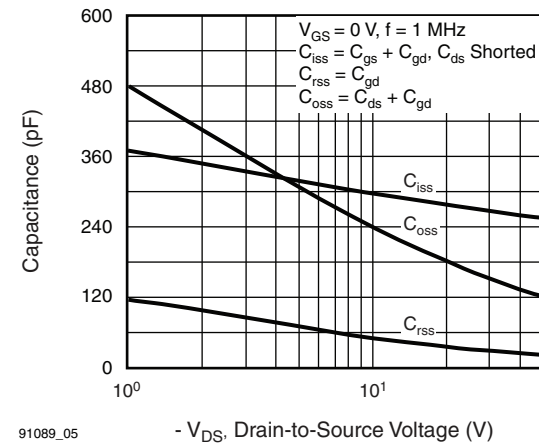


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

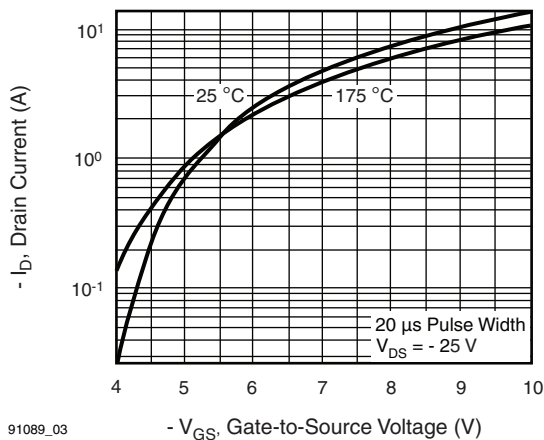


Fig. 3 - Typical Transfer Characteristics

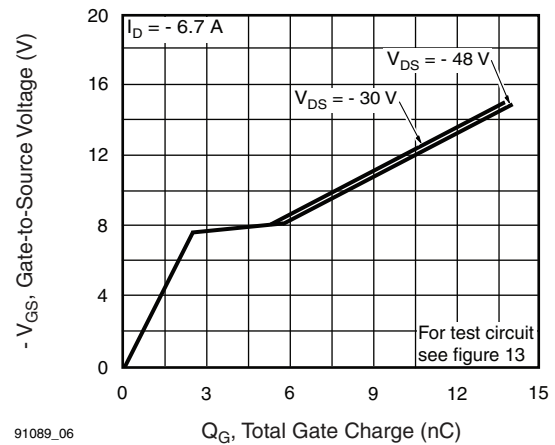
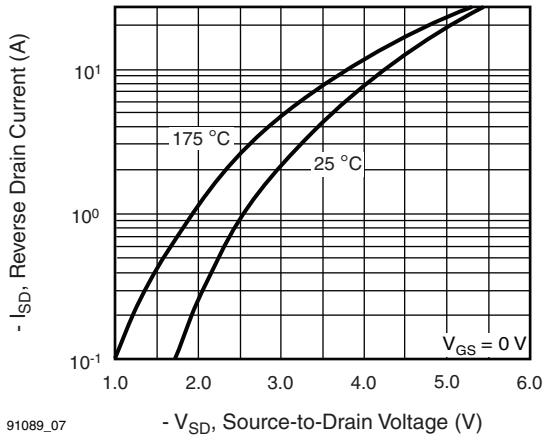
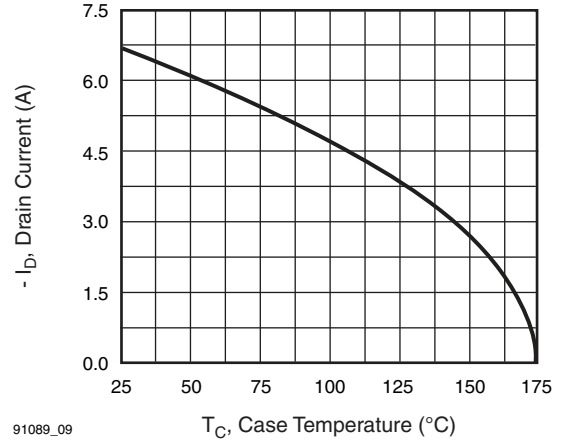


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



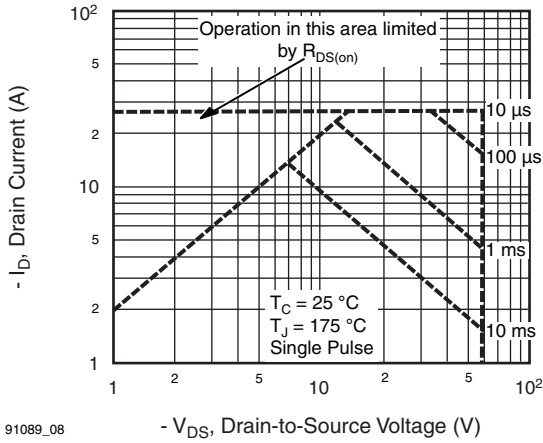
91089_07

Fig. 7 - Typical Source-Drain Diode Forward Voltage



91089_09

Fig. 9 - Maximum Drain Current vs. Case Temperature



91089_08

Fig. 8 - Maximum Safe Operating Area

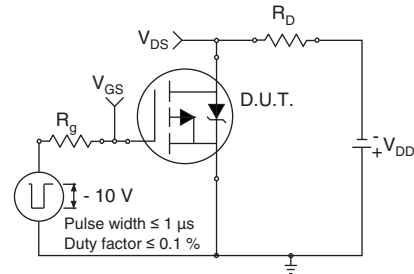


Fig. 10a - Switching Time Test Circuit

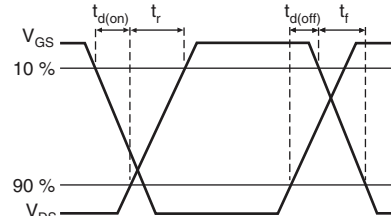
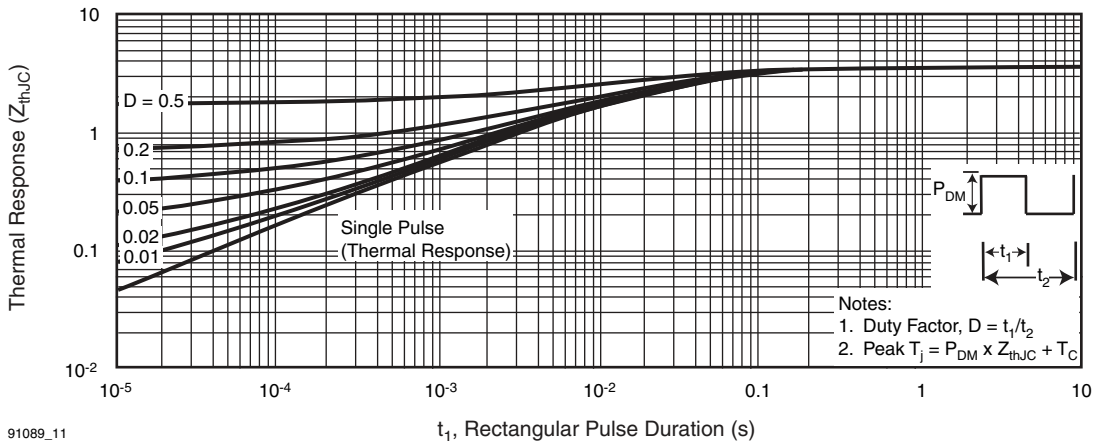


Fig. 10b - Switching Time Waveforms



91089_11

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

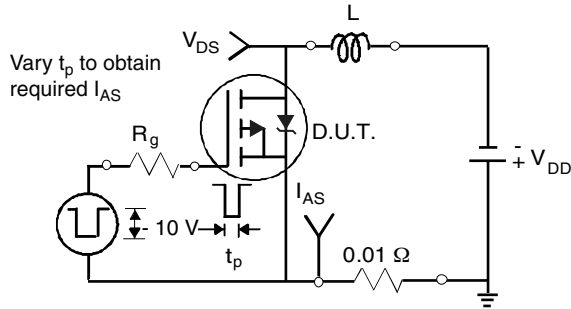


Fig. 12a - Unclamped Inductive Test Circuit

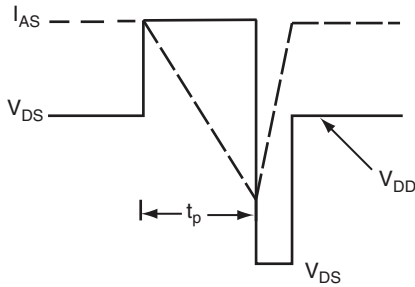


Fig. 12b - Unclamped Inductive Waveforms

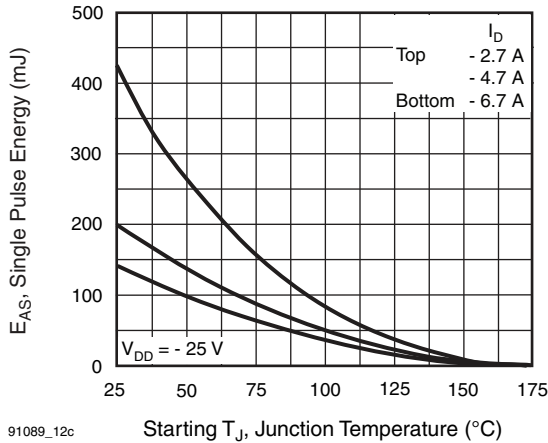


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

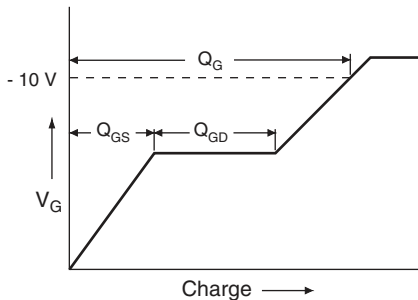


Fig. 13a - Basic Gate Charge Waveform

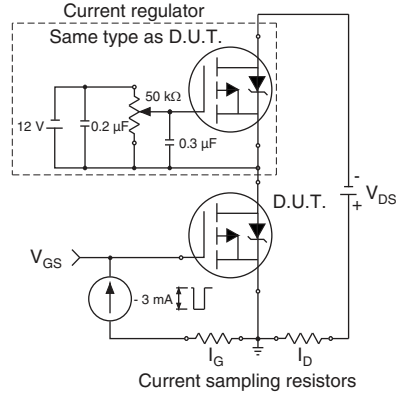
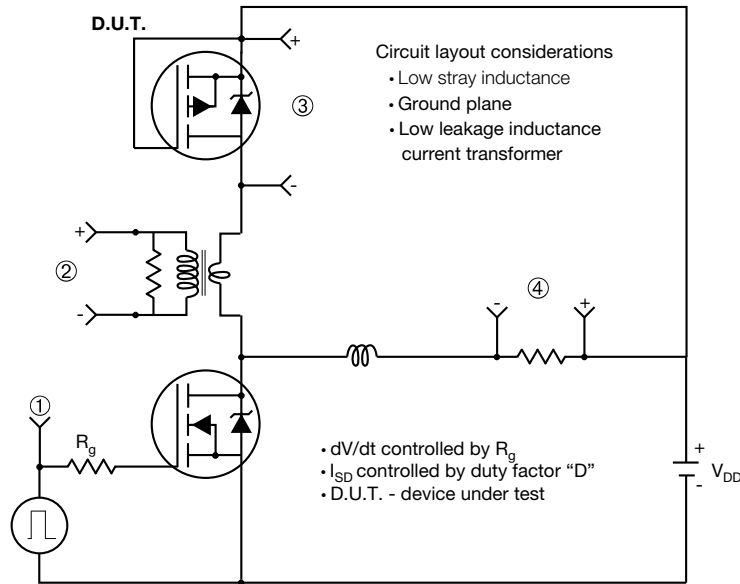
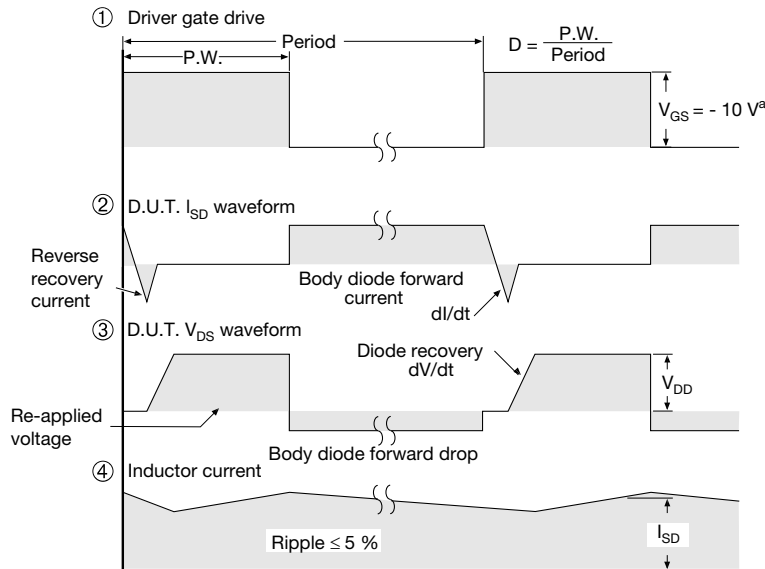


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note
• Compliment N-Channel of D.U.T. for driver



Note
a. $V_{GS} = -5\text{ V}$ for logic level and -3 V drive devices

Fig. 14 - For P-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91089.

TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

I²PAK (TO-262) (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

ECN: S-82442-Rev. A, 27-Oct-08
DWG: 5977

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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