

## Power MOSFET

**TO-220AB**


N-Channel MOSFET

### FEATURES

- Low gate charge  $Q_g$  results in simple drive Requirement
- Improved gate, avalanche, and dynamic  $dV/dt$  ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Low  $t_{rr}$  and soft diode recovery
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS\***  
Available

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

### APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching
- ZVS and high frequency circuit
- PWM inverters

PRODUCT SUMMARY	
$V_{DS}$ (V)	500
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$ 0.28
$Q_g$ max. (nC)	130
$Q_{gs}$ (nC)	33
$Q_{gd}$ (nC)	59
Configuration	Single

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRFB17N50LPbF


ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		$V_{DS}$	500	V	
Gate-source voltage		$V_{GS}$	$\pm 30$		
Continuous drain current	$V_{GS}$ at 10 V	$I_D$	$T_C = 25\text{ }^\circ\text{C}$	16	A
			$T_C = 100\text{ }^\circ\text{C}$	11	
Pulsed drain current <sup>a</sup>		$I_{DM}$	64		
Linear derating factor			1.8	W/ $^\circ\text{C}$	
Single pulse avalanche energy <sup>b</sup>		$E_{AS}$	390	mJ	
Repetitive avalanche current <sup>a</sup>		$I_{AR}$	16	A	
Repetitive avalanche energy <sup>a</sup>		$E_{AR}$	22	mJ	
Maximum power dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	220	W	
Peak diode recovery $dV/dt$ <sup>c</sup>		$dV/dt$	13	V/ns	
Operating junction and storage temperature range		$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$	
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s		300		
Mounting torque	6-32 or M3 screw		10	lbf · in	
			1.1	N · m	

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3.0\text{ mH}$ ,  $R_g = 25\text{ }^\circ\Omega$ ,  $I_{AS} = 16\text{ A}$  (see fig. 12)
- $I_{SD} \leq 16\text{ A}$ ,  $dI/dt \leq 347\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	62	°C/W
Case-to-sink, flat, greased surface	$R_{thCS}$	0.50	-	
Maximum junction-to-case (drain)	$R_{thJC}$	-	0.56	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		500	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.6	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$		-	-	50	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	2.0	mA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 9.9\text{ A}^b$	-	0.28	0.32	$\Omega$
Forward transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 9.9\text{ A}^b$		11	-	-	S
<b>Dynamic</b>							
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5		-	2760	-	pF
Output capacitance	$C_{oss}$			-	325	-	
Reverse transfer capacitance	$C_{rss}$			-	37	-	
Output capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	3690	-	pF
		$V_{GS} = 0\text{ V}$	$V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$	-	84	-	
Effective output capacitance	$C_{oss\text{ eff.}}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 0\text{ V to } 400\text{ V}^c$	-	159	-	
Total gate charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 16\text{ A}, V_{DS} = 400\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	130	nC
Gate-source charge	$Q_{gs}$			-	-	33	
Gate-drain charge	$Q_{gd}$			-	-	59	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 16\text{ A}, R_g = 7.5\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	21	-	ns
Rise time	$t_r$			-	51	-	
Turn-off delay time	$t_{d(off)}$			-	50	-	
Fall time	$t_f$			-	28	-	
Gate input resistance	$R_g$	$f = 1\text{ MHz}$ , open drain		0.3	-	1.4	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	16	A
Pulsed diode forward current <sup>a</sup>	$I_{SM}$			-	-	64	
Body diode voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 16\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.5	V
Body diode reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$	$I_F = 16\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	170	250	ns
		$T_J = 125\text{ }^\circ\text{C}$		-	220	330	
Body diode reverse recovery charge	$Q_{rr}$	$T_J = 25\text{ }^\circ\text{C}$		-	470	710	nC
		$T_J = 125\text{ }^\circ\text{C}$		-	810	1210	
Reverse recovery current	$I_{RRM}$			-	7.3	11	A
Forward turn-on time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

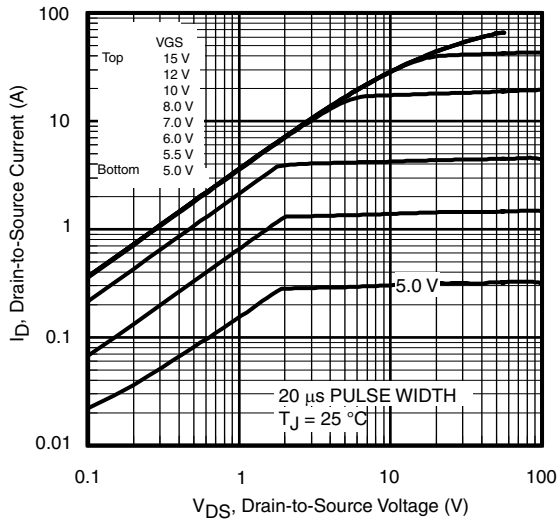


Fig. 1 - Typical Output Characteristics

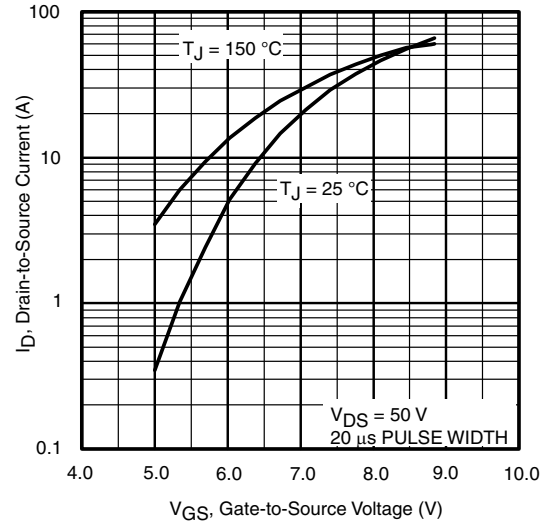


Fig. 3 - Typical Transfer Characteristics

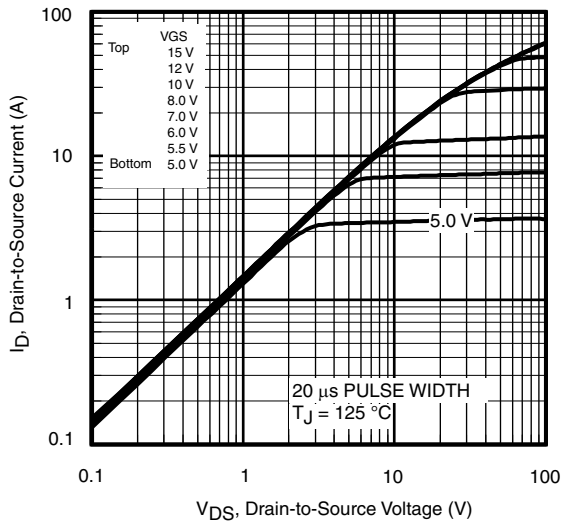


Fig. 2 - Typical Output Characteristics

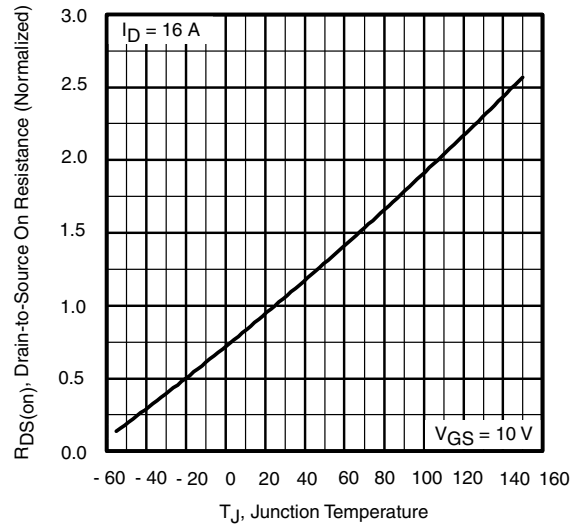


Fig. 4 - Normalized On-Resistance vs. Temperature

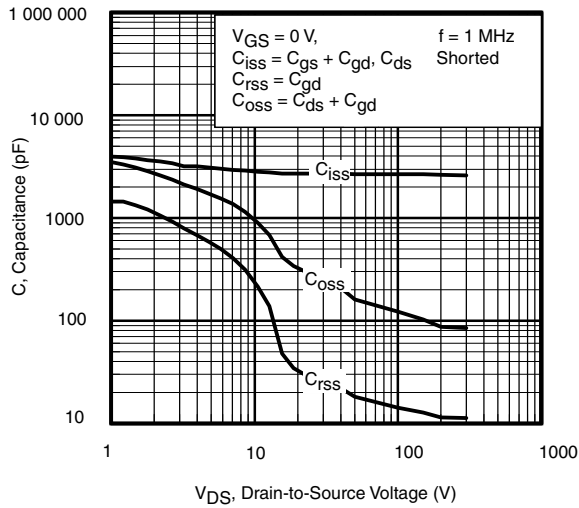


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

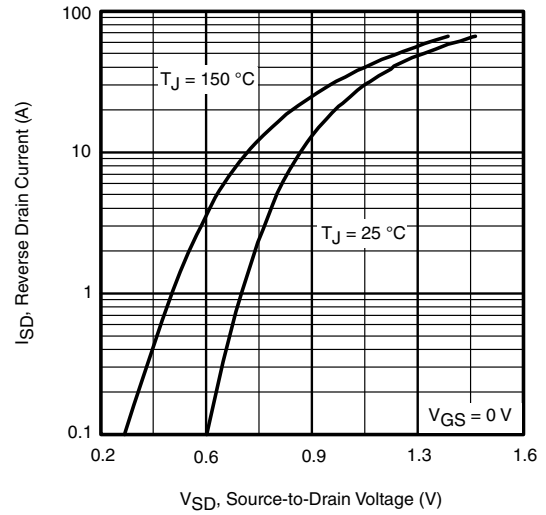


Fig. 7 - Typical Source-Drain Diode Forward Voltage

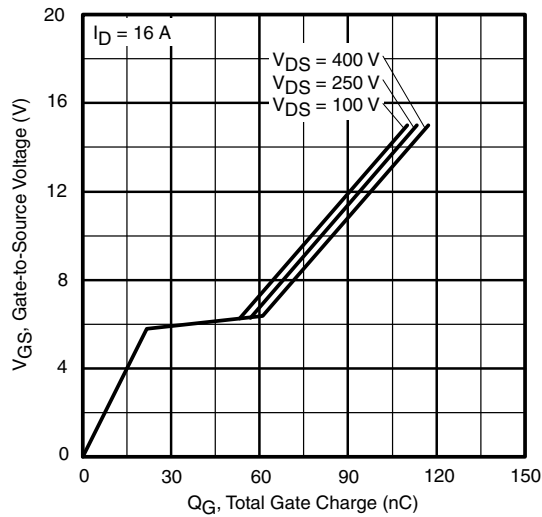


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

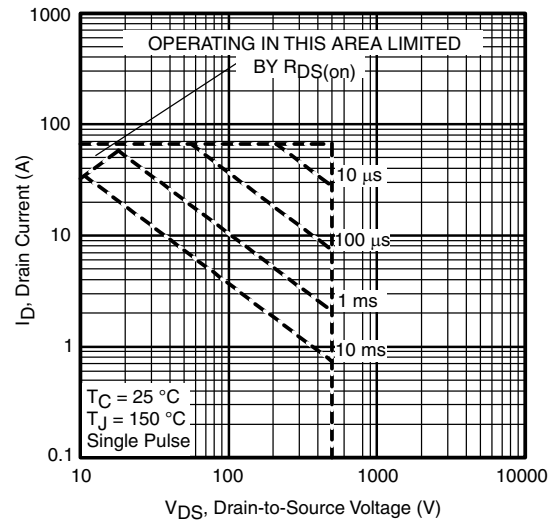


Fig. 8 - Maximum Safe Operating Area

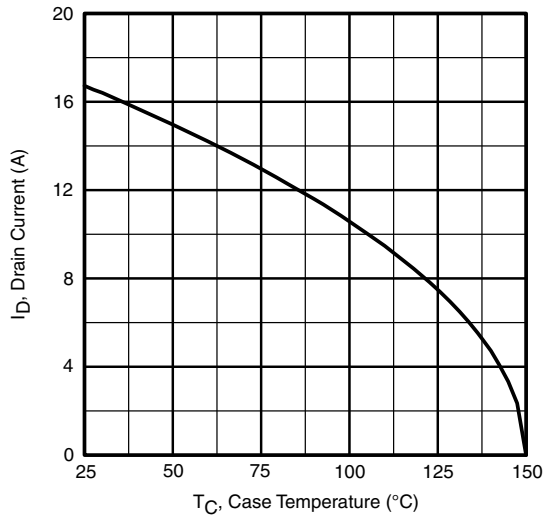


Fig. 9 - Maximum Drain Current vs. Case Temperature

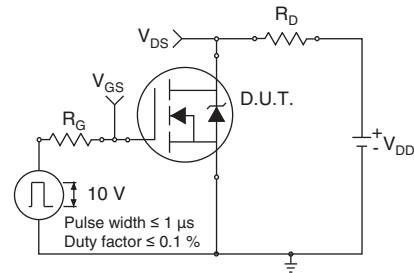


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

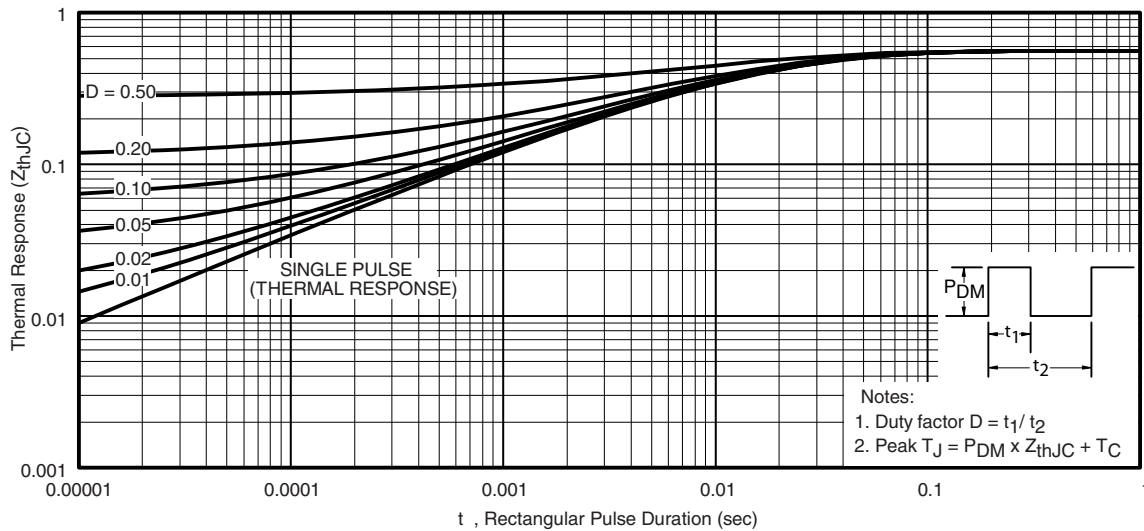


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

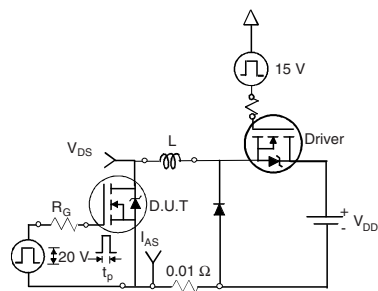


Fig. 12a - Unclamped Inductive Test Circuit

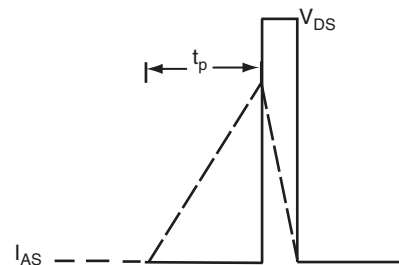
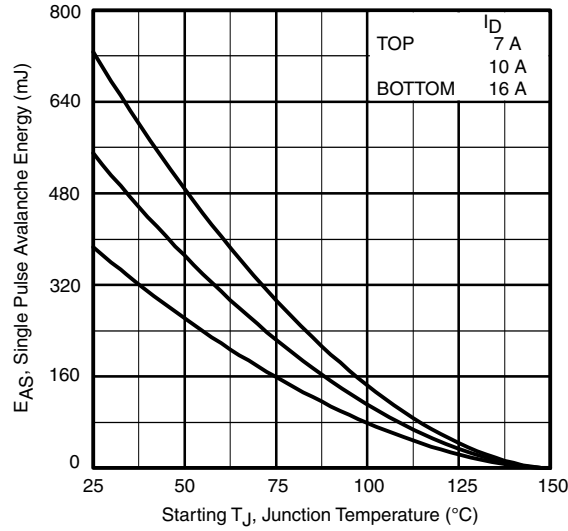
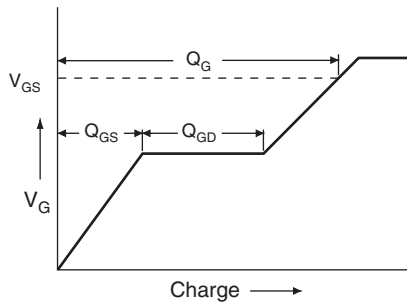


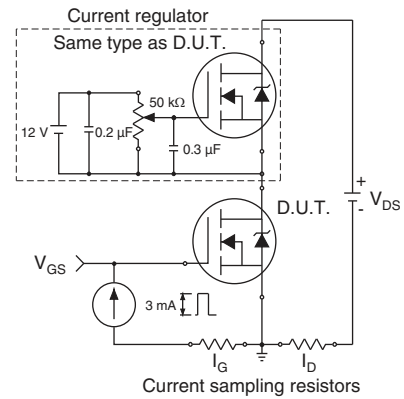
Fig. 12b - Unclamped Inductive Waveforms



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

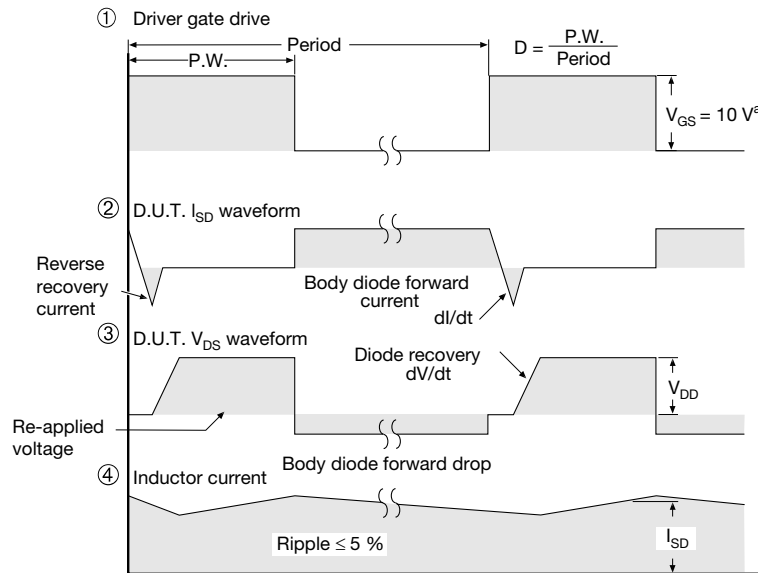
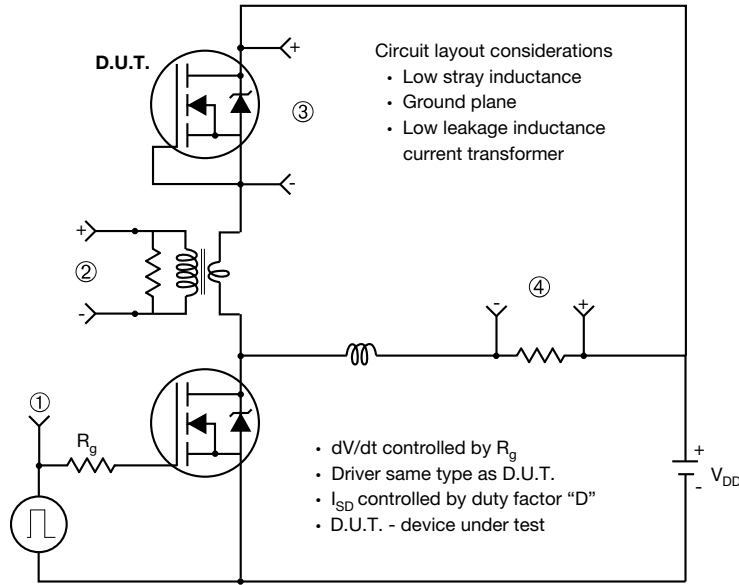


**Fig. 13a - Basic Gate Charge Waveform**



**Fig. 13b - Gate Charge Test Circuit**

Peak Diode Recovery dV/dt Test Circuit



**Note**  
a.  $V_{GS} = 5\text{ V}$  for logic level devices

Fig. 14 - For N-Channel

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