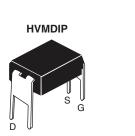
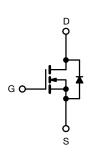
COMPLIANT



Power MOSFET





N-Channel MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	20	200				
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V	1.5				
Q _g (Max.) (nC)	8.2	8.2				
Q _{gs} (nC)	1.8	1.8				
Q _{gd} (nC)	4.9	4.5				
Configuration	Sing	Single				

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- · For automatic insertion
- End stackable
- Fast switching
- · Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

ORDERING INFORMATION	
Package	HVMDIP
Lead (Pb)-free	IRFD210PbF

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V_{DS}	200	V	
Gate-source voltage			V_{GS}	± 20		
Continuous drain current	V _{GS} at 10 V	$T_A = 25 ^{\circ}\text{C}$ $T_A = 100 ^{\circ}\text{C}$	1_	0.60	A	
		T _A = 100 °C	I _D	0.38		
Pulsed drain current ^a			I _{DM}	4.8		
Linear derating factor				0.0083	W/°C	
Single pulse avalanche energy ^b			E _{AS}	79	mJ	
Repetitive avalanche current ^a			I _{AR}	0.60	А	
Repetitive avalanche energy a			E _{AR}	0.10	mJ	
aximum power dissipation T _A = 25 °C		P _D	1.0	W		
Peak diode recovery dV/dt ^c			dV/dt	5.0	V/ns	
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150		
Soldering recommendations (peak temperature)	For 10 s			300 ^d	°C	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. $V_{DD} = 50 \text{ V}$, starting $T_J = 25 \,^{\circ}\text{C}$, L = 82 mH, $R_g = 25 \,\Omega$, $I_{AS} = 1.2 \,\text{A}$ (see fig. 12)
- c. $I_{SD} \le 3.3$ A, $dI/dt \le 70$ A/ μ s, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C
- d. 1.6 mm from case



Vishay Siliconix

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYP.	MAX.	UNIT		
Maximum Junction-to-Ambient	R _{thJA}	-	120	°C/W		

SPECIFICATIONS (T _J = 25 °C, u		1		I	l ——		
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		1		T	T	T	
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		200	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referen	ce to 25 °C, I _D = 1 mA	-	0.30	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS}	$= V_{GS}, I_D = 250 \mu A$	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	less	$V_{DS} = 200 \text{ V}, V_{GS} = 0 \text{ V}$		-	-	25	μA
Zero date voltage Brain Gunent	I _{DSS}	V _{DS} = 160 '	$V, V_{GS} = 0 V, T_{J} = 125 ^{\circ}C$	-	-	250	μΑ
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	$I_D = 0.36 A^b$	-	-	1.5	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 0.36 A ^b		0.10	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V		-	140	-	pF
Output Capacitance	C _{oss}]	V _{DS} = 25 V		53	-	
Reverse Transfer Capacitance	C _{rss}	f = 1.0 MHz, see fig. 5		-	15	-	
Total Gate Charge	Qg			-	-	8.2	
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V	$I_D = 3.3 \text{ A}, V_{DS} = 160 \text{ V}$ see fig. 6 and 13^b	-	-	1.8	nC
Gate-Drain Charge	Q _{gd}			-	-	4.5	
Turn-On Delay Time	t _{d(on)}	V_{DD} = 100 V, I_{D} = 3.3 A R_{g} = 24 Ω , R_{D} = 30 Ω , see fig. 10 ^b		-	8.2	-	- ns
Rise Time	t _r			-	17	-	
Turn-Off Delay Time	t _{d(off)}			-	14	-	
Fall Time	t _f			-	8.9	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from		-	4.0	-	-11
Internal Source Inductance	L _S	package and die contact	-	6.0	-	- nH	
Drain-Source Body Diode Characteristic	cs					•	
Continuous Source-Drain Diode Current	Is	MOSFET symbol showing the integral reverse p - n junction diode		-	-	0.60	^
Pulsed Diode Forward Current ^a	I _{SM}			-	-	4.8	A
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 0.60 A, V _{GS} = 0 V ^b		-	-	2.0	V
Body Diode Reverse Recovery Time	t _{rr}	T 05.00 :	0.0 4 .11/.11 . 400.47 . 5	-	150	310	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = 3.3 \text{A}, dI/dt = 100 \text{A/} \mu \text{s}^{\text{b}}$		-	0.60	1.4	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated l				v L _s and	<u>Ln)</u>

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width \leq 300 μ s; duty cycle \leq 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

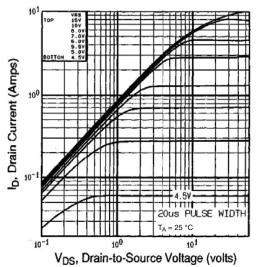


Fig. 1 - Typical Output Characteristics, T_A = 25 °C

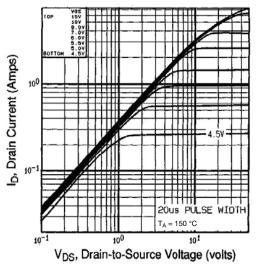


Fig. 2 - Typical Output Characteristics, T_A = 150 °C

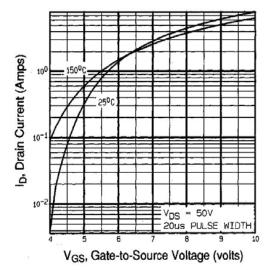


Fig. 3 - Typical Transfer Characteristics

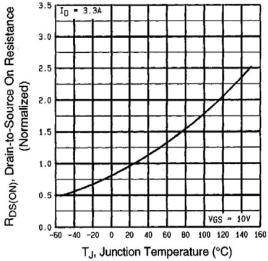


Fig. 4 - Normalized On-Resistance vs. Temperature



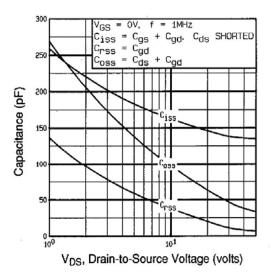


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

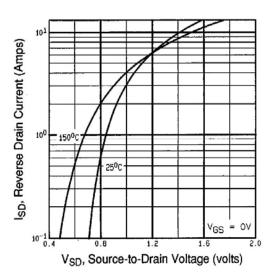


Fig. 7 - Typical Source-Drain Diode Forward Voltage

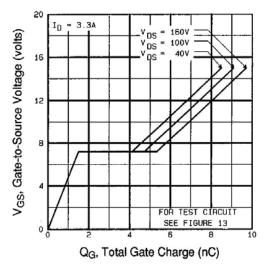


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

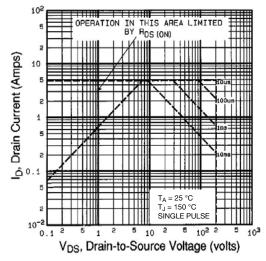


Fig. 8 - Maximum Safe Operating Area



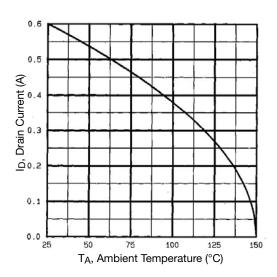


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

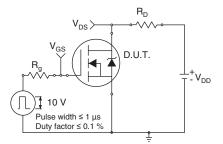


Fig. 10a - Switching Time Test Circuit

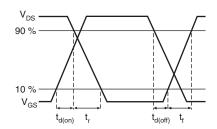


Fig. 10b - Switching Time Waveforms

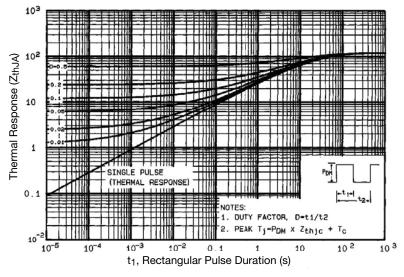


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



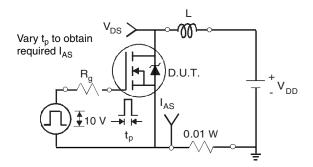


Fig. 12a - Unclamped Inductive Test Circuit

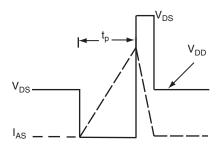


Fig. 12b - Unclamped Inductive Waveforms

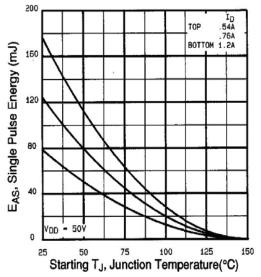


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

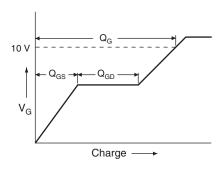


Fig. 13a - Basic Gate Charge Waveform

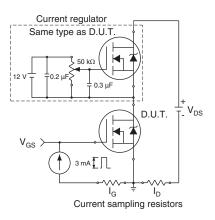
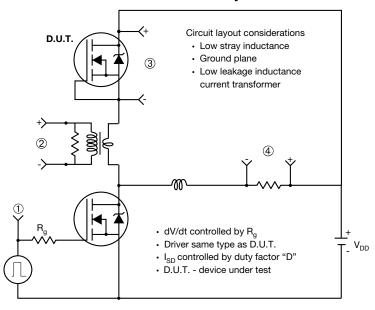


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



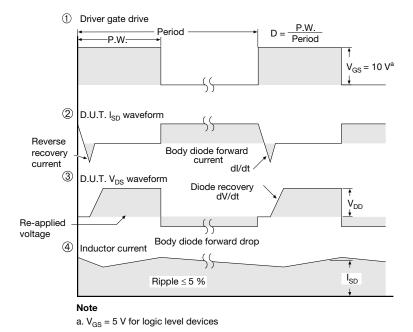
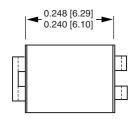


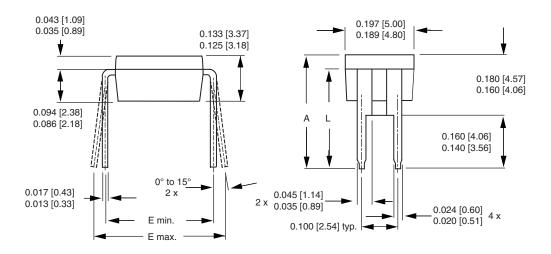
Fig. 14 - For N-Channel

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HVM DIP (High voltage)





	INCHES		MILLIMETERS	
DIM.	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
Е	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36

ECN: X10-0386-Rev. B, 06-Sep-10

DWG: 5974

Note

1. Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.

Document Number: 91361 Revision: 06-Sep-10



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