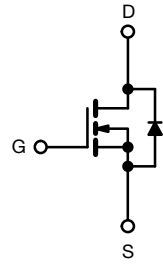


## Power MOSFET



N-Channel MOSFET

### FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- For automatic insertion
- End stackable
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT

### PRODUCT SUMMARY

$V_{DS}$ (V)	400	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	3.6
$Q_g$ (Max.) (nC)	17	
$Q_{gs}$ (nC)	3.4	
$Q_{gd}$ (nC)	8.5	
Configuration	Single	

### DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertible case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

### ORDERING INFORMATION

Package	HVMDIP
Lead (Pb)-free	IRFD310PbF

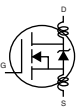

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	400	V
Gate-source voltage	$V_{GS}$	$\pm 20$	
Continuous drain current	$I_D$	$T_A = 25$ °C	0.35
		$T_A = 100$ °C	0.22
Pulsed drain current <sup>a</sup>	$I_{DM}$	2.8	A
Linear derating factor		0.0083	W/°C
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	46	mJ
Repetitive avalanche current <sup>a</sup>	$I_{AR}$	0.35	A
Repetitive avalanche energy <sup>a</sup>	$E_{AR}$	0.10	mJ
Maximum power dissipation	$P_D$	1.0	W
Peak diode recovery dV/dt <sup>c</sup>	$dV/dt$	4.0	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature)	For 10 s	300 <sup>d</sup>	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 41$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 1.4$  A (see fig. 12)
- $I_{SD} \leq 2.0$  A,  $dI/dt \leq 40$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C
- 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	120	°C/W

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		400	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.47	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 320\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 0.21\text{ A}^b$	-	-	3.6	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 1.2\text{ A}$		1.0	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5		-	170	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$			-	34	-	
Reverse Transfer Capacitance	$C_{rss}$			-	6.3	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 2.0\text{ A}, V_{DS} = 320\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	17	nC
Gate-Source Charge	$Q_{gs}$			-	-	3.4	
Gate-Drain Charge	$Q_{gd}$			-	-	8.5	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 200\text{ V}, I_D = 2.0\text{ A}, R_g = 24\text{ }\Omega, R_D = 95\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	8.0	-	ns
Rise Time	$t_r$			-	9.9	-	
Turn-Off Delay Time	$t_{d(off)}$			-	21	-	
Fall Time	$t_f$			-	11	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	$L_S$			-	6.0	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	0.35	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	2.8	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 0.35\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.6	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 2.0\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	240	540	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.85	1.6	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)  
 b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

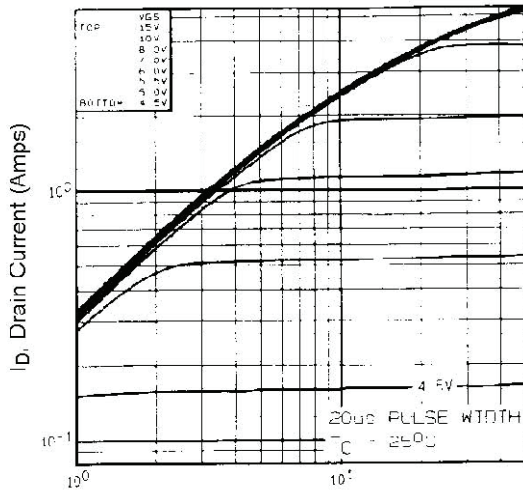


Fig. 1 - Typical Output Characteristics,  $T_A = 25\text{ }^\circ\text{C}$

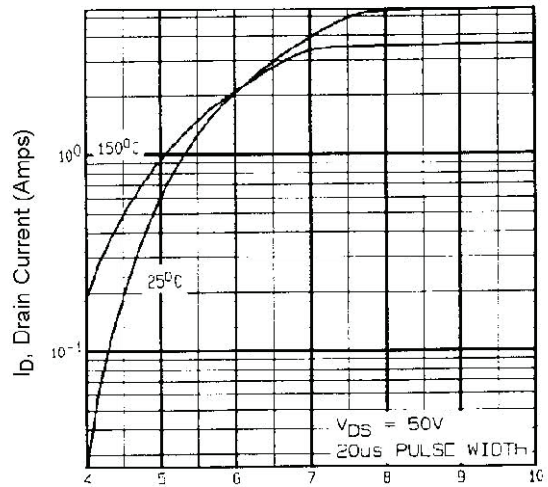


Fig. 2 - Typical Transfer Characteristics

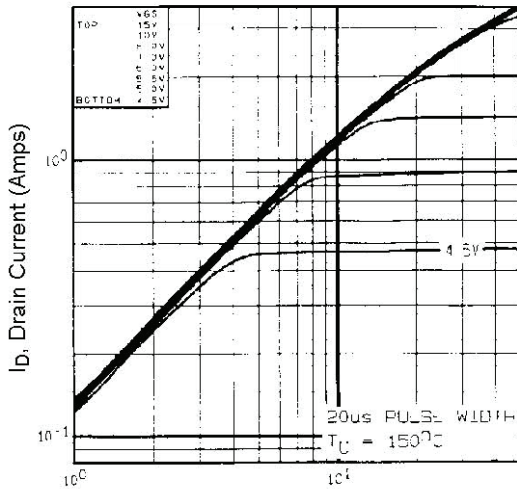


Fig. 1 - Typical Output Characteristics,  $T_A = 150\text{ }^\circ\text{C}$

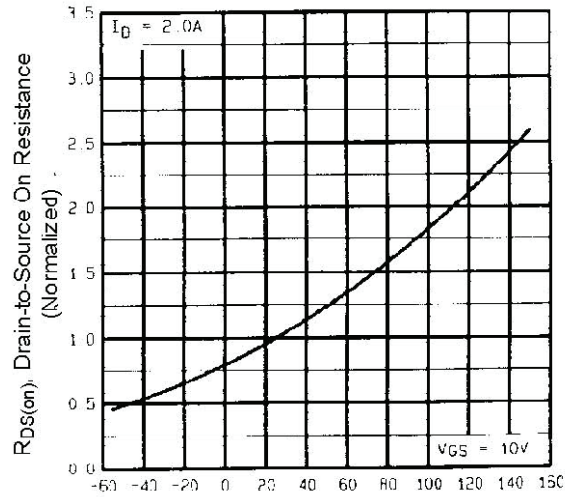


Fig. 3 - Normalized On-Resistance vs. Temperature

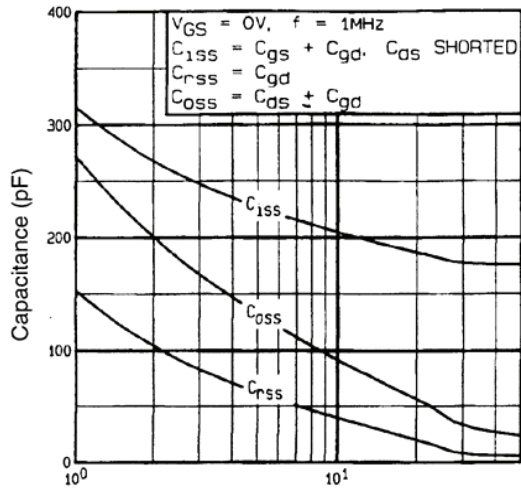


Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

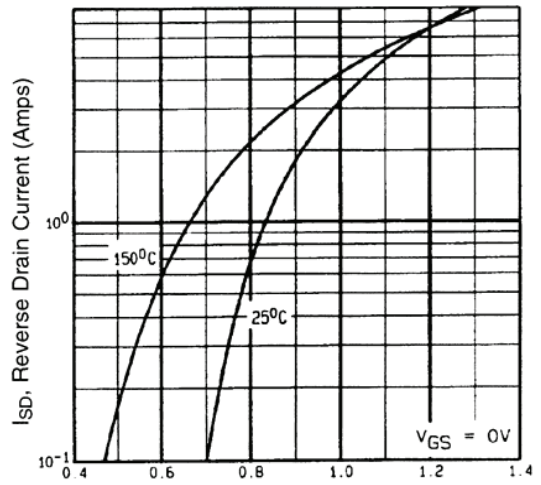


Fig. 6 - Typical Source-Drain Diode Forward Voltage

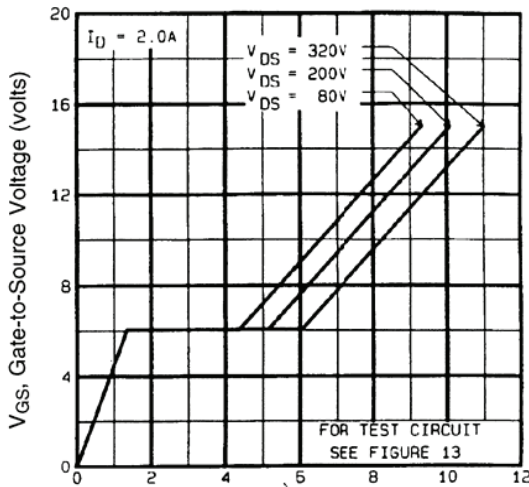


Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage

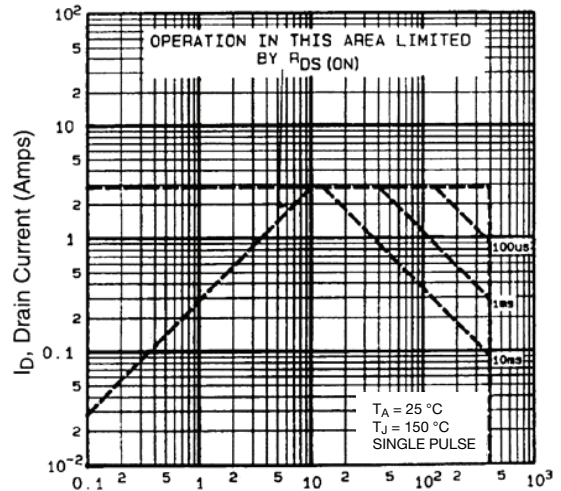


Fig. 7 - Maximum Safe Operating Area

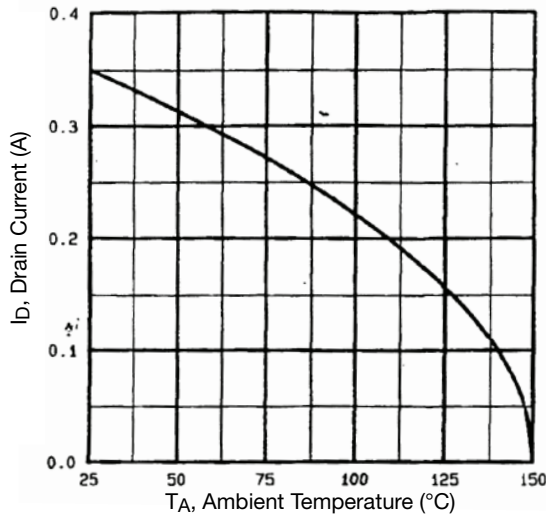


Fig. 8 - Maximum Drain Current vs. Ambient Temperature

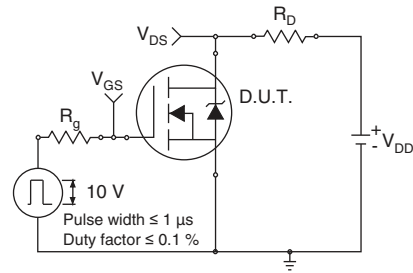


Fig. 10a - Switching Time Test Circuit

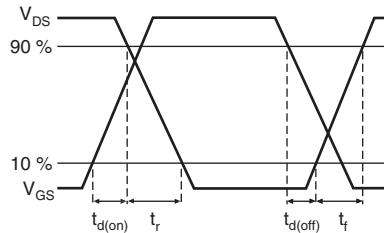


Fig. 10b - Switching Time Waveforms

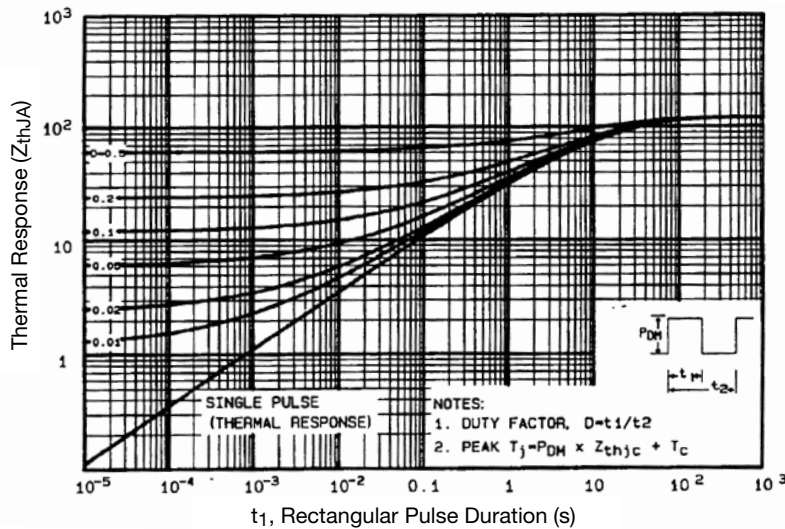


Fig. 9 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

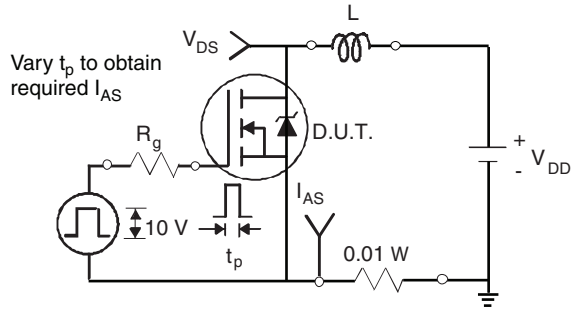


Fig. 12a - Unclamped Inductive Test Circuit

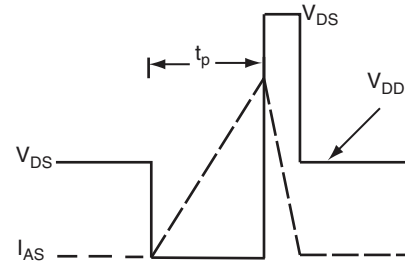


Fig. 12b - Unclamped Inductive Waveforms

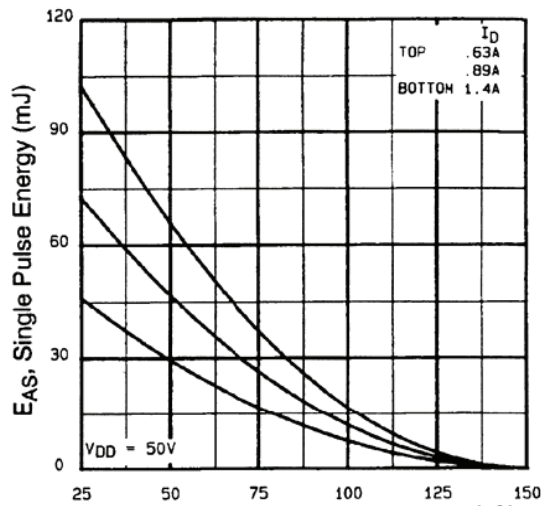


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

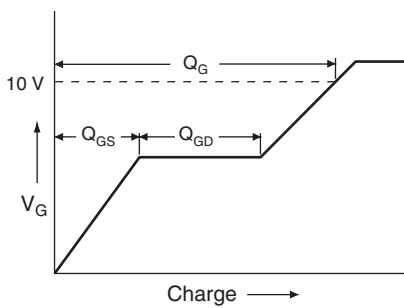


Fig. 13a - Basic Gate Charge Waveform

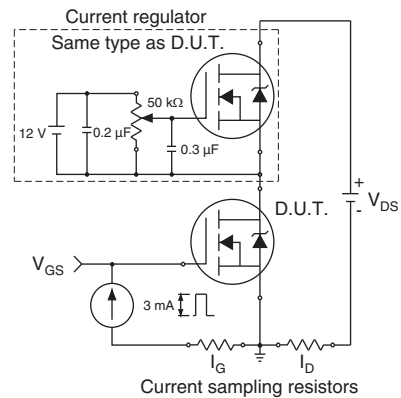
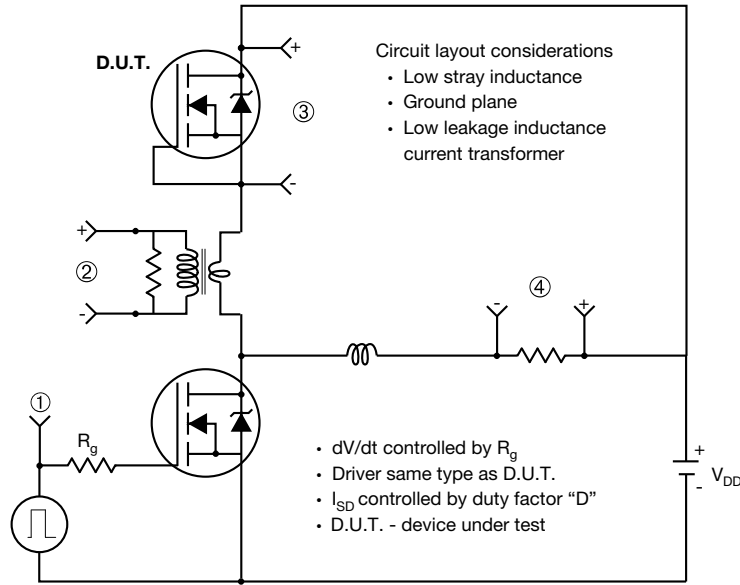


Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**



**Note**  
a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 10 - For N-Channel**

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## HVM DIP (High voltage)



DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36

ECN: X10-0386-Rev. B, 06-Sep-10  
DWG: 5974

### Note

- Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.





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