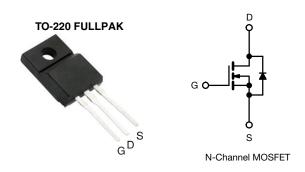
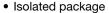
Vishay Siliconix

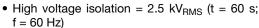
## **Power MOSFET**



PRODUCT SUMMARY				
V <sub>DS</sub> (V)	100			
$R_{DS(on)}(\Omega)$	V <sub>GS</sub> = 10 V 0.077			
Q <sub>g</sub> max. (nC)	72			
Q <sub>gs</sub> (nC)	11			
Q <sub>gd</sub> (nC)	32			
Configuration	Single			

### **FEATURES**







COMPLIANT

• Sink to lead creepage distance = 4.8 mm

- 175 °C operating temperature
- Dynamic dV/dt rating
- by name av, at raining
- · Low thermal resistance
- Material categorization: for definitions of compliance please see <a href="https://www.vishav.com/doc?99912"><u>www.vishav.com/doc?99912</u></a>

### **DESCRIPTION**

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	IRFI540GPbF

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			$V_{DS}$	100	V	
Gate-source voltage			$V_{GS}$	± 20	V	
Continuous dusin surrent			I <sub>D</sub>	17		
Continuous drain current $V_{GS} \text{ at 10 V} \frac{T_C = 25 ^{\circ}\text{C}}{T_C = 100 ^{\circ}\text{C}}$				12	Α	
Pulsed drain current <sup>a</sup>			I <sub>DM</sub>	68		
Linear derating factor				0.32	W/°C	
Single pulse avalanche energy b			E <sub>AS</sub>	720	mJ	
Repetitive avalanche current a			I <sub>AR</sub>	17	Α	
Repetitive avalanche energy <sup>a</sup>			E <sub>AR</sub>	4.8	mJ	
Maximum power dissipation $T_C = 25  ^{\circ}C$			$P_{D}$	48	W	
Peak diode recovery dV/dt <sup>c</sup>			dV/dt	5.5	V/ns	
Operating junction and storage temperature range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	00	
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s			300	°C	
Mounting torque	M3 screw			0.6	Nm	

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b.  $V_{DD}$  = 25 V, starting  $T_J$  = 25 °C, L = 3.7 mH,  $R_g$  = 25  $\Omega$ ,  $I_{AS}$  = 17 A (see fig. 12)
- c.  $I_{SD} \leq$  17 A,  $dI/dt \leq$  200 A/µs,  $V_{DD} \leq V_{DS}$ ,  $T_{J} \leq$  175 °C
- d. 1.6 mm from case



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THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R <sub>thJA</sub>	=	65	°C/W
Maximum junction-to-case (drain)	R <sub>thJC</sub>	-	3.1	G/ VV

PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						•	
Drain-ssource breakdown voltage	$V_{DS}$	V <sub>GS</sub> =	= 0 V, I <sub>D</sub> = 250 μA	100	-	-	V
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I <sub>D</sub> = 1 mA	-	0.13	-	V/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	· V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	-	4.0	V
Gate-source leakage	I <sub>GSS</sub>	,	V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zoro goto voltago droin ourrent	1	V <sub>DS</sub> =	: 100 V, V <sub>GS</sub> = 0 V	-	-	25	
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{DS} = 80 \text{ V}$	V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C	-	-	250	μA
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A <sup>b</sup>	-	-	0.077	Ω
Forward transconductance	9 <sub>fs</sub>	V <sub>DS</sub> =	= 50 V, I <sub>D</sub> = 10 A <sup>b</sup>	9.1	-	-	S
Dynamic							
Input capacitance	C <sub>iss</sub>		$V_{GS} = 0 V$ ,	-	1700	-	
Output capacitance	C <sub>oss</sub>	$V_{DS} = 25 \text{ V},$		-	560	-	pF
Reverse transfer capacitance	C <sub>rss</sub>	f = 1.	f = 1.0 MHz, see fig. 5		120	-	
Drain to sink capacitance	С		f = 1.0 MHz	-	12	-	
Total gate charge	Qg			=.	-	72	
Gate-source charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$I_D = 17 \text{ A}, V_{DS} = 80 \text{ V},$ see fig. 6 and 13 b	_	-	11	nC
Gate-drain charge	Q <sub>gd</sub>		See fig. 6 and 16	-	-	32	
Turn-on delay time	t <sub>d(on)</sub>			-	11	-	
Rise time	t <sub>r</sub>		= 50 V, I <sub>D</sub> = 17 A,	-	44	-	
Turn-off delay time	t <sub>d(off)</sub>		9.1 $\Omega$ , R <sub>D</sub> = 2.9 $\Omega$ , see fig. 10 <sup>b</sup>	-	53	-	ns
Fall time	t <sub>f</sub>			-	43	-	
Gate input resistance	R <sub>g</sub>	f = 1 MHz, open drain		0.3	-	1.6	Ω
Internal drain inductance	L <sub>D</sub>	Between lead 6 mm (0.25") f	١	-	4.5	-	
Internal source inductance	L <sub>S</sub>	package and center of die contact		-	7.5	-	- nH
<b>Drain-Source Body Diode Characteristic</b>	cs					•	,
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the		-	-	17	Α
Pulsed diode forward current <sup>a</sup>	I <sub>SM</sub>	integral revers p - n junction		-	-	68	
Body diode voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C	, I <sub>S</sub> = 17 A, V <sub>GS</sub> = 0 V <sup>b</sup>	-		2.5	V
Body diode reverse recovery time	t <sub>rr</sub>	T 25 °C 1	- 17 A dl/dt - 100 A/vab	-	180	360	ns
Body diode reverse recovery charge	Q <sub>rr</sub>	T₁ = 25 °C. I₅ = 17 A. dl/dt = 100 A/us b		2.6	μC		
Forward turn-on time	t <sub>on</sub>	Intrinsic tu	rn-on time is negligible (turn	-on is dor	ninated b	y L <sub>S</sub> and	L <sub>D</sub> )

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width  $\leq 300~\mu s;$  duty cycle  $\leq 2~\%$



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

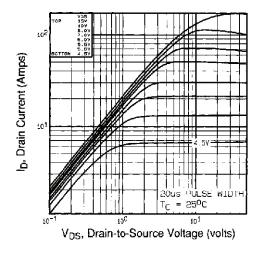


Fig. 1 - Typical Output Characteristics, T<sub>C</sub> = 25 °C

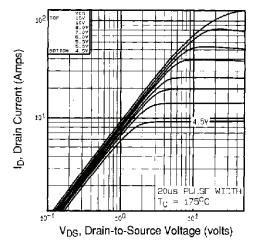


Fig. 2 - Typical Output Characteristics,  $T_C$  = 175 °C

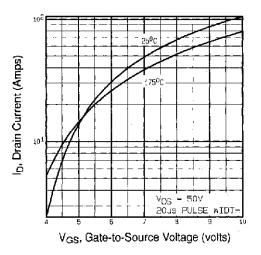


Fig. 3 - Typical Transfer Characteristics

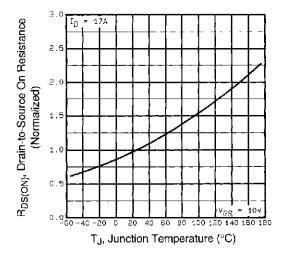


Fig. 4 - Normalized On-Resistance vs. Temperature



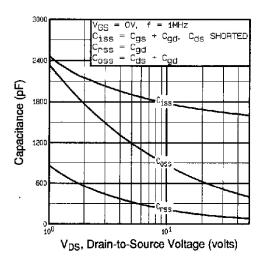


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

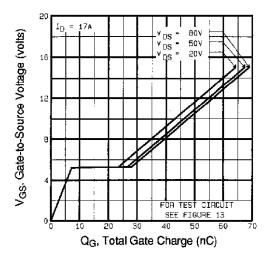


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

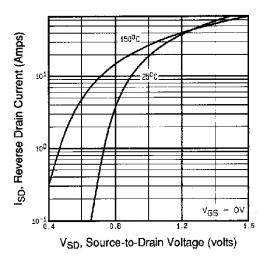


Fig. 7 - Typical Source-Drain Diode Forward Voltage

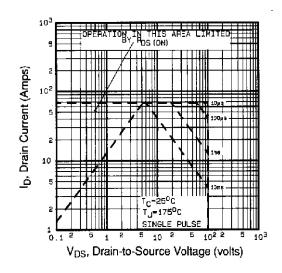


Fig. 8 - Maximum Safe Operating Area



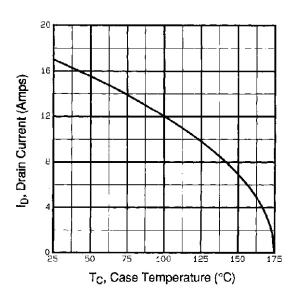


Fig. 9 - Maximum Drain Current vs. Case Temperature

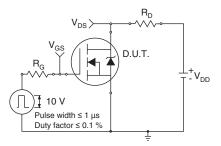


Fig. 10a - Switching Time Test Circuit

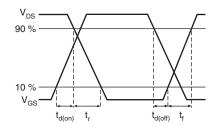


Fig. 10b - Switching Time Waveforms

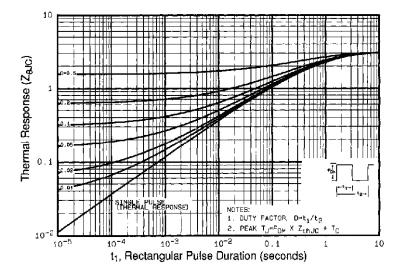


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

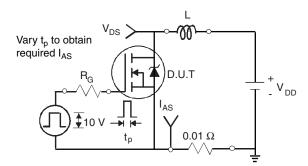


Fig. 12a - Unclamped Inductive Test Circuit

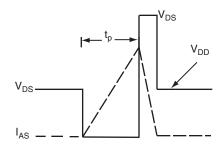


Fig. 12b - Unclamped Inductive Waveforms



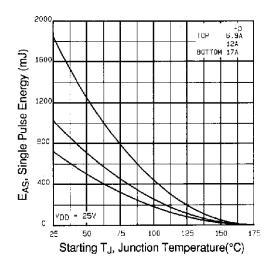


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

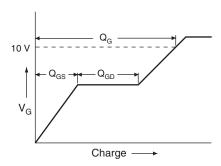


Fig. 13a - Basic Gate Charge Waveform

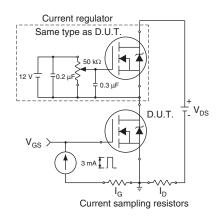
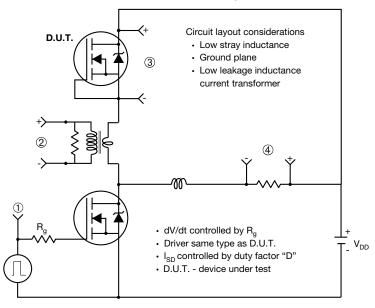


Fig. 13b - Gate Charge Test Circuit



### Peak Diode Recovery dV/dt Test Circuit



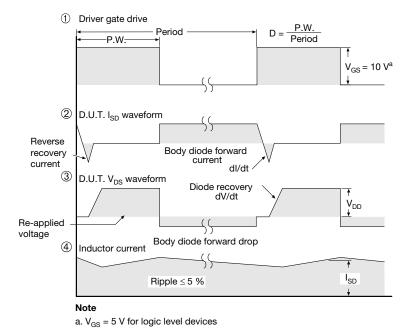


Fig. 14 - For N-Channel

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# **TO-220 FULLPAK (High Voltage)**

### **OPTION 1: FACILITY CODE = 9**



		MILLIMETERS	
DIM.	MIN.	NOM.	MAX.
Α	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
С	0.45	0.50	0.63
D	15.80	15.87	15.97
е		2.54 BSC	
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
ØR	3.08	3.18	3.28

- 1. To be used only for process drawing
- 2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
- 3. All critical dimensions should C meet  $C_{pk} > 1.33$
- 4. All dimensions include burrs and plating thickness
- 5. No chipping or package damage
- 6. Facility code will be the 1st character located at the 2nd row of the unit marking



### **OPTION 2: FACILITY CODE = Y**



	MILLIM	ERS INCHES			
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	4.570	4.830	0.180	0.190	
A1	2.570	2.830	0.101	0.111	
A2	2.510	2.850	0.099	0.112	
b	0.622	0.890	0.024	0.035	
b2	1.229	1.400	0.048	0.055	
b3	1.229	1.400	0.048	0.055	
С	0.440	0.629	0.017	0.025	
D	8.650	9.800	0.341	0.386	
d1	15.88	16.120	0.622	0.635	
d3	12.300	12.920	0.484	0.509	
Е	10.360	10.630	0.408	0.419	
е	2.54	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541	
L1	3.100	3.500	0.122	0.138	
n	6.050	6.150	0.238	0.242	
ØΡ	3.050	3.450	0.120	0.136	
u	2.400	2.500	0.094	0.098	
V	0.400	0.500	0.016	0.020	

ECN: E19-0180-Rev. D, 08-Apr-2019

DWG: 5972

- 1. To be used only for process drawing
- 2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
- 3. All critical dimensions should C meet  $C_{pk} > 1.33$
- 4. All dimensions include burrs and plating thickness
- 5. No chipping or package damage
- 6. Facility code will be the 1st character located at the 2nd row of the unit marking



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Vishay

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