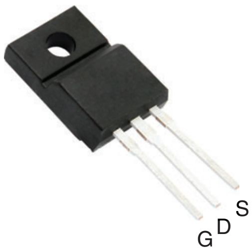
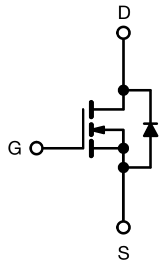
Power MOSFET

TO-220 FULLPAK





N-Channel MOSFET

FEATURES

- Ultra low gate charge
- Reduced gate drive requirement
- Enhanced 30 V V_{GS} rating
- Isolated package
- High voltage isolation = 2.5 kV_{RMS} (t = 60 s, f = 60 Hz)
- Sink to lead creepage distance = 4.8 mm
- Repetitive avalanche rated
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

DESCRIPTION

This series of low charge power MOSFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing advanced power MOSFETs technology, the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings. These device improvements combined with the proven ruggedness and reliability that are characteristic of Power MOSFETs offer the designer a new standard in power transistors for switching applications.

The TO-220 FULLPAK eliminates the need for additional insulating hardware. The molding compound used provides a high isolation capability and low thermal resistance between the tab and external heatsink.

PRODUCT SUMMARY		
V_{DS} (V)	400	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.55
Q_g max. (nC)	39	
Q_{gs} (nC)	10	
Q_{gd} (nC)	19	
Configuration	Single	

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	IRFI740GLCPbF

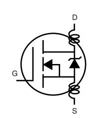
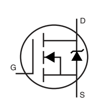
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	400	V
Gate-source voltage			V_{GS}	± 30	
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	5.7	A
		T_C = 100 °C		3.6	
Pulsed drain current [a]			I_{DM}	23	
Linear derating factor				0.32	W/°C
Single pulse avalanche energy [b]			E_{AS}	310	mJ
Repetitive avalanche current [a]			I_{AR}	5.7	A
Repetitive avalanche energy [a]			E_{AR}	4.0	mJ
Maximum power dissipation	T_C = 25 °C		P_D	40	W
Peak diode recovery dV/dt [c]			dV/dt	4.0	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d]	For 10 s			300	
Mounting torque	M3 screw			0.6	Nm

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 16 mH, R_g = 25 Ω, I_{AS} = 5.7 A (see fig. 12)
c. I_{SD} ≤ 10 A, dI/dt ≤ 120 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C
d. 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	R_{thJA}	-	65	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	3.1	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-ssource breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA		400	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.76	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		2.0	-	4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V		-	-	25	μA
		V_{DS} = 320 V, V_{GS} = 0 V, T_J = 125 °C		-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 3.4 A [b]	-	-	0.55	Ω
Forward transconductance	g_{fs}	V_{DS} = 50 V, I_D = 6.0 A [b]		3.0	-	-	S
Dynamic							
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1100	-	pF
Output capacitance	C_{oss}			-	190	-	
Reverse transfer capacitance	C_{rss}			-	18	-	
Drain to sink capacitance	C	f = 1.0 MHz		-	12	-	
Total gate charge	Q_g	V_{GS} = 10 V	I_D = 10 A, V_{DS} = 320 V, see fig. 6 and 13 [b]	-	-	39	nC
Gate-source charge	Q_{gs}			-	-	10	
Gate-drain charge	Q_{gd}			-	-	19	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 200 V, I_D = 10 A, R_g = 9.1Ω, R_D= 20 Ω, see fig. 10 [b]		-	11	-	ns
Rise time	t_r			-	31	-	
Turn-off delay time	$t_{d(off)}$			-	25	-	
Fall time	t_f			-	20	-	
Gate input resistance	R_g	f = 1 MHz, open drain		0.3	-	1.7	Ω
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal source inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	5.7	A
Pulsed diode forward current [a]	I_{SM}			-	-	23	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = 5.7 A, V_{GS} = 0 V [b]		-	-	2.0	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = 10 A, dI/dt = 100 A/μs [b]		-	380	570	ns
Body diode reverse recovery charge	Q_{rr}			-	2.8	4.2	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

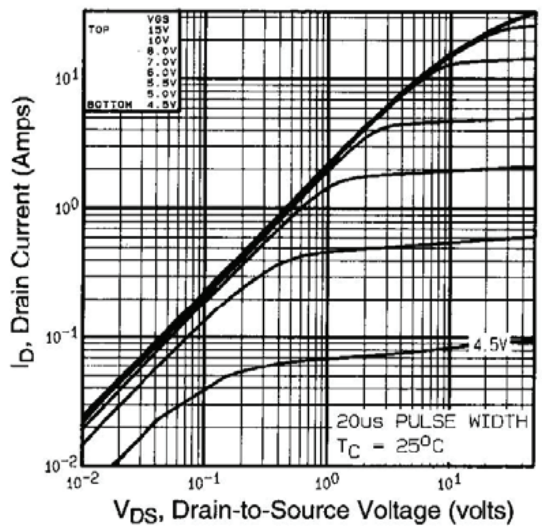


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

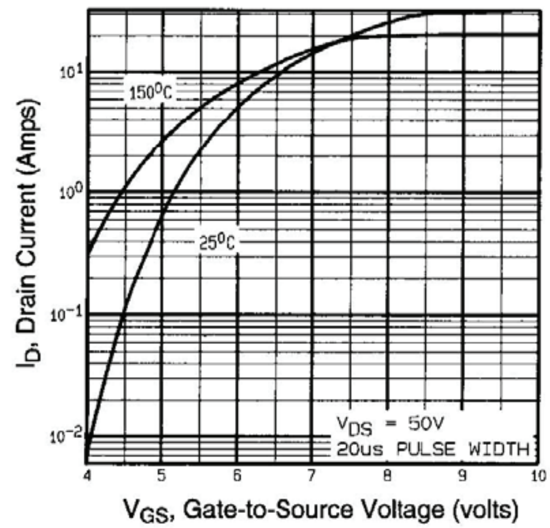


Fig. 3 - Typical Transfer Characteristics

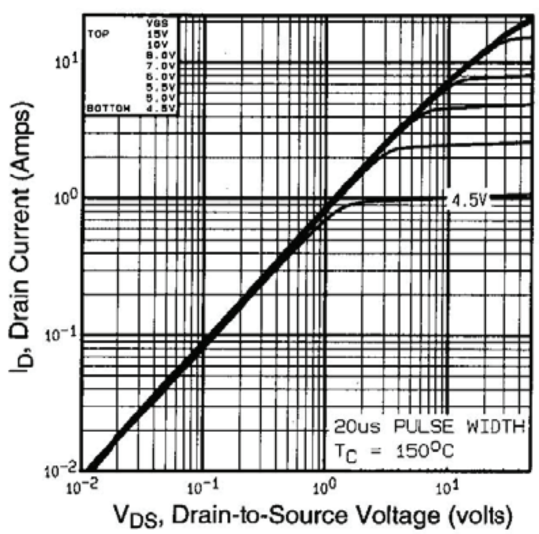


Fig. 2 - Typical Output Characteristics, T_C= 150 °C

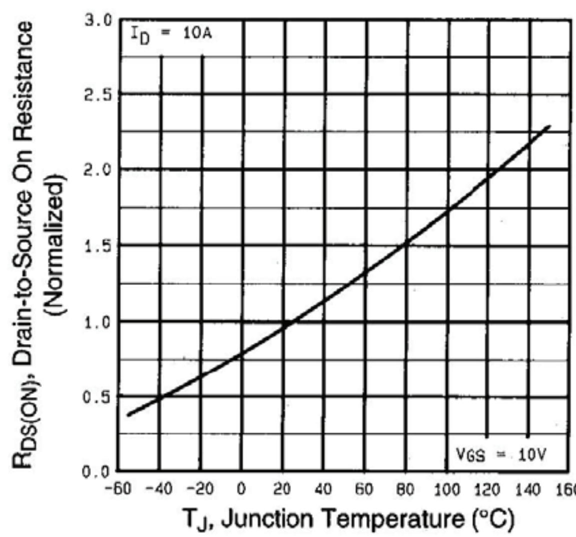


Fig. 4 - Normalized On-Resistance vs. Temperature

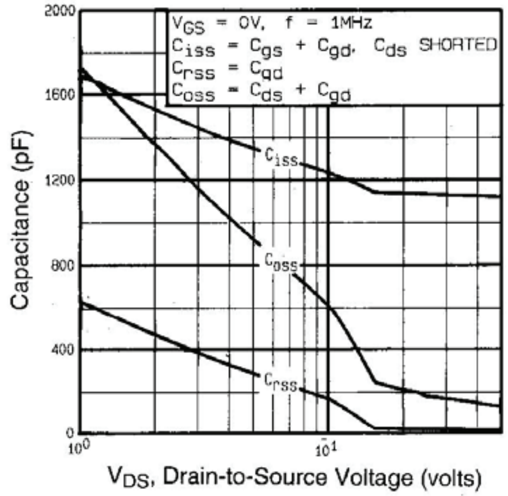


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

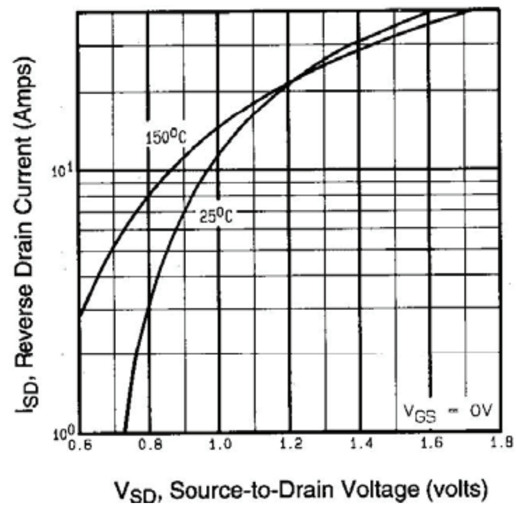


Fig. 7 - Typical Source-Drain Diode Forward Voltage

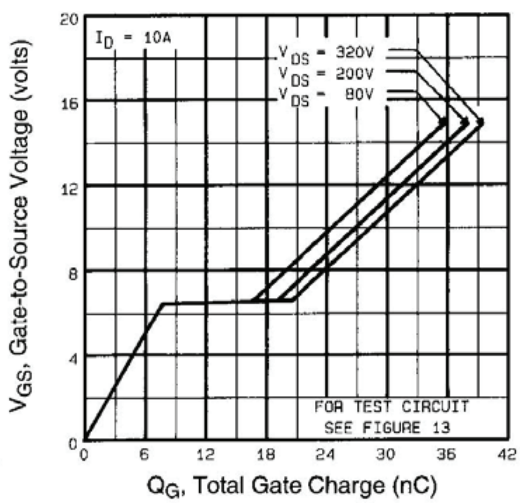


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

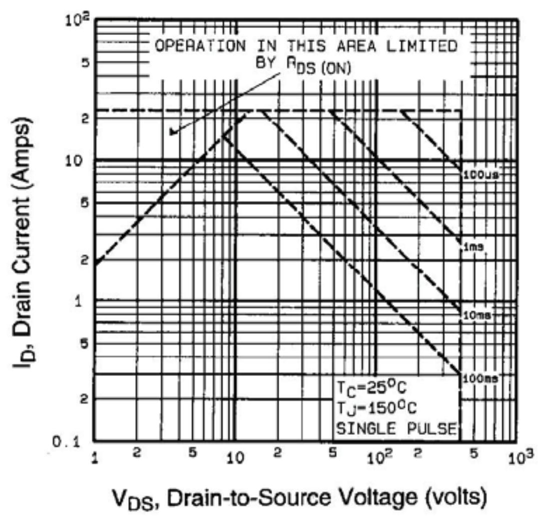


Fig. 8 - Maximum Safe Operating Area

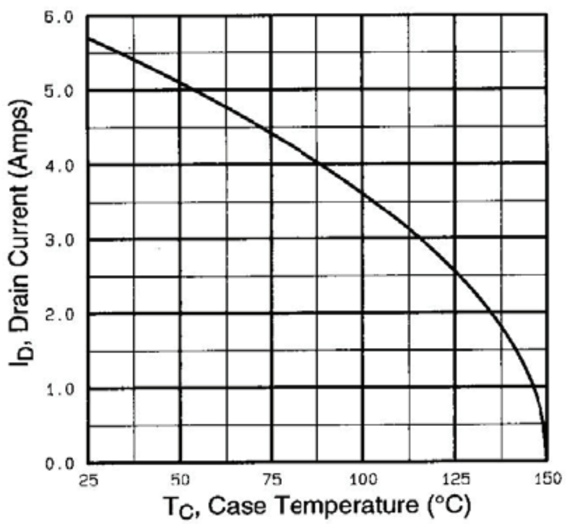


Fig. 9 - Maximum Drain Current vs. Case Temperature

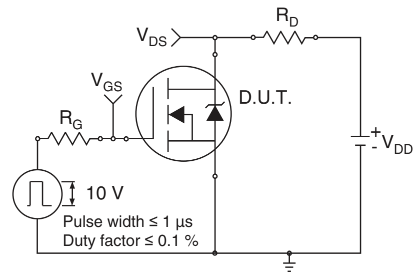


Fig. 10a - Switching Time Test Circuit

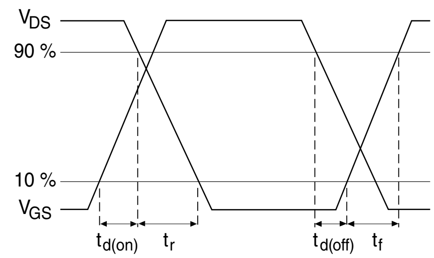


Fig. 10b - Switching Time Waveforms

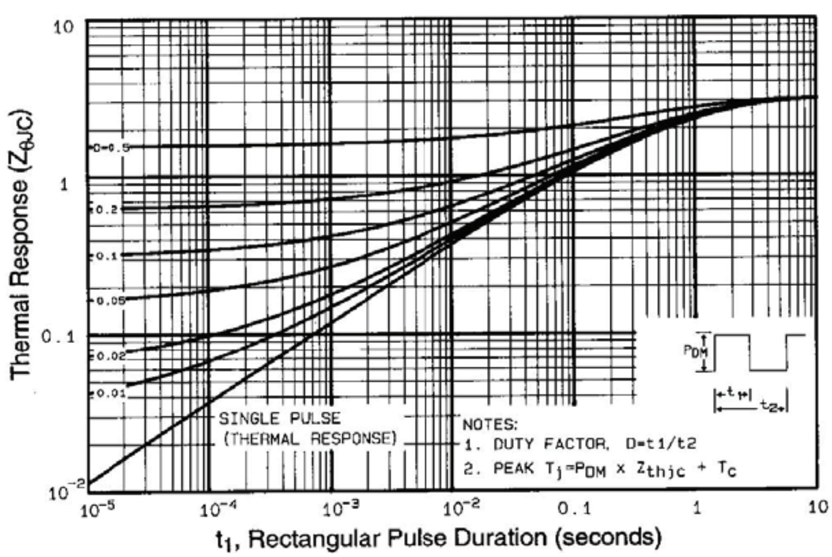


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

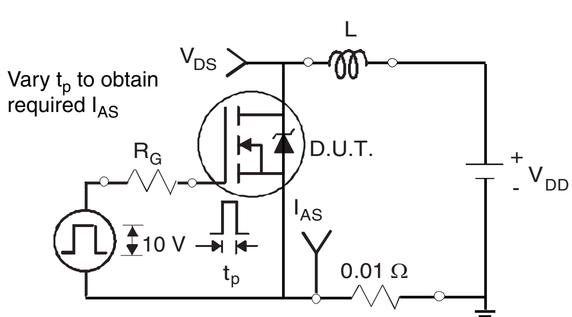


Fig. 12a - Unclamped Inductive Test Circuit

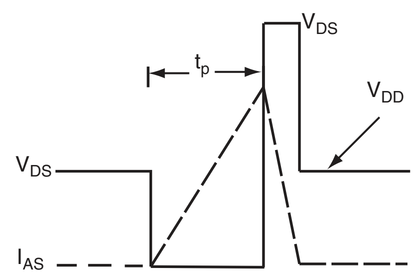


Fig. 12b - Unclamped Inductive Waveforms

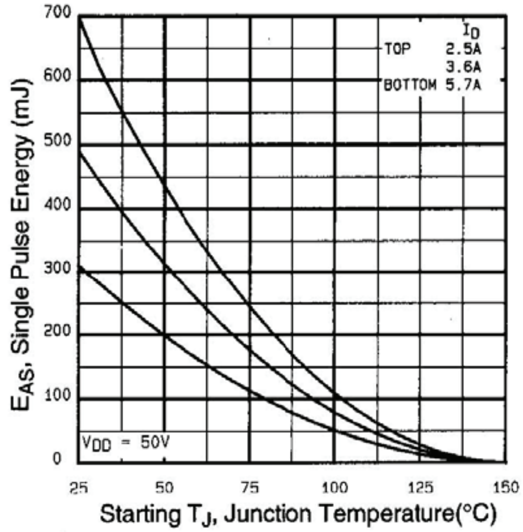


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

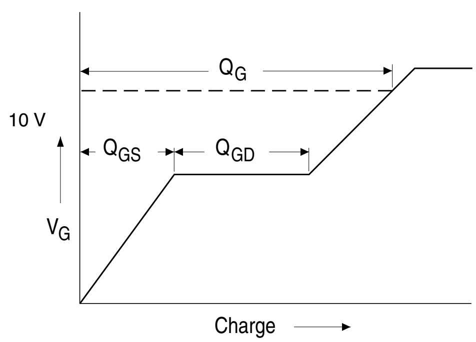


Fig. 13a - Basic Gate Charge Waveform

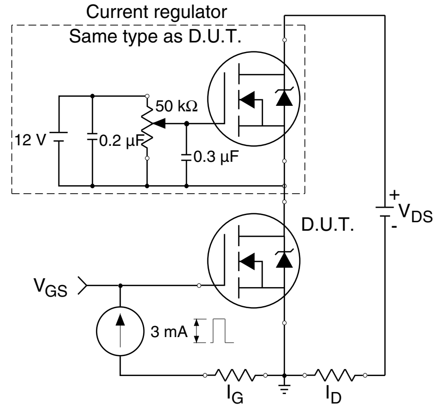
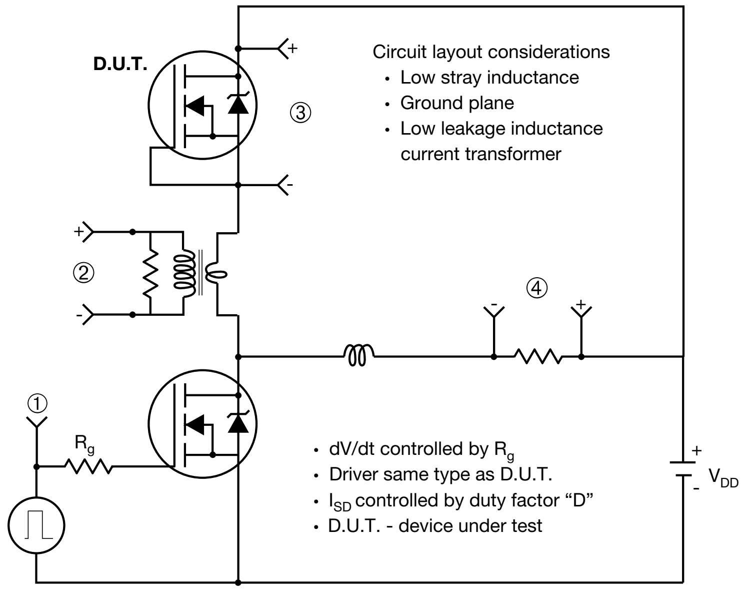
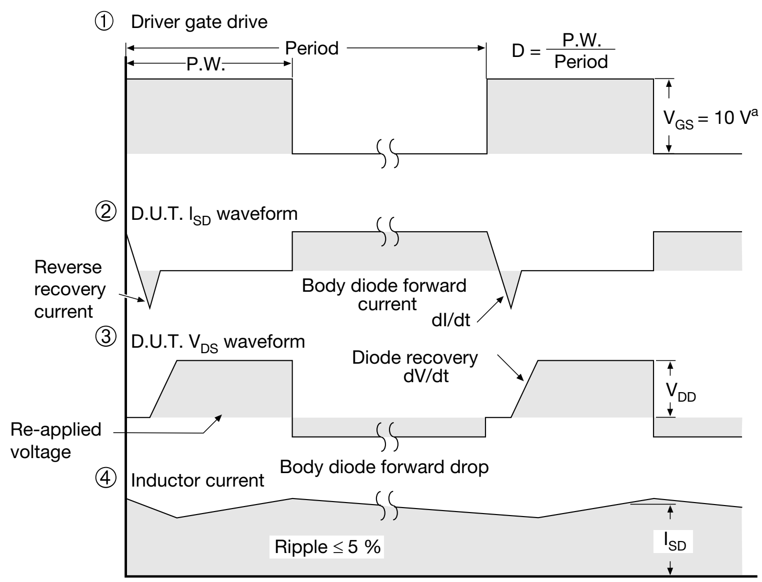


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





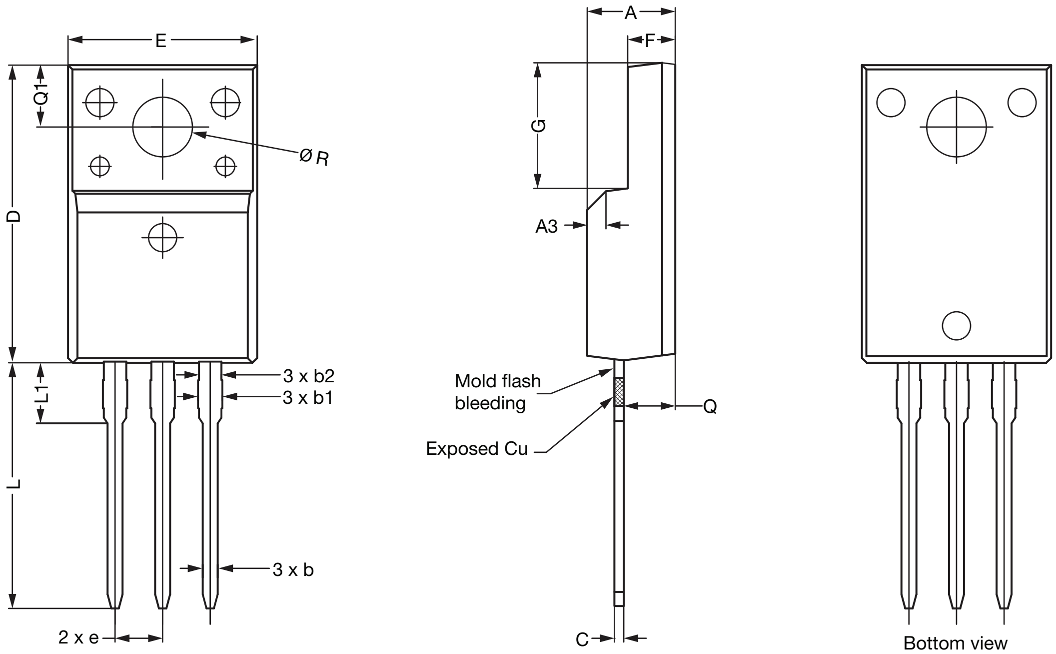
Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

TO-220 FULLPAK (High Voltage)

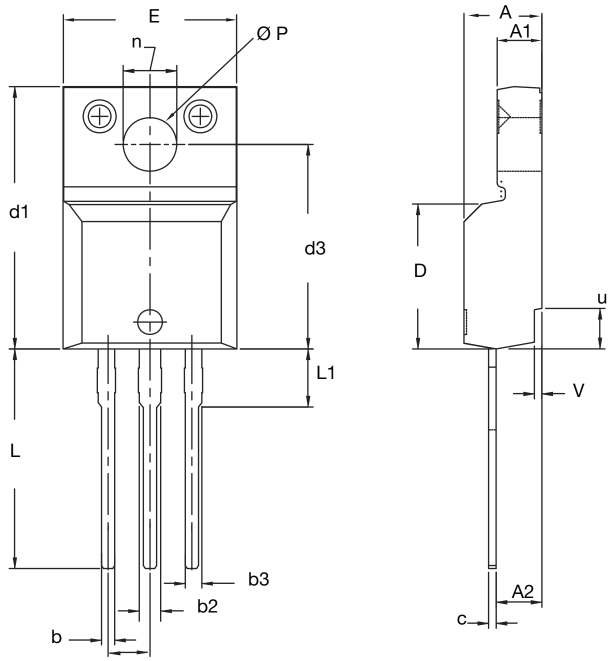
OPTION 1: FACILITY CODE = 9



	MILLIMETERS		
DIM.	MIN.	NOM.	MAX.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54 BSC		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
Ø R	3.08	3.18	3.28

Notes
1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking

OPTION 2: FACILITY CODE = Y



	MILLIMETERS		INCHES	
DIM.	**MIN.**	**MAX.**	**MIN.**	**MAX.**
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020
ECN: E19-0180-Rev. D, 08-Apr-2019 DWG: 5972				

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