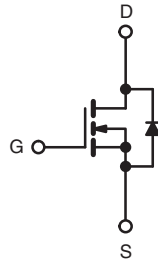
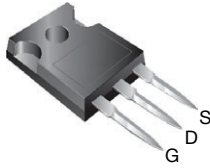


Power MOSFET

TO-247AC


N-Channel MOSFET

FEATURES

- Super fast body diode eliminates the need for external diodes in ZVS applications
- Lower gate charge results in simpler drive requirements
- Enhanced dV/dt capabilities offer improved ruggedness
- Higher gate voltage threshold offers improved noise immunity
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS*
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Zero voltage switching SMPS
- Telecom and server power supplies
- Uninterruptible power supplies
- Motor control applications

PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	0.15
Q_g (max.) (nC)	210	
Q_{gs} (nC)	58	
Q_{gd} (nC)	100	
Configuration	Single	

ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free	IRFP31N50LPbF

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	500	V	
Gate-source voltage	V_{GS}	± 30		
Continuous drain current	V_{GS} at 10 V	$T_C = 25^\circ\text{C}$	A	
		$T_C = 100^\circ\text{C}$		
Pulsed drain Current ^a	I_{DM}	124		
Linear derating Factor		3.7	W/ $^\circ\text{C}$	
Single pulse avalanche energy ^b	E_{AS}	460	mJ	
Repetitive avalanche current ^a	I_{AR}	31	A	
Repetitive avalanche energy ^a	E_{AR}	46	mJ	
Maximum power dissipation	$T_C = 25^\circ\text{C}$	P_D	W	
Peak diode recovery dV/dt ^c	dV/dt	19	V/ns	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
Soldering recommendations (peak temperature) ^d	for 10 s	300 ^d		
Mounting torque	6-32 or M3 screw		10	lbf · in
			1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting $T_J = 25^\circ\text{C}$, $L = 1$ mH, $R_g = 25 \Omega$, $I_{AS} = 31$ A (see fig. 12)
- $I_{SD} \leq 31$ A, $dI/dt \leq 422$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$
- 1.6 mm from case



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.24	-	
Maximum junction-to-case (drain)	R_{thJC}	-	0.26	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	500	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.28	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 500\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	50	μA
		$V_{DS} = 400\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	2.0	mA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 19\text{ A}^b$	-	0.15	0.18	Ω
Forward transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 19\text{ A}^b$	15	-	-	S
Dynamic						
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5	-	5000	-	pF
Output capacitance	C_{oss}		-	553	-	
Reverse transfer capacitance	C_{rss}		-	59	-	
Output capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}$, $f = 1.0\text{ MHz}$	-	6630	-
			$V_{DS} = 400\text{ V}$, $f = 1.0\text{ MHz}$	-	155	-
Effective output capacitance	$C_{oss\text{ eff.}}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 0\text{ V to } 400\text{ V}^c$	-	276	-
Effective output capacitance (energy related)	$C_{oss\text{ eff. (ER)}}$			-	200	-
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 31\text{ A}$, $V_{DS} = 400\text{ V}$, see fig. 7 and 13 ^b	-	-	210
Gate-source charge	Q_{gs}			-	-	58
Gate-drain charge	Q_{gd}			-	-	100
Internal gate resistance	R_g	$f = 1\text{ MHz}$, open drain		-	1.1	-
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 250\text{ V}$, $I_D = 31\text{ A}$, $R_g = 4.3\text{ }\Omega$, see fig. 10 ^b	-	28	-	ns
Rise time	t_r		-	115	-	
Turn-off delay time	$t_{d(off)}$		-	54	-	
Fall time	t_f		-	53	-	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p-n junction diode 	-	-	31	A
Pulsed diode forward current ^a	I_{SM}		-	-	124	
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 31\text{ A}$, $V_{GS} = 0\text{ V}^b$		-	-	1.5
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 31\text{ A}$		-	170	250
		$T_J = 125\text{ }^\circ\text{C}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	220	330
Body diode reverse recovery charge	Q_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 31\text{ A}$, $V_{GS} = 0\text{ V}^b$		-	570	860
		$T_J = 125\text{ }^\circ\text{C}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	1.2	1.8
Reverse recovery current	I_{RRM}	$T_J = 25\text{ }^\circ\text{C}$		-	7.9	12
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$
- c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}
 $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

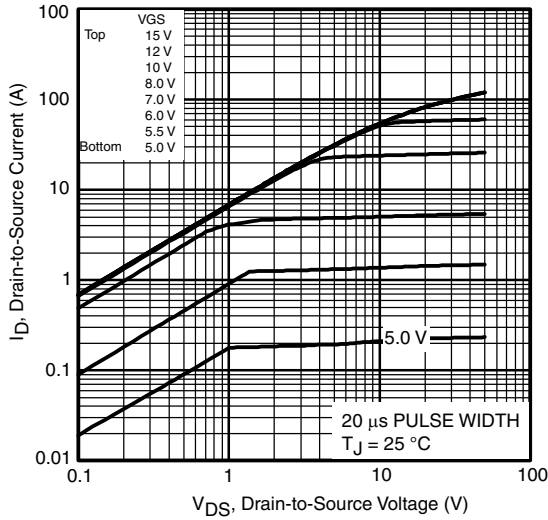


Fig. 1 - Typical Output Characteristics

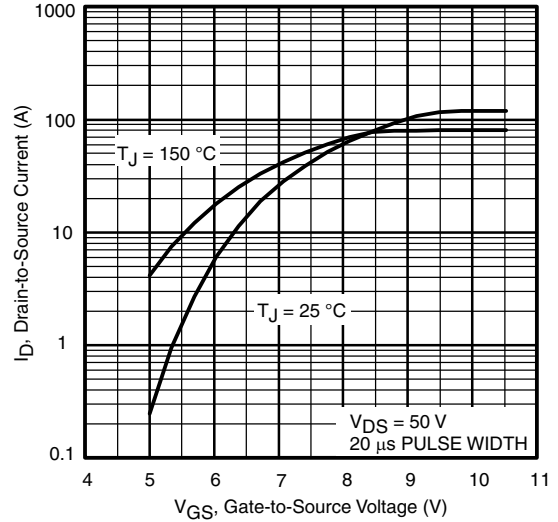


Fig. 3 - Typical Transfer Characteristics

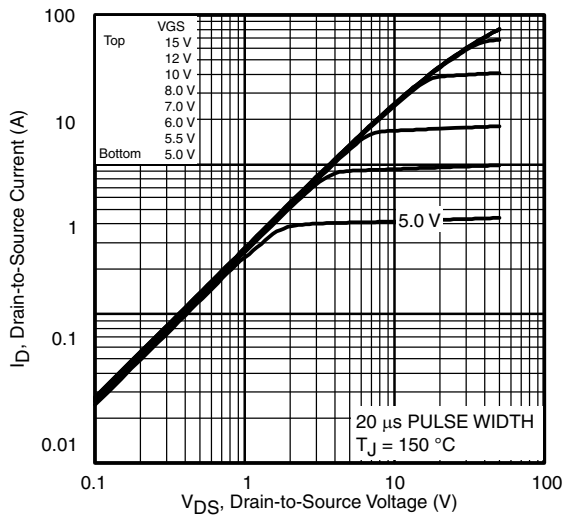


Fig. 2 - Typical Output Characteristics

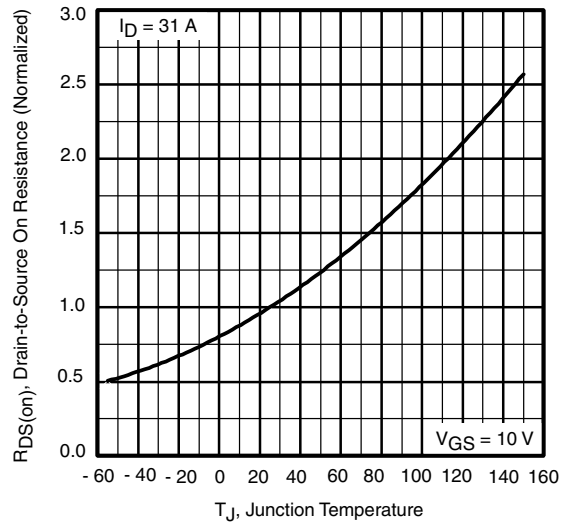


Fig. 4 - Normalized On-Resistance vs. Temperature

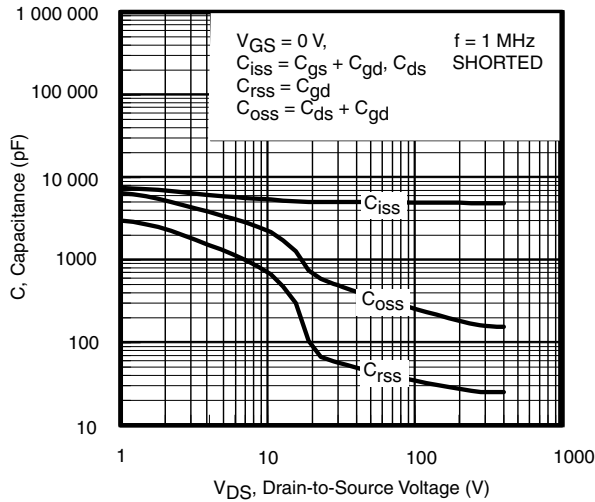


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

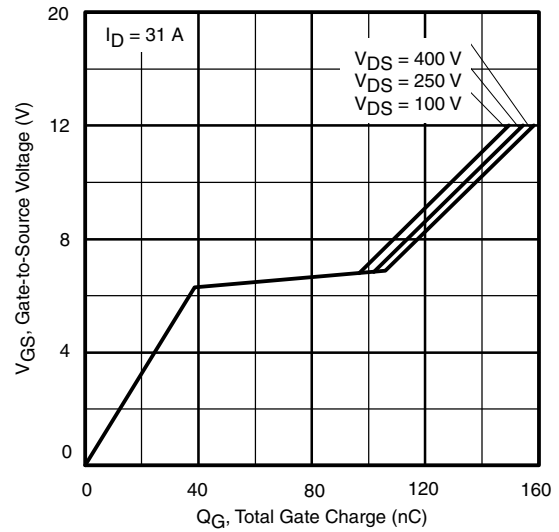


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

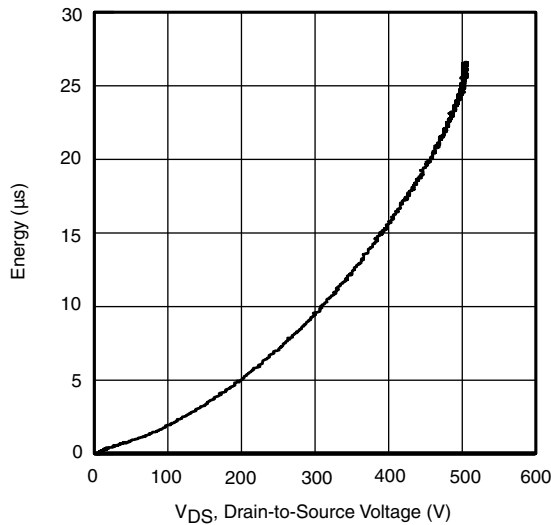


Fig. 6 - Output Capacitance Stored Energy vs. V_{DS}

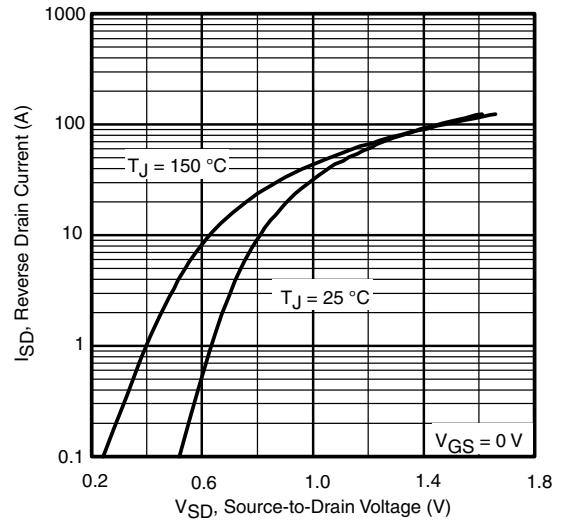


Fig. 8 - Typical Source Drain Diode Forward Voltage

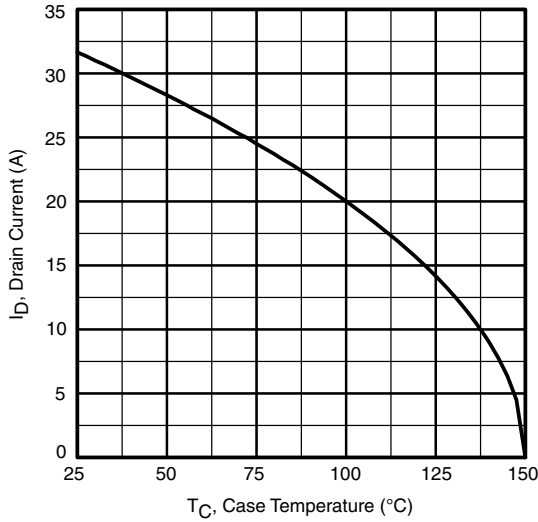


Fig. 9 - Maximum Drain Current vs. Case Temperature

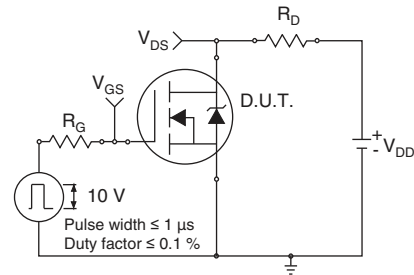


Fig. 10 - Switching Time Test Circuit

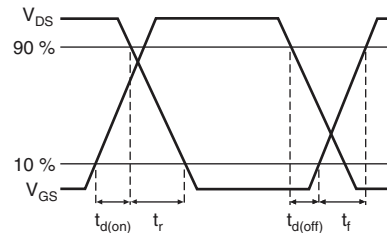


Fig. 11 - Switching Time Waveforms

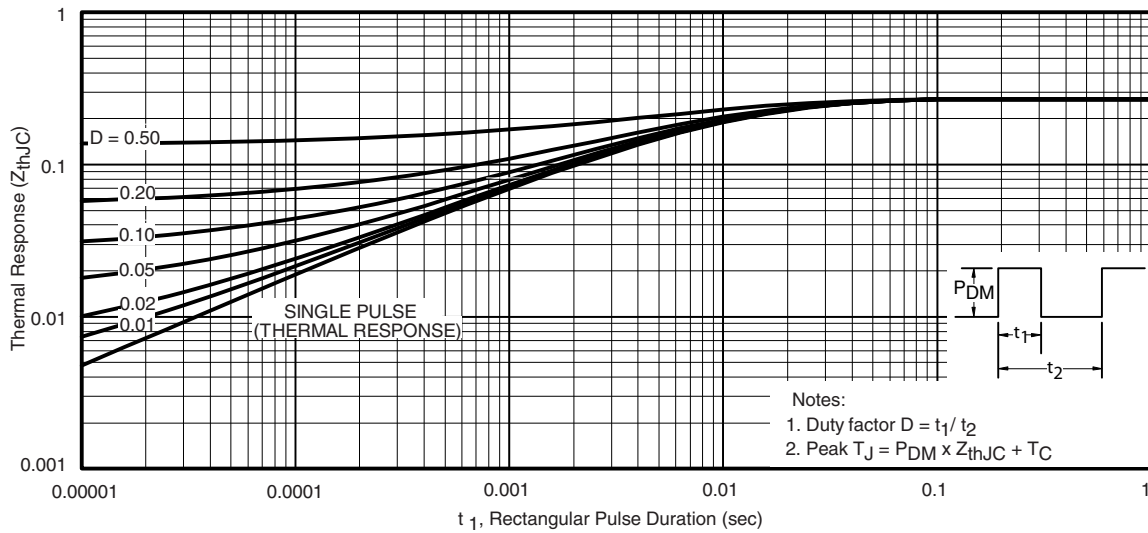


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

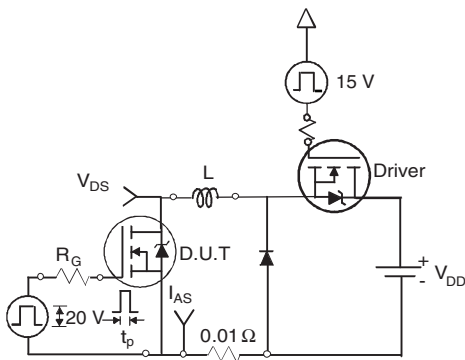


Fig. 13 - Unclamped Inductive Test Circuit

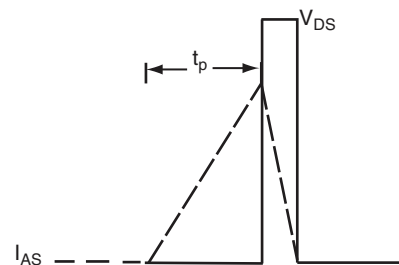


Fig. 14 - Unclamped Inductive Waveforms

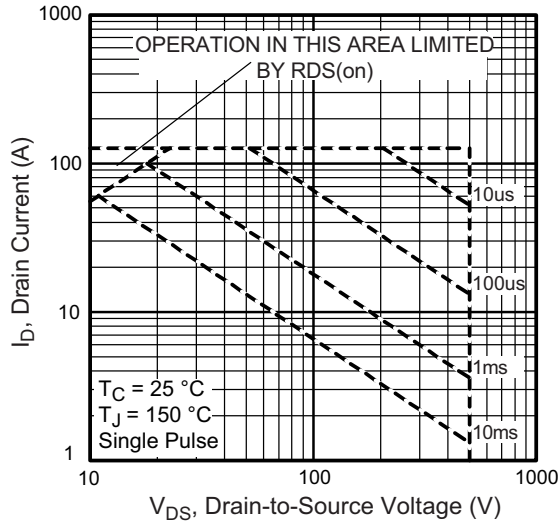


Fig. 15 - Maximum Avalanche Energy vs. Drain Current

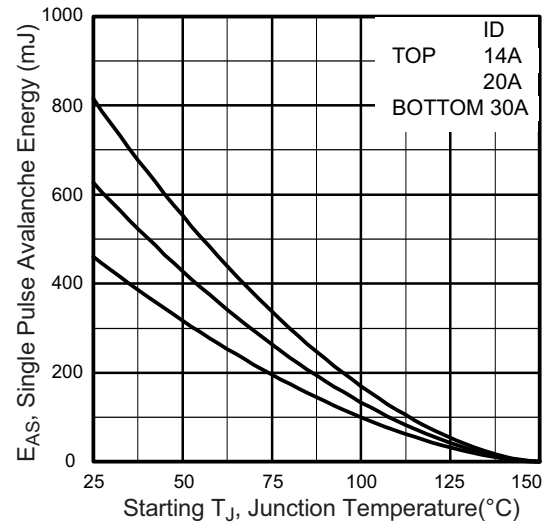


Fig. 16 - Gate Charge Test Circuit

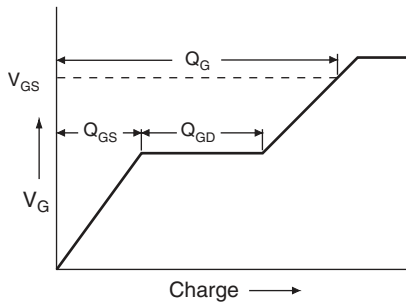


Fig. 17 - Maximum Safe Operating Area

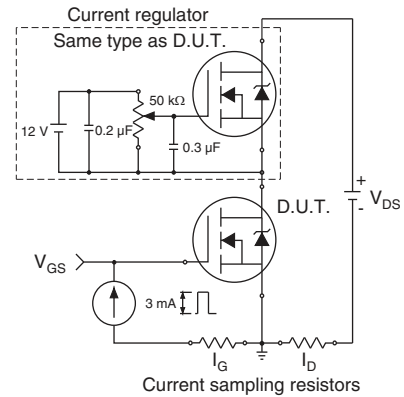
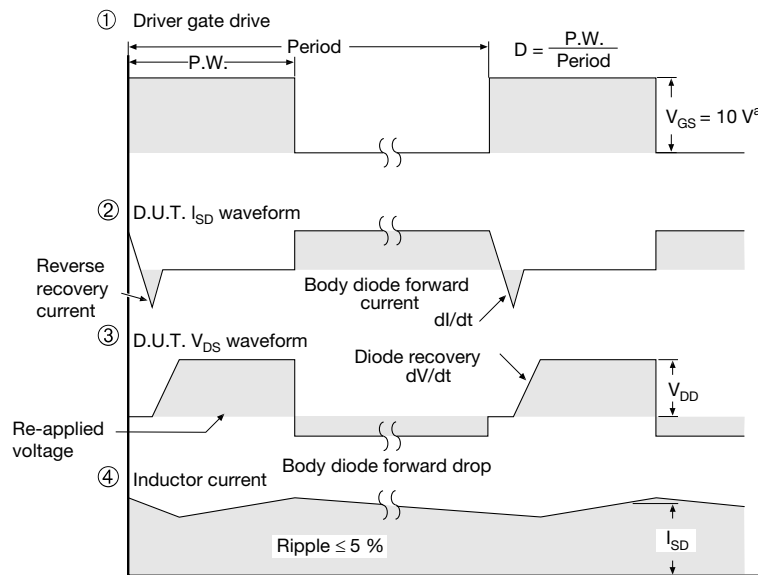
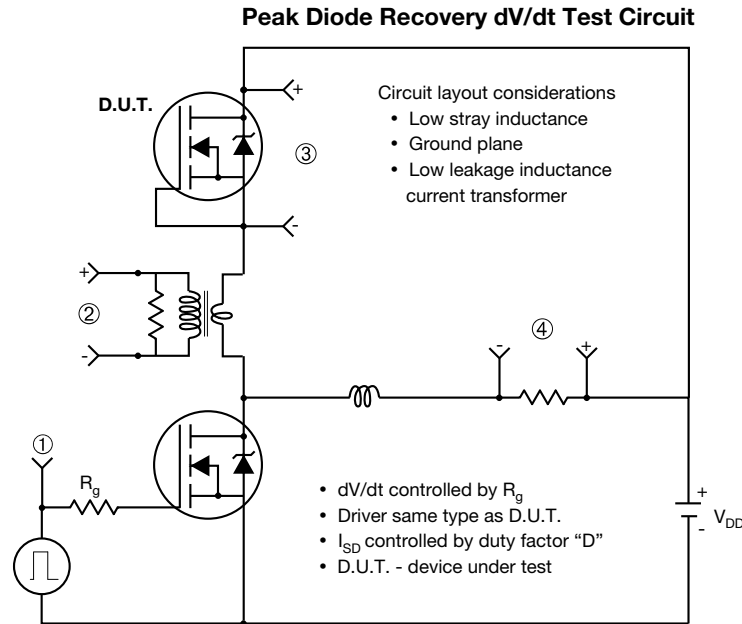


Fig. 18 - Basic Gate Charge Waveform



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 19 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91220.



VERSION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c



VERSION 3: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	4.65	5.31
A1	2.21	2.59
A2	1.17	1.37
b	0.99	1.40
b1	0.99	1.35
b2	1.65	2.39
b3	1.65	2.34
b4	2.59	3.43
b5	2.59	3.38
c	0.38	0.89
c1	0.38	0.84
D	19.71	20.70
D1	13.08	-

MILLIMETERS		
DIM.	MIN.	MAX.
D2	0.51	1.35
E	15.29	15.87
E1	13.46	-
e	5.46 BSC	
k	0.254	
L	14.20	16.10
L1	3.71	4.29
N	7.62 BSC	
P	3.56	3.66
P1	-	7.39
Q	5.31	5.69
R	4.52	5.49
S	5.51 BSC	

ECN: E22-0452-Rev. G, 31-Oct-2022
 DWG: 5971

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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