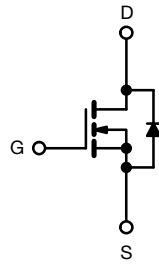
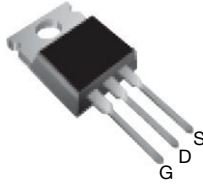


## Power MOSFET

TO-220AB



N-Channel MOSFET

### FEATURES

- Low figure-of-merit  $R_{on} \times Q_g$
- 100 % avalanche tested
- High peak current capability
- $dv/dt$  ruggedness
- Improved  $t_{rr}/Q_{rr}$
- Improved gate charge
- High power dissipations capability
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	560	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	0.225
$Q_g$ max. (nC)	76	
$Q_{gs}$ (nC)	21	
$Q_{gd}$ (nC)	29	
Configuration	Single	

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

### ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free and halogen-free	SiHP18N50C-E3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	500	V
Gate-source voltage	$V_{GS}$	$\pm 30$	
Continuous drain current ( $T_J = 150$ °C) <sup>a</sup>	$V_{GS}$ at 10 V	$T_C = 25$ °C	18
		$T_C = 100$ °C	11
Pulsed drain current <sup>b</sup>	$I_{DM}$	72	A
Linear derating factor		1.8	W/°C
Single pulse avalanche energy <sup>c</sup>	$E_{AS}$	361	mJ
Maximum power dissipation	$P_D$	223	W
Reverse diode $dv/dt$ <sup>d</sup>	$dv/dt$	5	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s	300	


### Notes

- Drain current limited by maximum junction temperature
- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 2.5$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 17$  A
- $I_{SD} \leq 18$  A,  $di/dt \leq 380$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C
- 1.6 mm from case

### THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	62	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	0.56	



<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$	-	0.6	-	$\text{V}/^\circ\text{C}$
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	0.225	0.270	$\Omega$
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 10\text{ A}$	-	6.4	-	S
<b>Dynamic</b>						
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	-	2451	2942	$\mu\text{F}$
Output capacitance	$C_{oss}$		-	300	360	
Reverse transfer capacitance	$C_{riss}$		-	26	32	
Total gate charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 18\text{ A}, V_{DS} = 400\text{ V}$	-	65	76	nC
Gate-source charge	$Q_{gs}$		-	21	-	
Gate-drain charge	$Q_{gd}$		-	29	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 18\text{ A}, V_{GS} = 10\text{ V}, R_g = 7.5\text{ }\Omega$	-	80	-	ns
Rise time	$t_r$		-	27	-	
Turn-off delay time	$t_{d(off)}$		-	32	-	
Fall time	$t_f$		-	44	-	
Gate input resistance	$R_g$	$f = 1\text{ MHz}, \text{open drain}$	-	1.1	-	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	18	A
Pulsed diode forward current	$I_{SM}$		-	-	72	
Diode forward voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 18\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.5	V
Reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S, di/dt = 100\text{ A}/\mu\text{s}, V_R = 35\text{ V}$	-	503	-	ns
Reverse recovery charge	$Q_{rr}$		-	6.7	-	$\mu\text{C}$
Reverse recovery current	$I_{RRM}$		-	30	-	A

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature

The information shown here is a preliminary product proposal, not a commercial product datasheet. Vishay Siliconix is not committed to produce this or any similar product. This information should not be used for design purposes, nor construed as an offer to furnish or sell such products.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

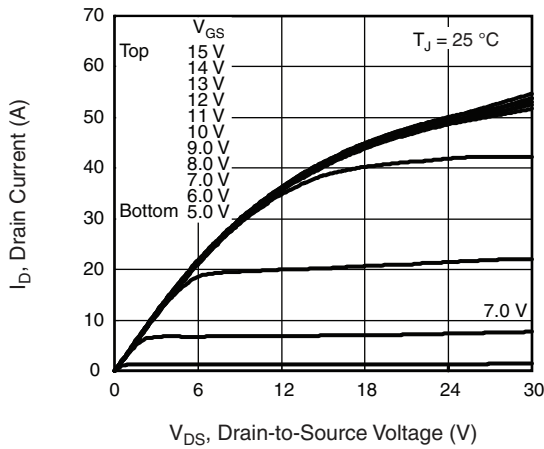


Fig. 1 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$

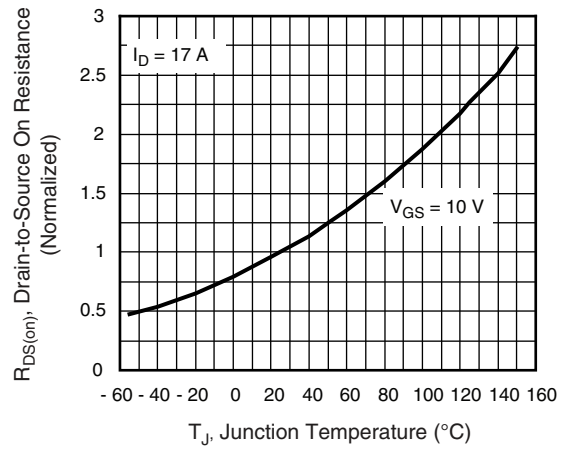


Fig. 4 - Normalized On-Resistance vs. Temperature

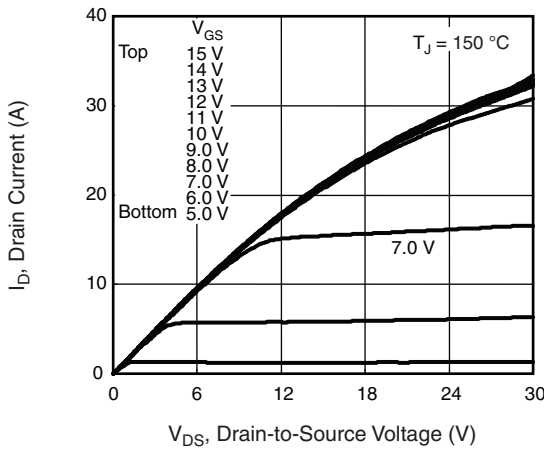


Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$

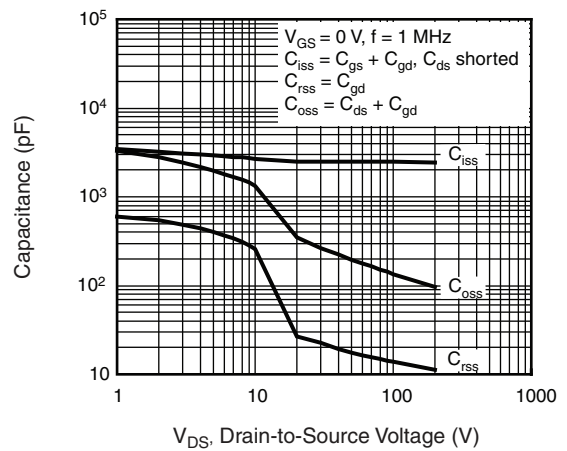


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

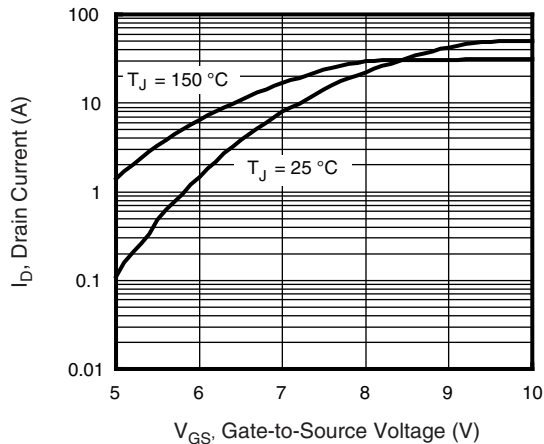


Fig. 3 - Typical Transfer Characteristics

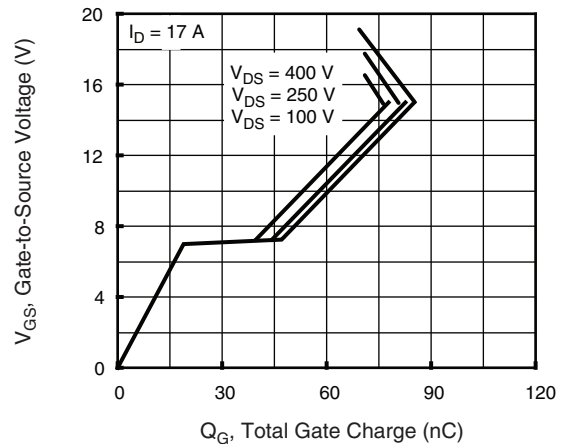
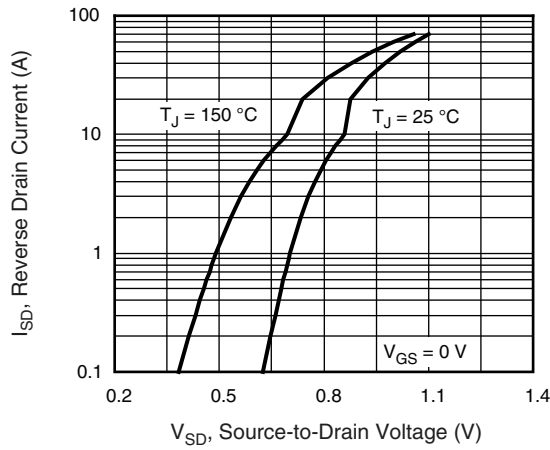
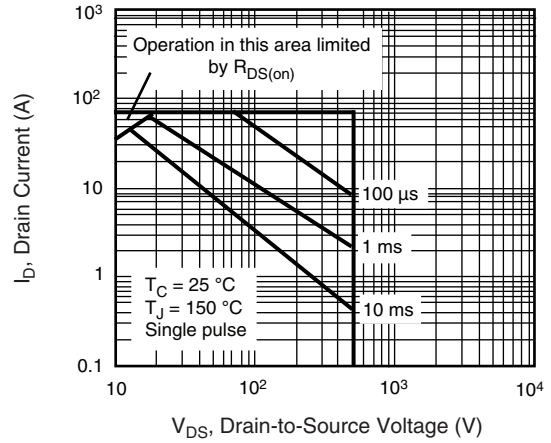


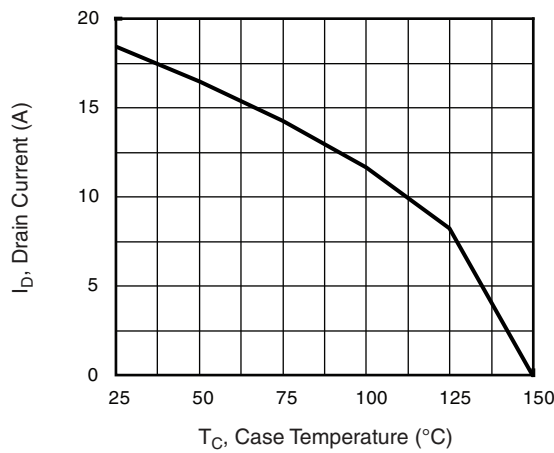
Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



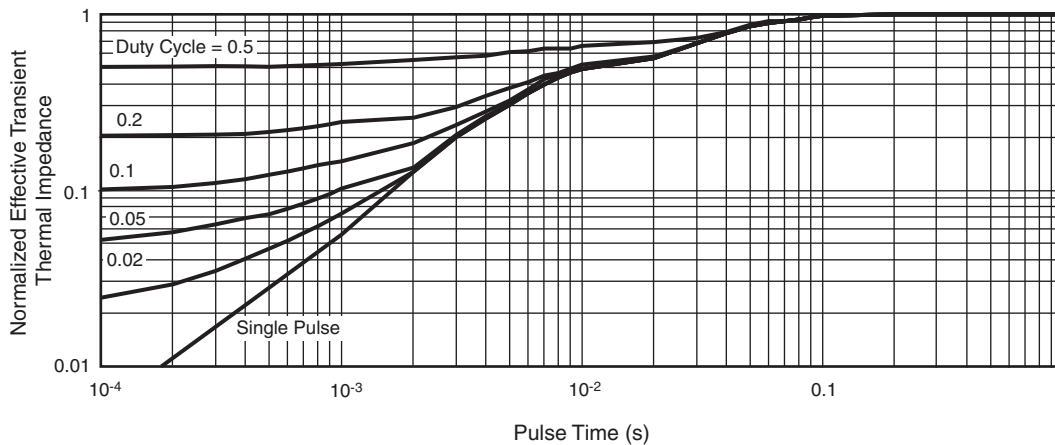
**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



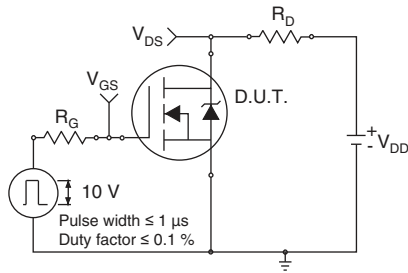
**Fig. 8 - Maximum Safe Operating Area**



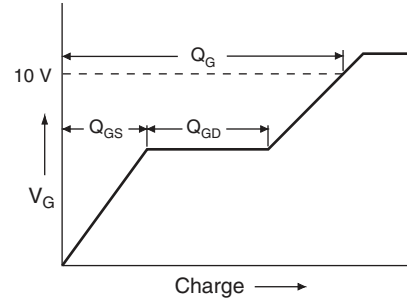
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



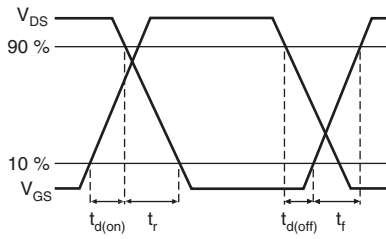
**Fig. 10 - Normalized Thermal Transient Impedance, Junction-to-Case**



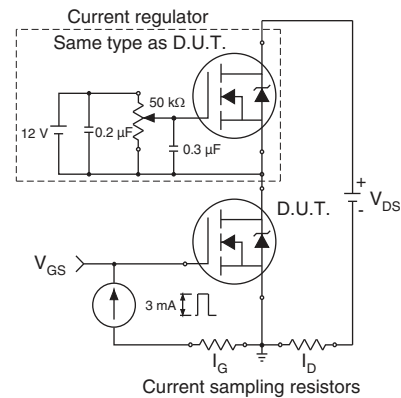
**Fig. 11 - Switching Time Test Circuit**



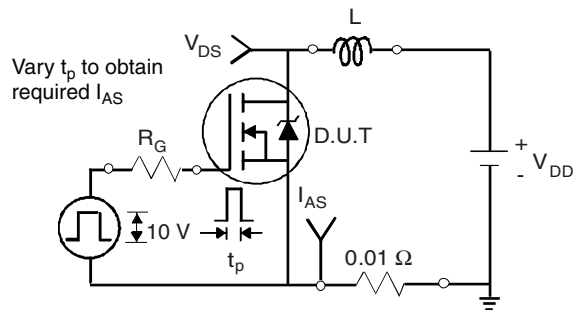
**Fig. 15 - Basic Gate Charge Waveform**



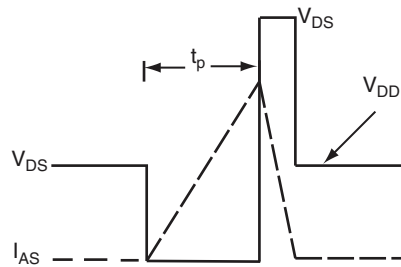
**Fig. 12 - Switching Time Waveforms**



**Fig. 16 - Gate Charge Test Circuit**

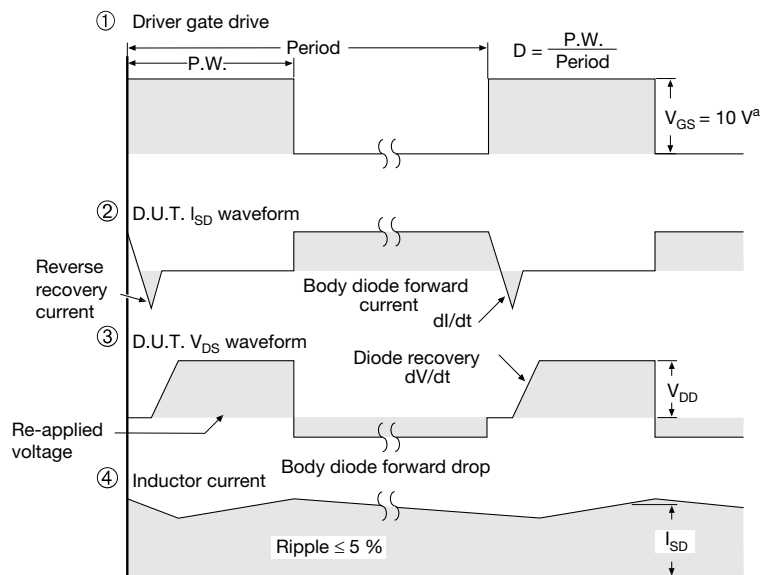
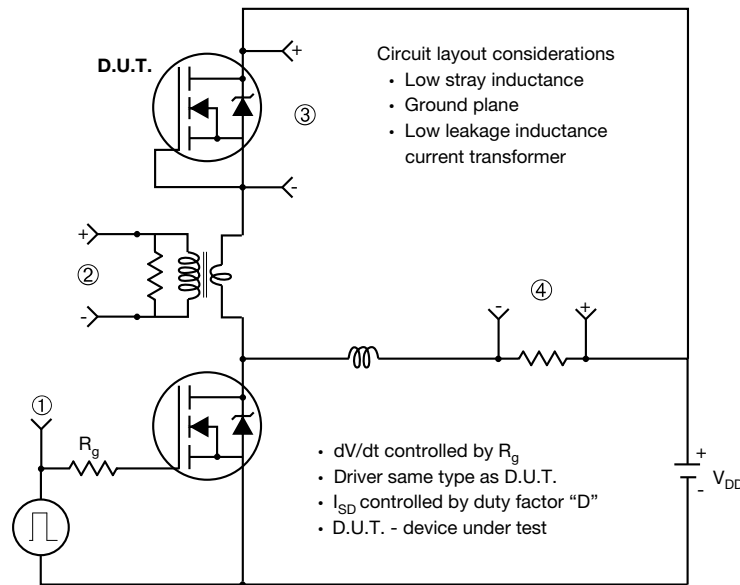


**Fig. 13 - Unclamped Inductive Test Circuit**



**Fig. 14 - Unclamped Inductive Waveforms**

### Peak Diode Recovery dV/dt Test Circuit



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 17 - For N-Channel**

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# TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: E21-0621-Rev. D, 04-Nov-2021  
DWG: 6031

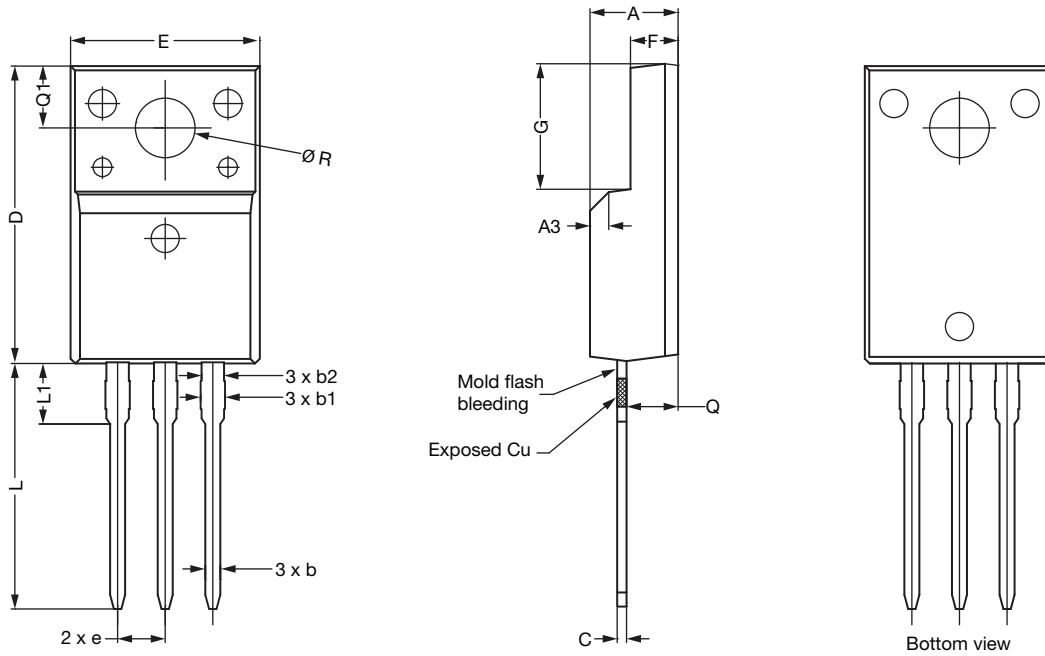
**Note**

- M\* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



### TO-220 FULLPAK (High Voltage)

**OPTION 1: FACILITY CODE = 9**



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54 BSC		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
$\varnothing R$	3.08	3.18	3.28

**Notes**

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking





OPTION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020

ECN: E19-0180-Rev. D, 08-Apr-2019  
DWG: 5972

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking



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