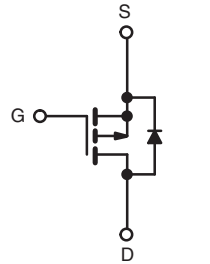
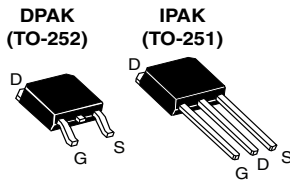


Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	- 50
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V 0.50
Q_g (Max.) (nC)	9.1
Q_{gs} (nC)	3.0
Q_{gd} (nC)	5.9
Configuration	Single



P-Channel MOSFET

FEATURES

- Surface Mountable (Order as IRFR9010, SiHFR9010)
- Straight Lead Option (Order as IRFU9010, SiHFU9010)
- Repetitive Avalanche Ratings
- Dynamic dV/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

DESCRIPTION

The power MOSFET technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dV/dt capability.

The power MOSFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

Surface mount packages enhance circuit performance by reducing stray inductances and capacitance. The DPAK (TO-252) surface mount package brings the advantages of power MOSFETs to high volume applications where PC Board surface mounting is desirable. The surface mount option IRFR9010, SiHFR9010 is provided on 16 mm tape. The straight lead option IRFU9010, SiHFU9010 of the device is called the IPAK (TO-251).

They are well suited for applications where limited heat dissipation is required such as, computers and peripherals, telecommunication equipment, DC/DC converters, and a wide range of consumer products.

ORDERING INFORMATION				
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and Halogen-free	SiHFR9010-GE3	SiHFR9010TR-GE3 ^a	SiHFR9010TRL-GE3 ^a	SiHFU9010-GE3
Lead (Pb)-free	IRFR9010PbF	IRFR9010TRPbF ^a	IRFR9010TRLPbF ^a	IRFU9010PbF
	SiHFR9010-E3	SiHFR9010T-E3 ^a	SiHFR9010TL-E3 ^a	SiHFU9010-E3

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	V_{DS}		- 50	V
Gate-Source Voltage	V_{GS}		± 20	
Continuous Drain Current	V_{GS} at - 10 V	$T_C = 25$ °C	- 5.3	A
		$T_C = 100$ °C	- 3.3	
Pulsed Drain Current ^a	I_{DM}		- 21	
Linear Derating Factor			0.20	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}		136	mJ
Repetitive Avalanche Current ^a	I_{AR}		- 5.3	A
Repetitive Avalanche Energy ^a	E_{AR}		2.5	mJ
Maximum Power Dissipation	$T_C = 25$ °C		P_D	25
Peak Diode Recovery dV/dt ^c			dV/dt	5.8
Operating Junction and Storage Temperature Range	T_J, T_{stg}		- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) ^d	for 10 s		300	

Notes

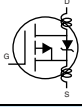

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14).
- $V_{DD} = -25$ V, starting $T_J = 25$ °C, $L = 9.7$ mH, $R_g = 25$ Ω , peak $I_L = -5.3$ A.
- $I_{SD} \leq -5.3$ A, $dI/dt \leq -80$ A/ μ s, $V_{DD} \leq 40$ V, $T_J \leq 150$ °C, suggested $R_g = 24$ Ω .
- 0.063" (1.6 mm) from case.



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R _{thJA}	-	-	110	°C/W
Case-to-Sink	R _{thCS}	-	1.7	-	
Maximum Junction-to-Case (Drain) ^a	R _{thJC}	-	-	5.0	

Note

a. Mounting pad must cover heatsink surface area.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA		- 50	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA		- 2.0	-	- 4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 500	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = max. rating, V _{GS} = 0 V		-	-	- 250	μA
		V _{DS} = 0.8 x max. rating, V _{GS} = 0 V, T _J = 125 °C		-	-	- 1000	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = - 10 V	I _D = - 2.8 A ^b	-	0.35	0.5	Ω
Forward Transconductance	g _{fs}	V _{DS} ≤ - 50 V, I _{DS} = - 2.8 A		1.1	1.7	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = - 25 V, f = 1.0 MHz, see fig. 9		-	240	-	pF
Output Capacitance	C _{oss}			-	160	-	
Reverse Transfer Capacitance	C _{rss}			-	30	-	
Total Gate Charge	Q _g	V _{GS} = - 10 V	I _D = - 4.7 A, V _{DS} = 0.8 x max. rating, see fig. 16 (Independent operating temperature)	-	6.1	9.1	nC
Gate-Source Charge	Q _{gs}			-	2.0	3.0	
Gate-Drain Charge	Q _{gd}			-	3.9	5.9	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 25 V, I _D = - 4.7 A, R _g = 24 Ω, R _D = 5.6 Ω, see fig. 15 (Independent operating temperature)		-	6.1	9.2	ns
Rise Time	t _r			-	47	71	
Turn-Off Delay Time	t _{d(off)}			-	13	20	
Fall Time	t _f			-	35	59	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact. 		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 5.3	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	- 18	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = - 5.3 A, V _{GS} = 0 V ^b		-	-	- 5.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = - 4.7 A, di/dt = 100 A/μs ^b		33	75	160	ns
Body Diode Reverse Recovery Charge	Q _{rr}			0.090	0.22	0.52	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14).
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

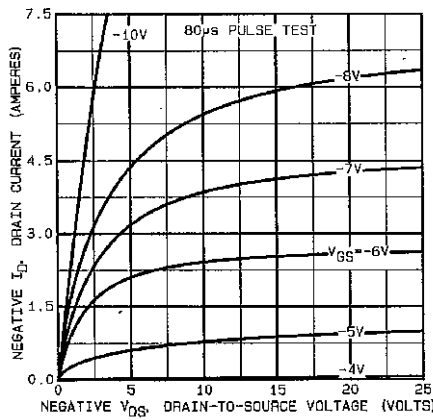


Fig. 1 - Typical Output Characteristics

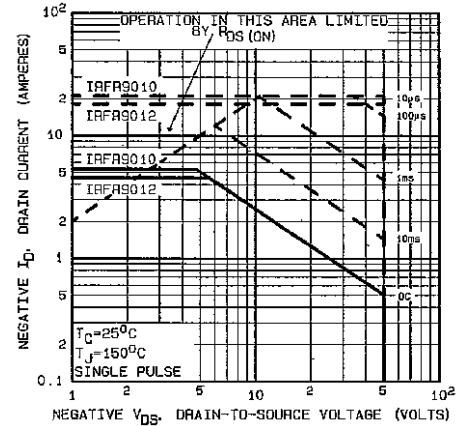


Fig. 4 - Maximum Safe Operating Area

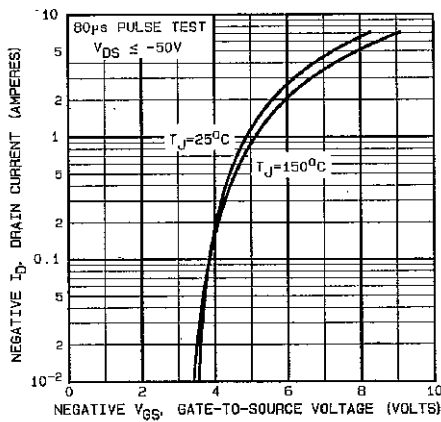


Fig. 2 - Typical Transfer Characteristics

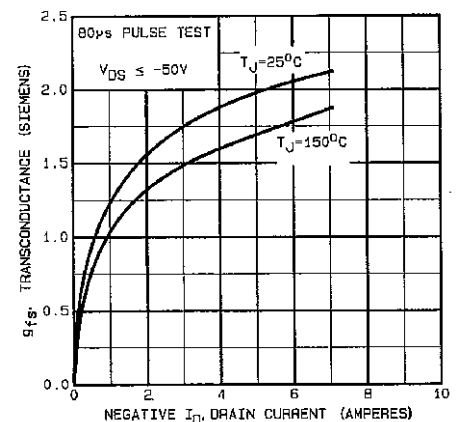


Fig. 5 - Typical Transconductance vs. Drain Current

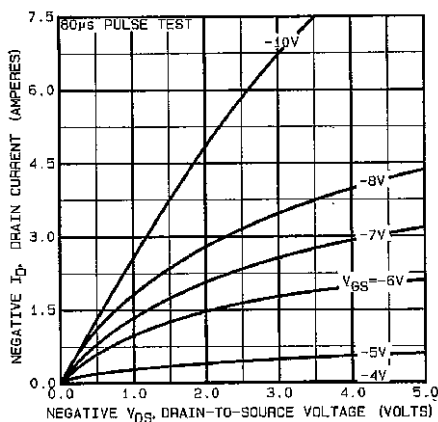


Fig. 3 - Typical Saturation Characteristics

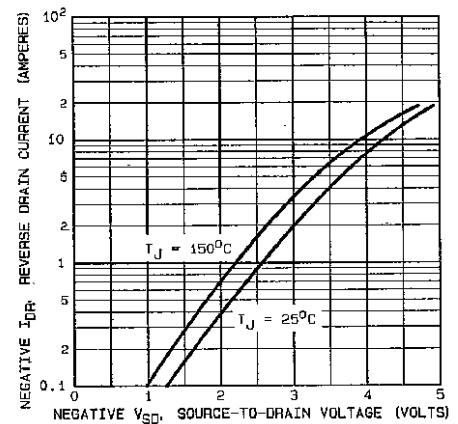


Fig. 6 - Typical Source-Drain Diode Forward Voltage

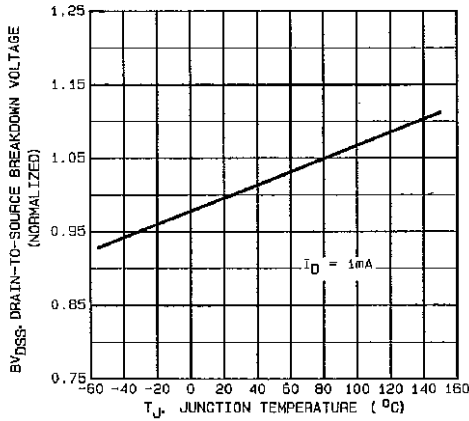


Fig. 7 - Breakdown Voltage vs. Temperature

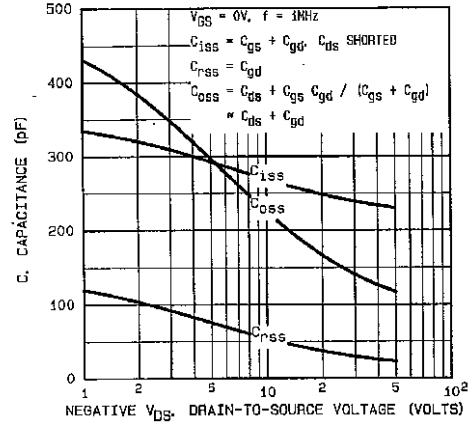


Fig. 9 - Typical Capacitance vs. Drain-to-Source Voltage

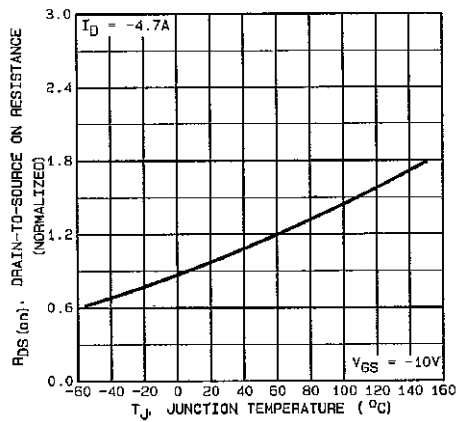


Fig. 8 - Normalized On-Resistance vs. Temperature

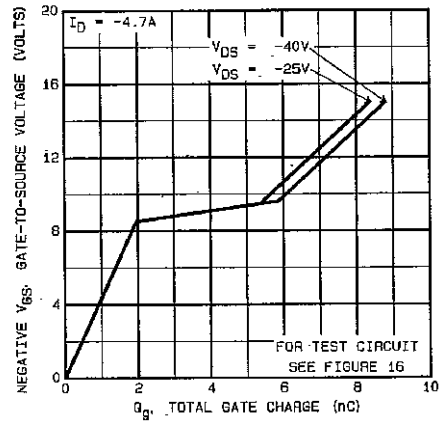


Fig. 10 - Typical Gate Charge vs. Gate-to-Source Voltage

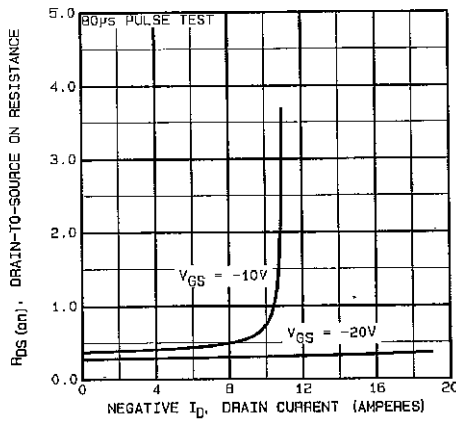


Fig. 11 - Typical On-Resistance vs. Drain Current

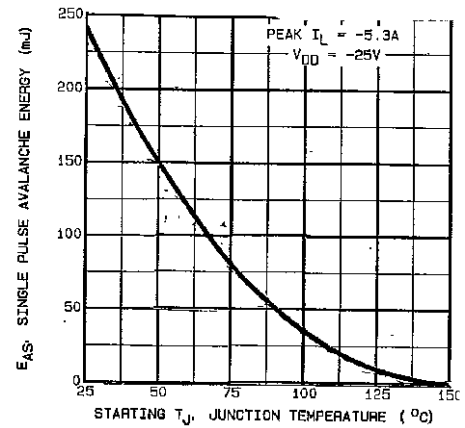


Fig. 13a - Maximum Avalanche vs. Starting Junction Temperature

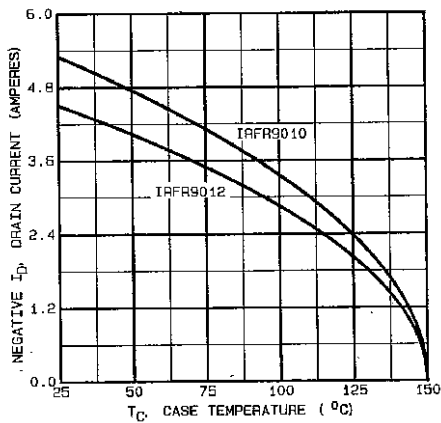


Fig. 12 - Maximum Drain Current vs. Case Temperature

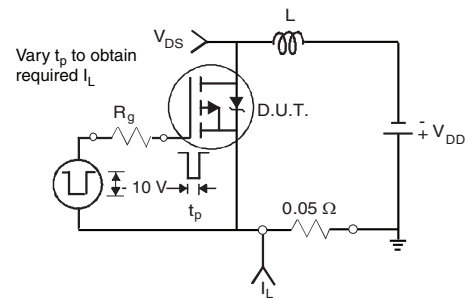


Fig. 13b - Unclamped Inductive Test Circuit

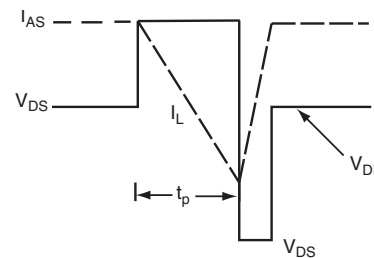


Fig. 13c - Unclamped Inductive Waveforms

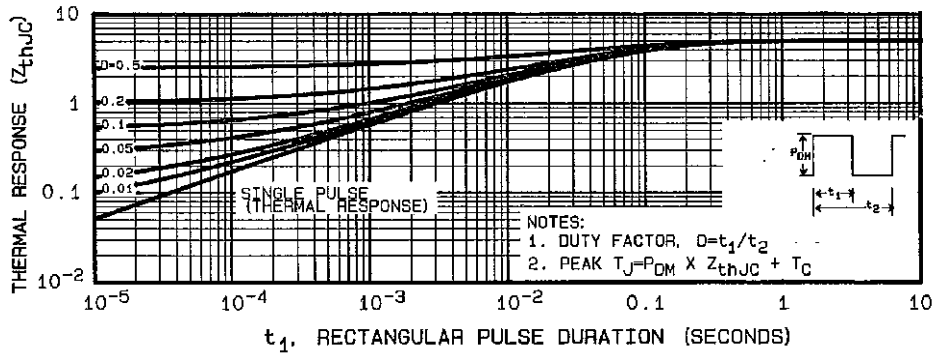


Fig. 14 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

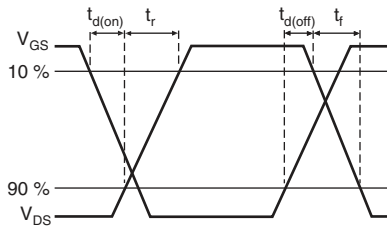


Fig. 15a - Switching Time Waveforms

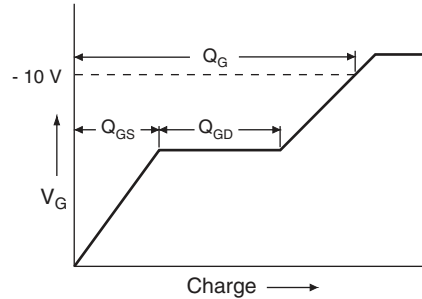


Fig. 16a - Basic Gate Charge Waveform

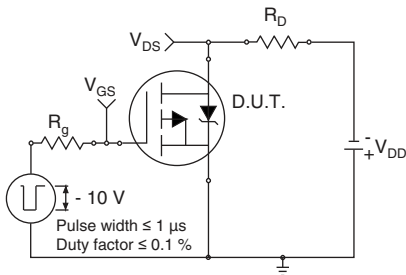


Fig. 15b - Switching Time Test Circuit

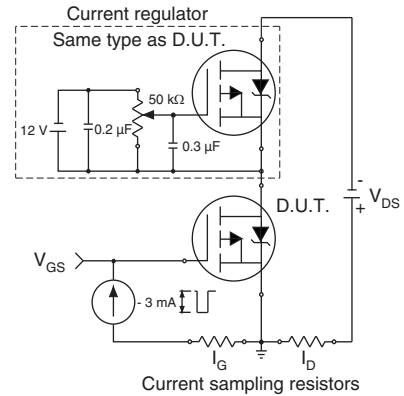
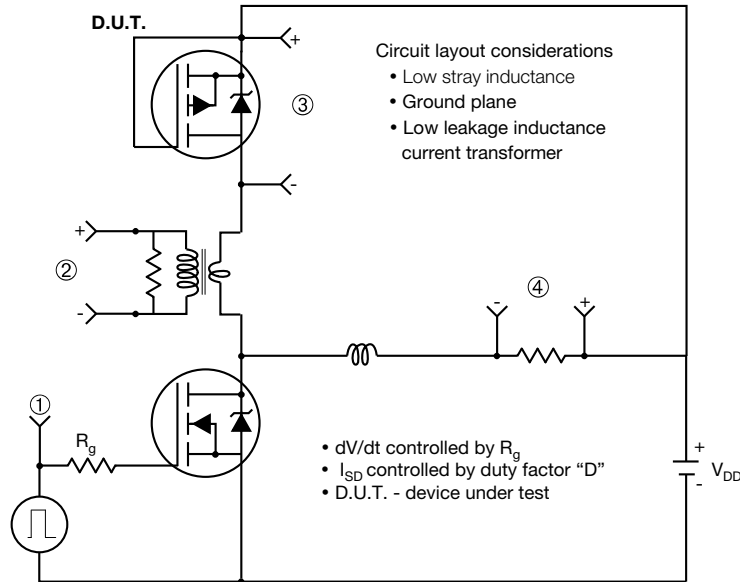


Fig. 16b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note
 • Compliment N-Channel of D.U.T. for driver



Fig. 17 - For P-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91378.



TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

MILLIMETERS		
DIM.	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ1	0°	15°
θ2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E19-0649-Rev. Q, 16-Dec-2019
 DWG: 5347

TO-251AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
theta1	0'	15'	0'	15'
theta2	25'	35'	25'	35'

ECN: S-82111-Rev. A, 15-Sep-08
DWG: 5968

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension are shown in inches and millimeters.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
5. Lead dimension uncontrolled in L3.
6. Dimension b1, b3 and c1 apply to base metal only.
7. Outline conforms to JEDEC outline TO-251AA.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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