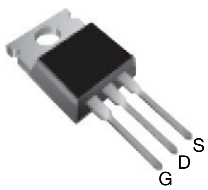
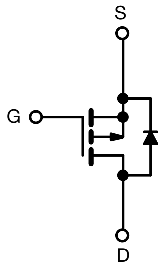
Power MOSFET

TO-220AB





P-Channel MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	-50	
$R_{DS(on)}$ (Ω)	V_{GS} = -10 V	0.14
Q_g max. (nC)	39	
Q_{gs} (nC)	10	
Q_{gd} (nC)	15	
Configuration	Single	

FEATURES

- P-channel versatility
- Compact plastic package
- Fast switching
- Low drive current
- Ease of paralleling
- Excellent temperature stability
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb Available

RoHS* Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

The power MOSFET technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the power MOSFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The p-channel power MOSFET's are designed for application which require the convenience of reverse polarity operation. They retain all of the features of the more common n-channel Power MOSFET's such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability.

P-channel power MOSFETs are intended for use in power stages where complementary symmetry with n-channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF9Z30PbF
Lead (Pb)-free and halogen-free	IRF9Z30PbF-BE3

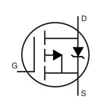
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	-50	V
Gate-source voltage			V_{GS}	± 20	V
Continuous drain current	V_{GS} at -10 V	T_C = 25 °C	I_D	-18	A
		T_C = 100 °C		-11	
Pulsed drain current [a]			I_{DM}	-60	
Linear derating factor				0.59	W/°C
Inductive current, clamped	L = 100 μH		I_{LM}	-60	A
Unclamped inductive current (avalanche current)			I_L	-3.1	A
Maximum power dissipation	T_C = 25 °C		P_D	74	W
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [c]	For 10 s			300	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14)
b. V_{DD} = -25 V, starting T_J = 25 °C, L = 100 μH, R_g = 25 Ω
c. 0.063" (1.6 mm) from case

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	R_{thJA}	-	80	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	1.7	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 μA	-50	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 μA	-2.0	-	-4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 500	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = max. rating, V_{GS} = 0 V	-	-	-250	μA
		V_{DS} = max. rating x 0.8, V_{GS} = 0 V, T_J =125 °C	-	-	-1000	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = -10 V; I_D = -9.3 A [b]	-	0.093	0.14	Ω
Forward transconductance	g_{fs}	V_{DS} = 2 x V_{GS}, I_{DS} = -9 A [b]	3.1	4.7	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz, see fig. 9	-	900	-	pF
Output capacitance	C_{oss}		-	570	-	
Reverse transfer capacitance	C_{rss}		-	140	-	
Total gate charge	Q_g	V_{GS} = -10 V; I_D = -18 A, V_{DS} = -0.8 max. rating. see fig. 17	-	26	39	nC
Gate-source charge	Q_{gs}		-	6.9	10	
Gate-drain charge	Q_{gd}		-	9.7	15	
Turn-on delay time	$t_{d(on)}$	V_{DD} = -25 V, I_D = -18 A, R_g = 13 Ω, R_D = 1.3 Ω, see fig. 16 (MOSFET switching times are essentially independent of operating temperature)	-	12	18	ns
Rise time	t_r		-	110	170	
Turn-off delay time	$t_{d(off)}$		-	21	32	
Fall time	t_f		-	64	96	
Gate input resistance	R_g	f = 1 MHz, open drain	0.7	-	3.9	Ω
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	-18	A
Pulsed diode forward current [a]	I_{SM}		-	-	-60	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = -18 A, V_{GS} = 0 V [b]	-	-	-6.3	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = -18 A, dI/dt = 100 A/μs [b]	54	120	250	ns
Body diode reverse recovery charge	Q_{rr}		0.20	0.47	1.1	μC

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14)

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

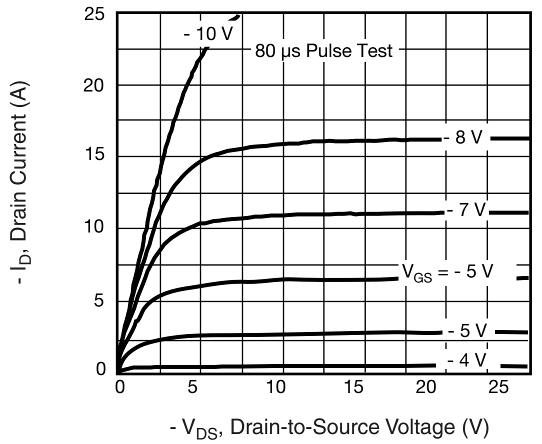


Fig. 1 - Typical Output Characteristics

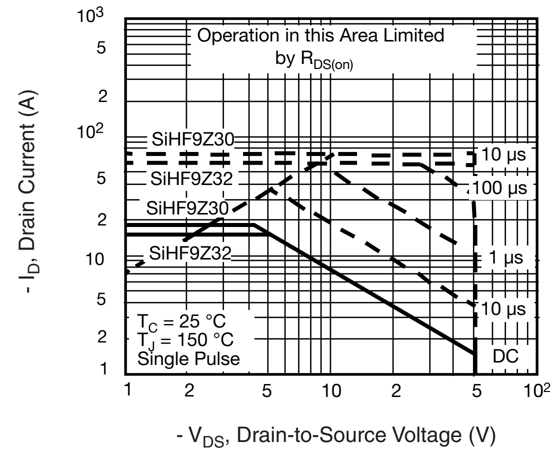


Fig. 4 - Maximum Safe Operating Area

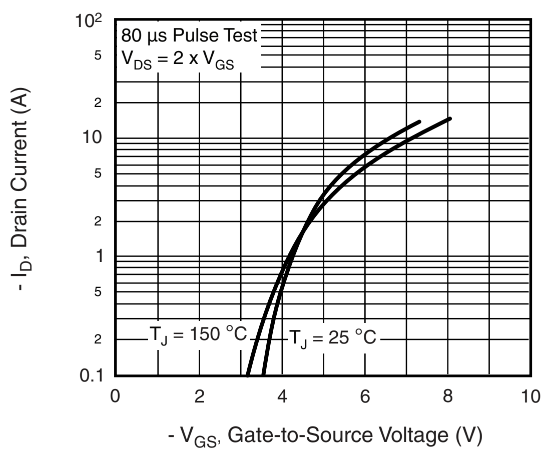


Fig. 2 - Typical Transfer Characteristics

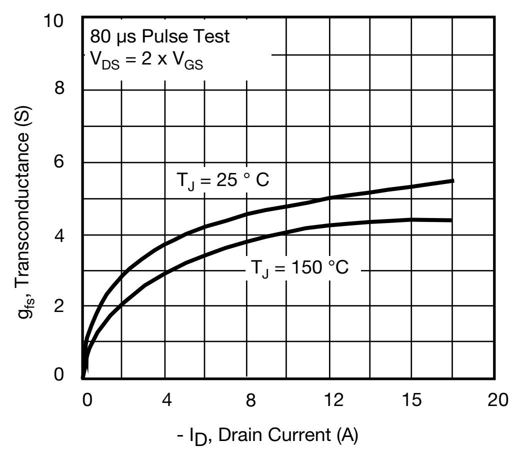


Fig. 5 - Typical Transconductance vs. Drain Current

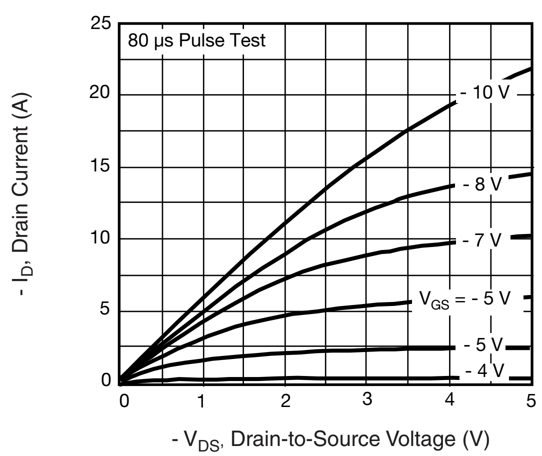


Fig. 3 - Typical Saturation Characteristics

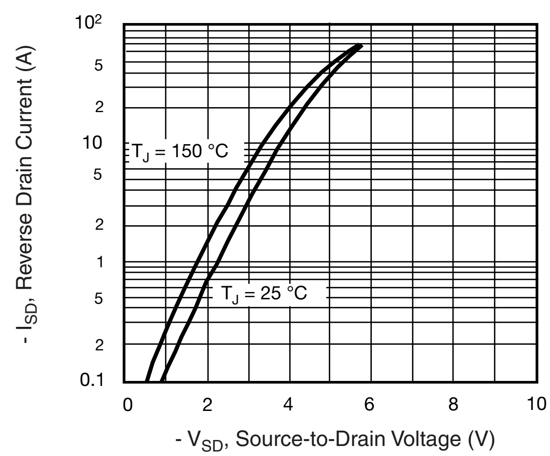


Fig. 6 - Typical Source-Drain Diode Forward Voltage

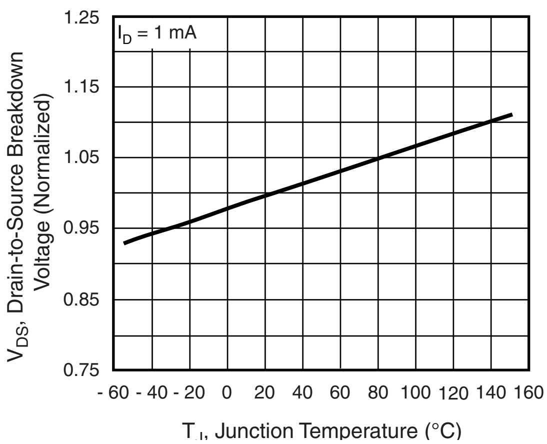


Fig. 7 - Breakdown Voltage vs. Temperature

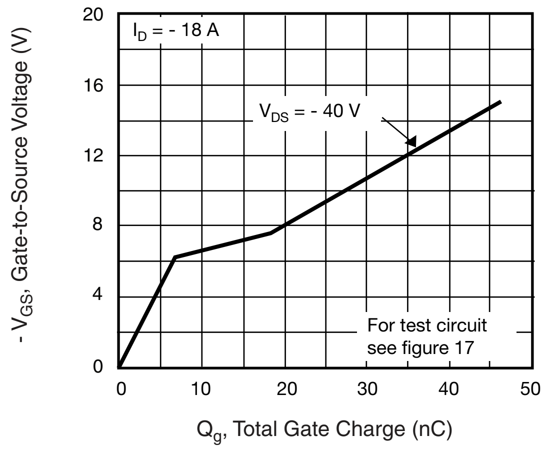


Fig. 10 - Typical Gate Charge vs. Gate-to-Source Voltage

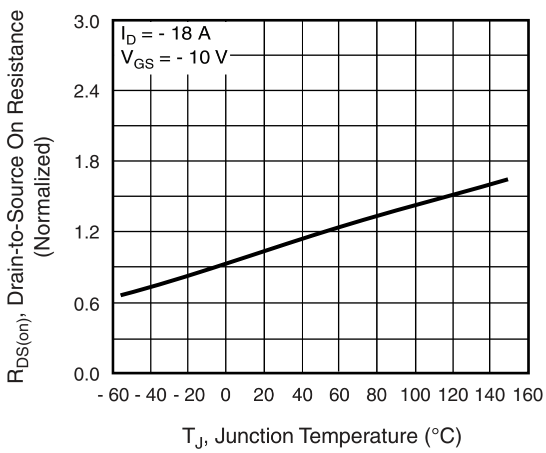


Fig. 8 - Normalized On-Resistance vs. Temperature

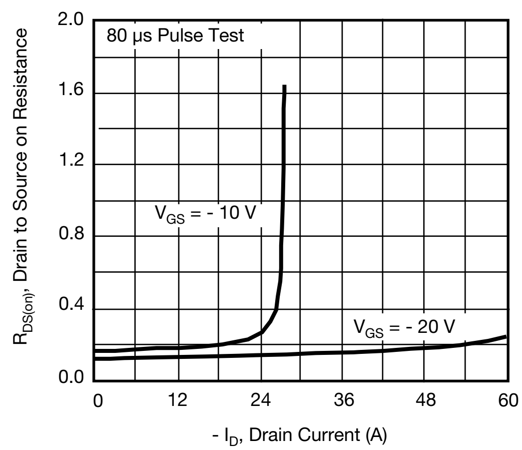


Fig. 11 - Typical On-Resistance vs. Drain Current

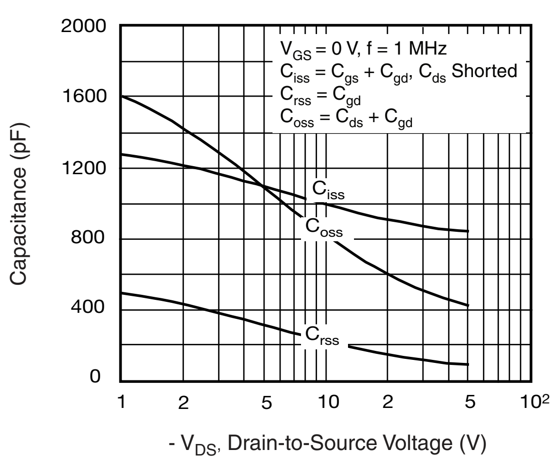


Fig. 9 - Typical Capacitance vs. Drain-to-Source Voltage

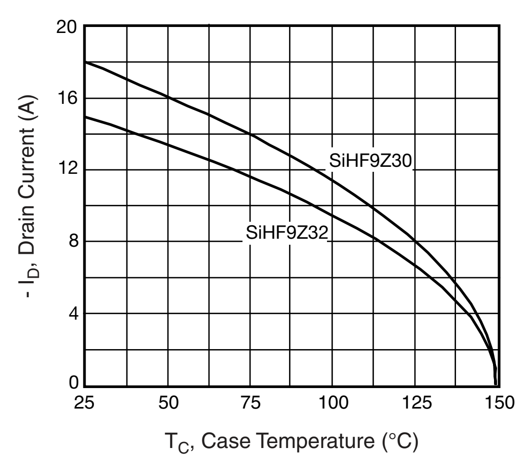


Fig. 12 - Maximum Drain Current vs. Case Temperature

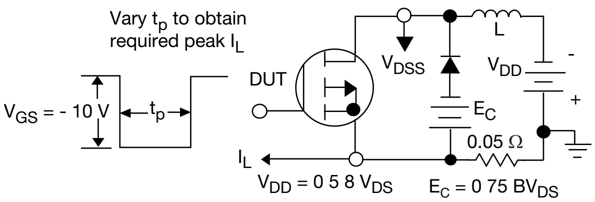


Fig. 13a - Unclamped Inductive Test Circuit

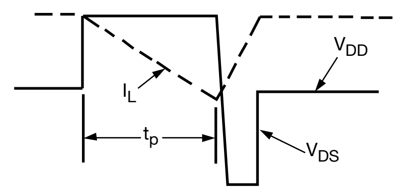


Fig. 13b - Unclamped Inductive Load Test Waveforms

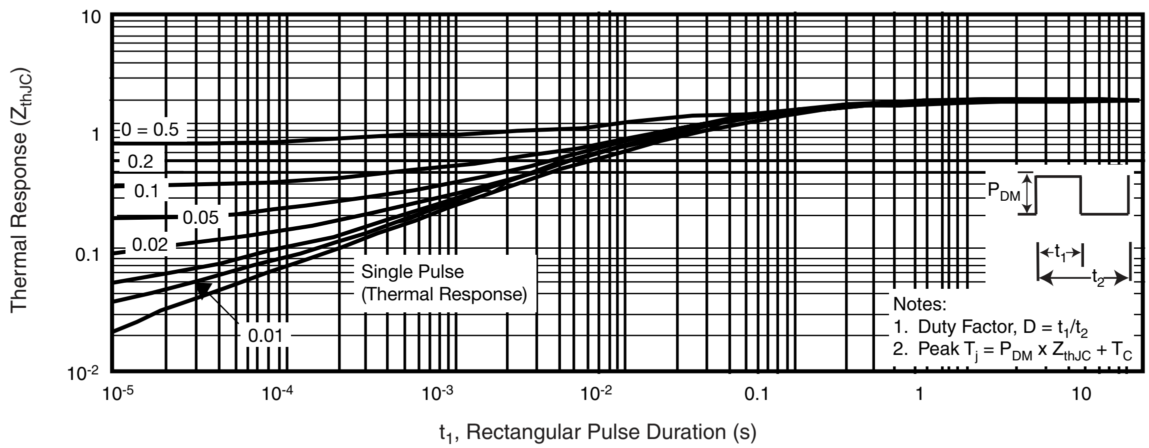


Fig. 14 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

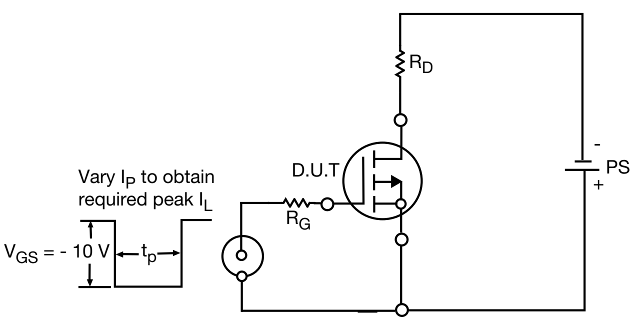


Fig. 13 - Switching Time Test Circuit

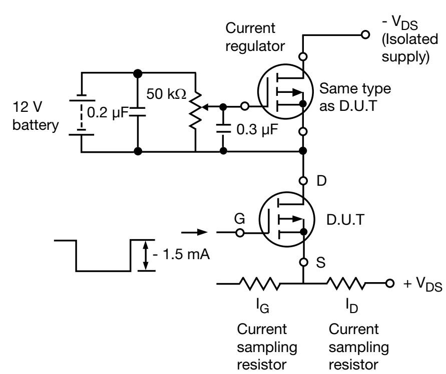


Fig. 14 - Gate Charge Test Circuit

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