

Vishay Siliconix

E Series Power MOSFET

DESCRIPTION

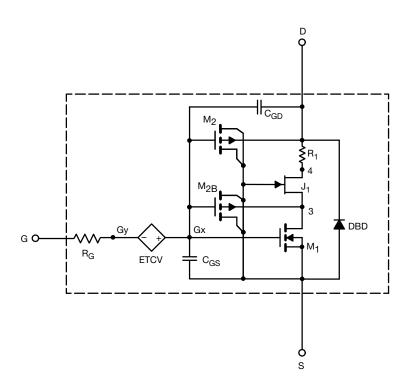
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to 150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- · Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- · Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPICE Device Model SiHA25N50E

Vishay Siliconix

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	3	-	V
Drain-Source On-State Resistance a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}$	0.155	0.125	Ω
Forward Transconductance a	g _{fs}	$V_{DS} = 30 \text{ V}, I_D = 12 \text{ A}$	8.8	6.6	S
Diode Forward Voltage	V _{SD}	$I_S = 16.5 \text{ A}, V_{GS} = 0 \text{ V}$	0.90	-	V
Dynamic ^b					
Input Capacitance	C _{iss}	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz	2010	1980	pF
Output Capacitance	C _{oss}		170	105	
Reverse Transfer Capacitance	C _{rss}		17	8	
Total Gate Charge	Qg		57	57	
Gate-Source Charge	Q _{gs}	$V_{DS} = 400 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 11 \text{ A}$	14	14	nC
Gate-Drain Charge	Q_{gd}		25	25	

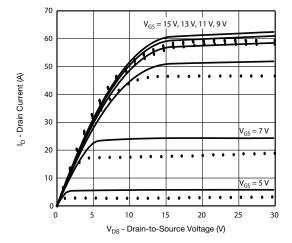
Notes

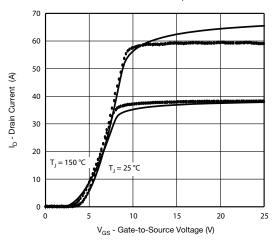
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

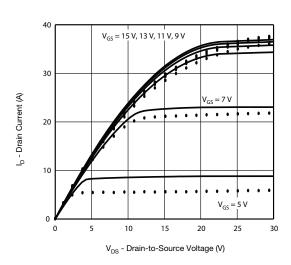
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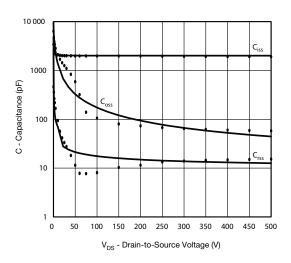
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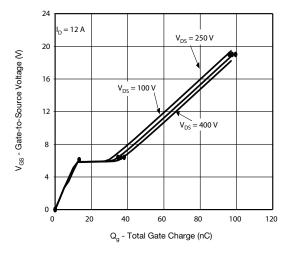
COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25$ °C, unless otherwise noted)

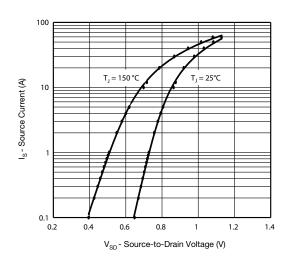












Note

Dots and squares represent measured data.
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