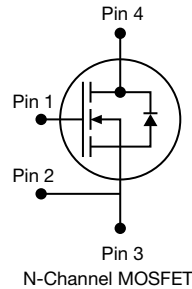
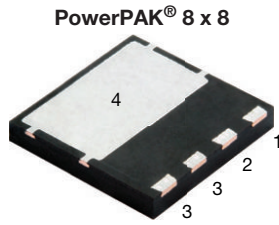


## E Series Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V) at $T_J$ max.	700
$R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V   0.130
$Q_g$ max. (nC)	116
$Q_{gs}$ (nC)	19
$Q_{gd}$ (nC)	33
Configuration	Single



### FEATURES

- Completely lead (Pb)-free device
- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Kelvin connection for reduced gate noise
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

ORDERING INFORMATION	
Package	PowerPAK 8 x 8
Lead (Pb)-free and Halogen-free	SiHH24N65E-T1-GE3


ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		$V_{DS}$	650	V	
Gate-Source Voltage		$V_{GS}$	$\pm 30$		
Continuous Drain Current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$I_D$	$T_C = 25$ °C	23	A
			$T_C = 100$ °C	15	
Pulsed Drain Current <sup>a</sup>		$I_{DM}$	58		
Linear Derating Factor			1.61	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>		$E_{AS}$	353	mJ	
Maximum Power Dissipation		$P_D$	202	W	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +150	°C	
Drain-Source Voltage Slope	$T_J = 125$ °C	dV/dt	70	V/ns	
Reverse Diode dV/dt <sup>c</sup>			16		

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 140$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 5$  A.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C.



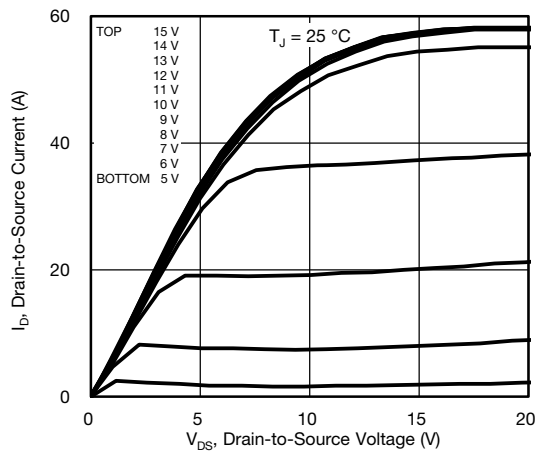
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R <sub>thJA</sub>	38	50	°C/W
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	0.48	0.62	

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		650	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.75	-	V/°C
Gate-Source Threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
		V <sub>GS</sub> = ± 30 V		-	-	± 1	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 650 V, V <sub>GS</sub> = 0 V		-	-	1	μA
		V <sub>DS</sub> = 520 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	25	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 12 A	-	0.130	0.150	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 12 A		-	8.2	-	S
<b>Dynamic</b>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1 MHz		-	2814	-	pF
Output Capacitance	C <sub>oss</sub>			-	121	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	5	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	C <sub>o(er)</sub>			-	88	-	
Effective Output Capacitance, Time Related <sup>b</sup>	C <sub>o(tr)</sub>	V <sub>DS</sub> = 0 V to 520 V, V <sub>GS</sub> = 0 V		-	365	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 12 A, V <sub>DS</sub> = 520 V	-	77	116	nC
Gate-Source Charge	Q <sub>gs</sub>			-	19	-	
Gate-Drain Charge	Q <sub>gd</sub>			-	33	-	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 520 V, I <sub>D</sub> = 12 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω		-	29	58	ns
Rise Time	t <sub>r</sub>			-	59	71	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	78	117	
Fall Time	t <sub>f</sub>			-	46	92	
Gate Input Resistance	R <sub>g</sub>	f = 1 MHz, open drain		0.27	0.55	1.10	Ω
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	23	A
Pulsed Diode Forward Current	I <sub>SM</sub>			-	-	58	
Diode Forward Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 12 A, V <sub>GS</sub> = 0 V		-	0.9	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 12 A, dI/dt = 100 A/μs, V <sub>R</sub> = 25 V		-	436	872	ns
Reverse Recovery Charge	Q <sub>rr</sub>			-	7.4	14.8	μC
Reverse Recovery Current	I <sub>RRM</sub>			-	29	-	A

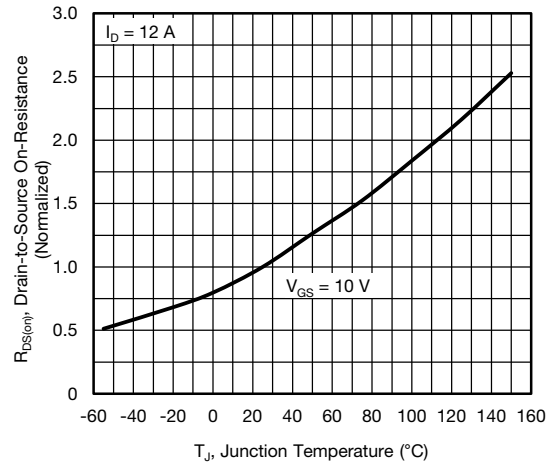
**Notes**

- a. C<sub>oss(er)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DS</sub>.
- b. C<sub>oss(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DS</sub>.

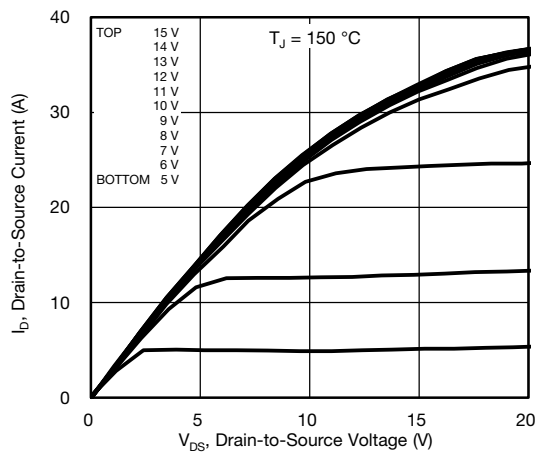
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



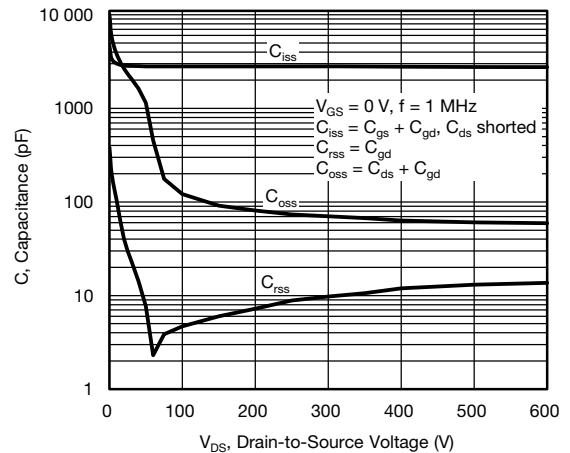
**Fig. 1 - Typical Output Characteristics**



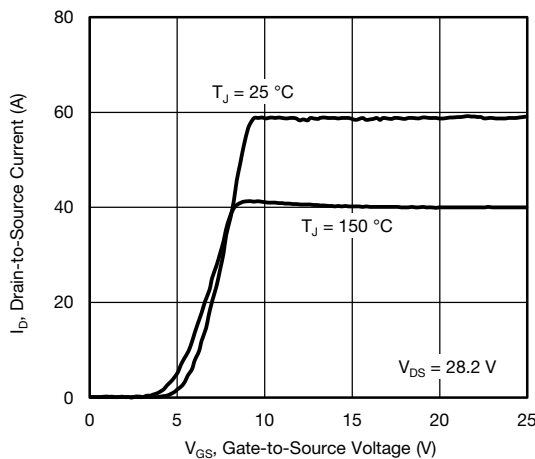
**Fig. 4 - Normalized On-Resistance vs. Temperature**



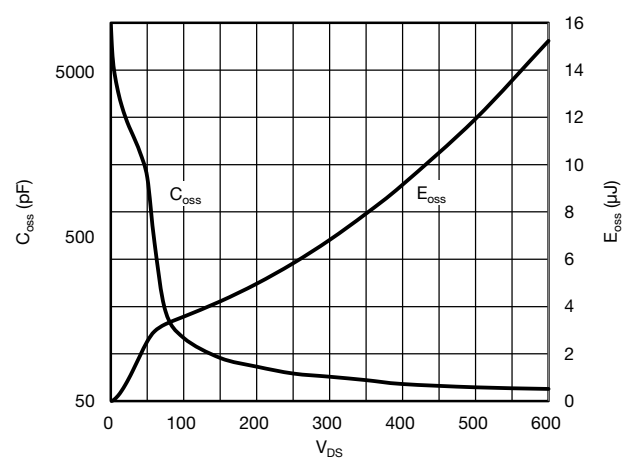
**Fig. 2 - Typical Output Characteristics**



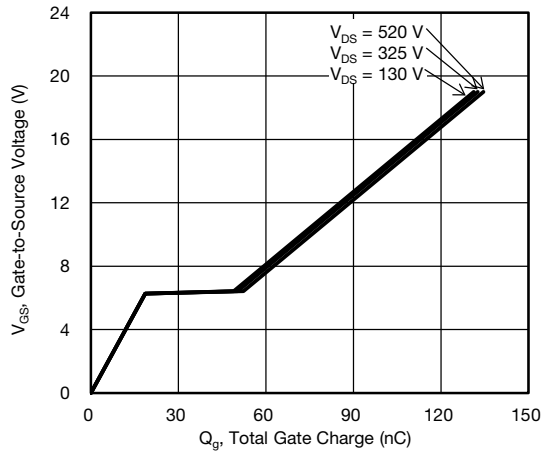
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



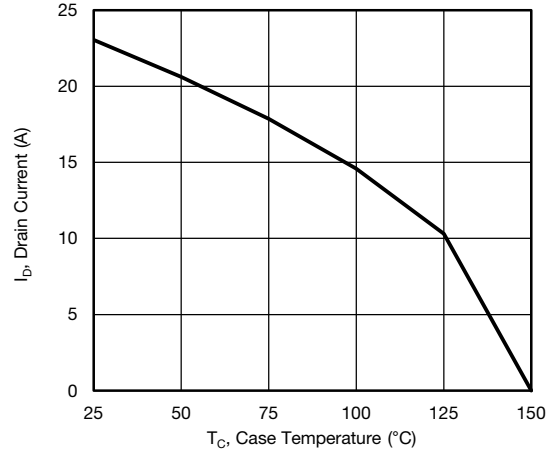
**Fig. 3 - Typical Transfer Characteristics**



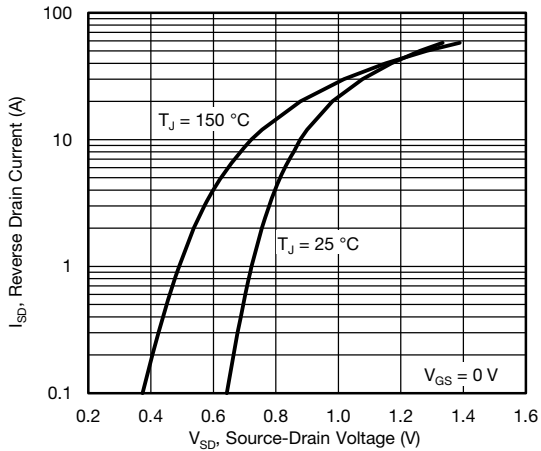
**Fig. 6 - Coss and Eoss vs. VDS**



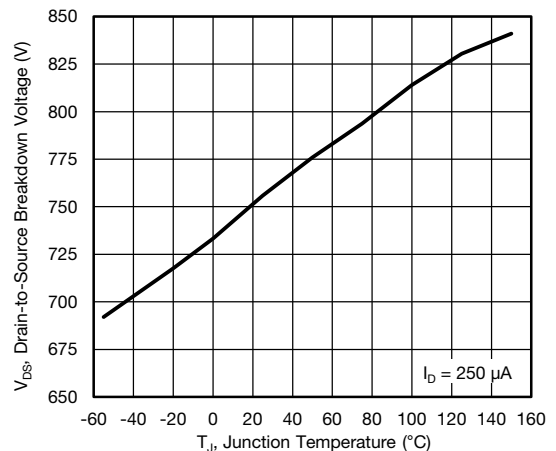
**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**



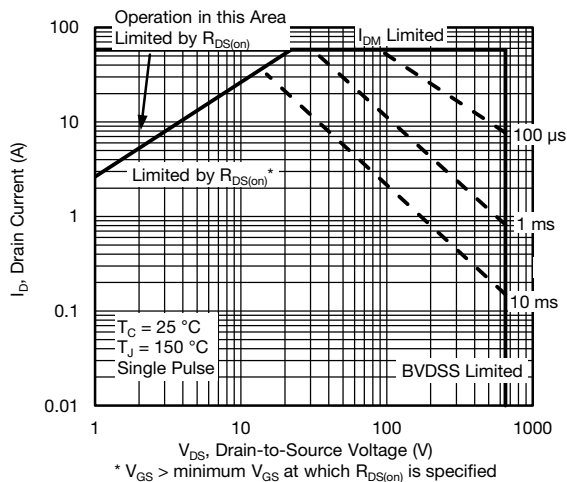
**Fig. 10 - Maximum Drain Current vs. Case Temperature**



**Fig. 8 - Typical Source-Drain Diode Forward Voltage**



**Fig. 11 - Temperature vs. Drain-to-Source Voltage**



**Fig. 9 - Maximum Safe Operating Area**

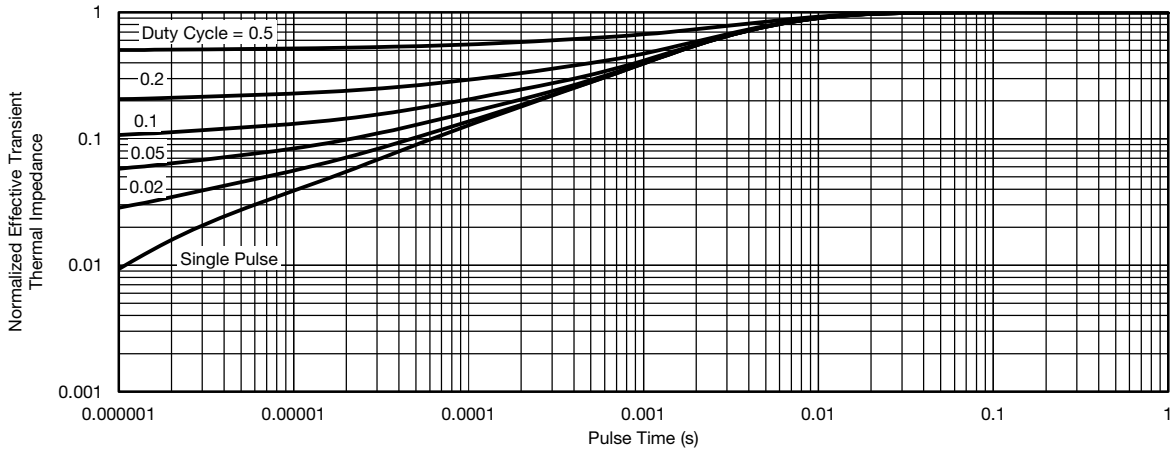


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

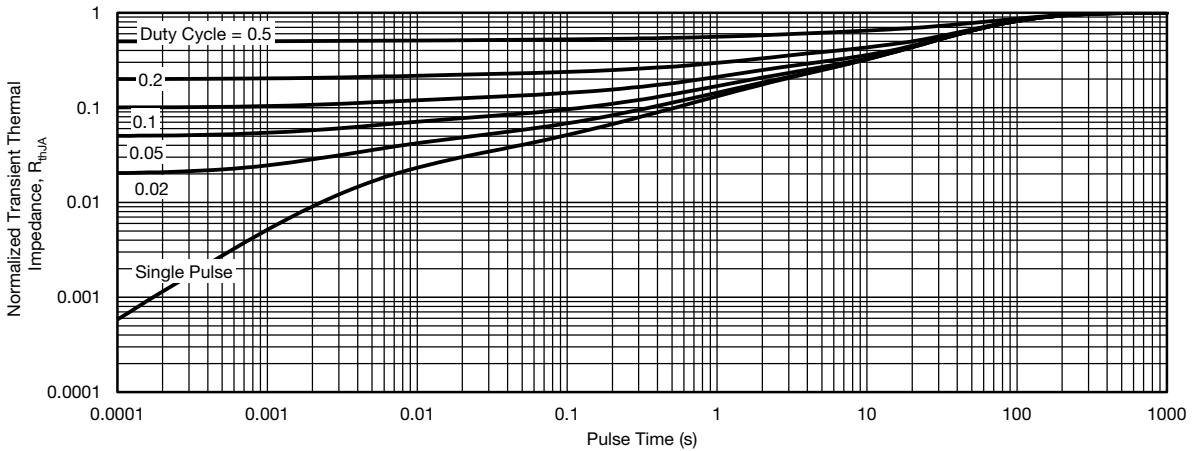


Fig. 13 - Normalized Thermal Transient Impedance, Junction-to-Ambient

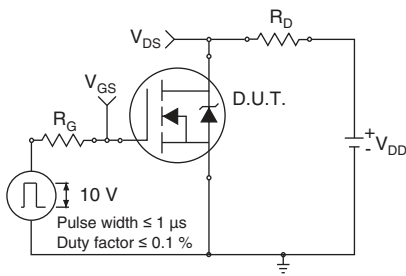


Fig. 14 - Switching Time Test Circuit

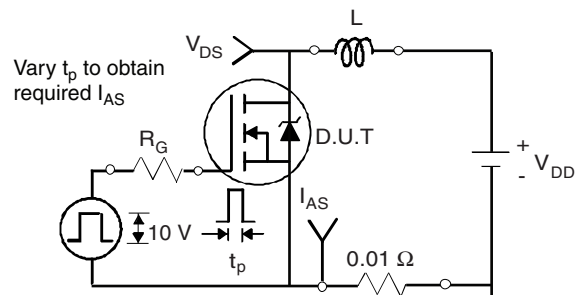


Fig. 16 - Unclamped Inductive Test Circuit

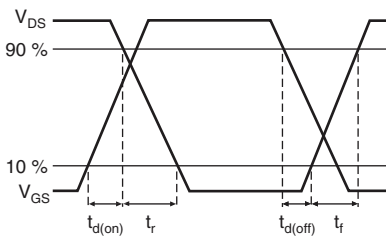


Fig. 15 - Switching Time Waveforms

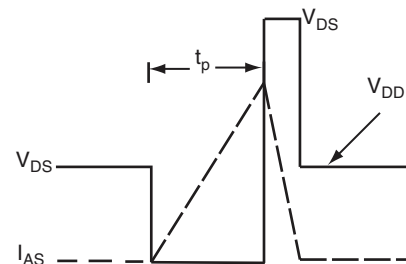


Fig. 17 - Unclamped Inductive Waveforms



Fig. 18 - Basic Gate Charge Waveform

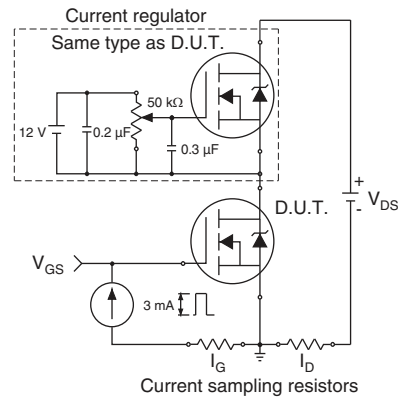
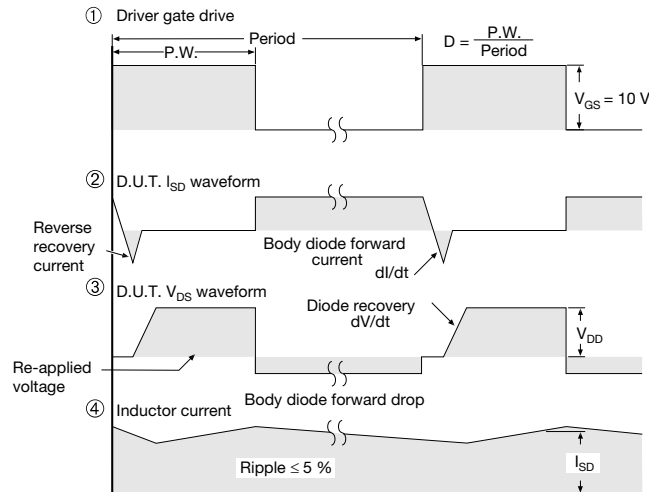
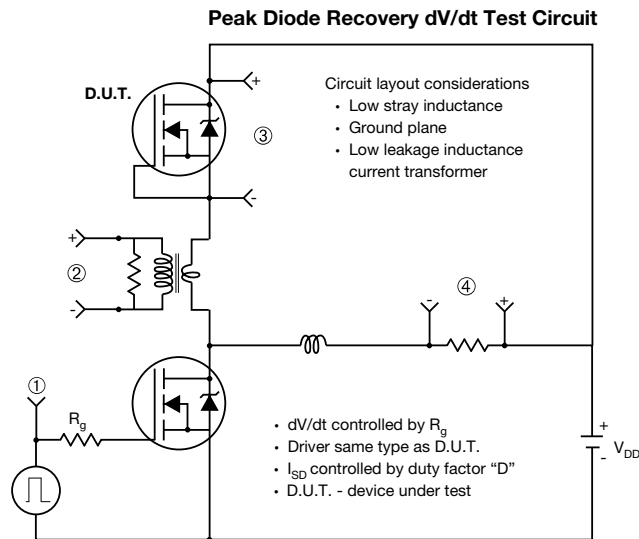


Fig. 19 - Gate Charge Test Circuit



Note  
a.  $V_{GS} = 5V$  for logic level devices

Fig. 20 - For N-Channel

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## PowerPAK® 8 x 8 Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.95	1.00	1.05	0.037	0.039	0.041
A1	0.00	-	0.05	0.000	-	0.002
A2	020 ref.			0.008 ref.		
b	0.95	1.00	1.05	0.037	0.039	0.041
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	7.10	7.20	7.30	0.280	0.283	0.287
D3	0.40 BSC			0.016 BSC		
e	2.00 BSC			0.079 BSC		
E	7.90	8.00	8.10	0.311	0.315	0.319
E2	4.30	4.35	4.40	0.169	0.171	0.173
E3	0.40 BSC			0.016 BSC		
K	2.75 BSC			0.108 BSC		
L	0.45	0.50	0.55	0.018	0.020	0.022
N <sup>(3)</sup>	8			8		

**Notes**

- (1) Use millimeters as the primary measurement
- (2) Dimensioning and tolerances conform to ASME Y14.5 M - 1994
- (3) N is the number of terminals
- (4) The pin 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- (5) Exact shape and size of this feature is optional

ECN: E20-0518-Rev. B, 28-Sep-2020  
 DWG: 6041



# Recommended Minimum PADs for PowerPAK<sup>®</sup> 8 mm x 8 mm



Dimensions in millimeters





## Disclaimer

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