Vishay Siliconix

# **E Series Power MOSFET with Fast Body Diode**

#### **DESCRIPTION**

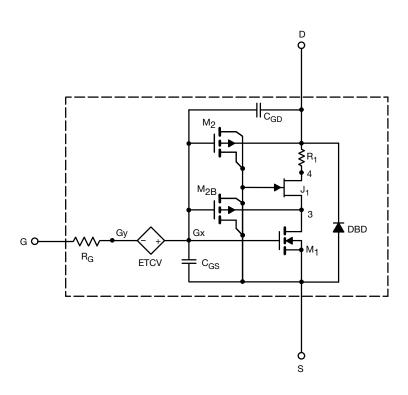
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{\rm gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### **CHARACTERISTICS**

- N-channel vertical DMOS
- Macro model (Sub-circuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- · Model the gate charge

#### SUBCIRCUIT MODEL SCHEMATIC



#### Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



# **SPICE Device Model SiHH14N60EF**

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SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	3	-	V
Drain-Source On-State Resistance a	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7 A	0.231	0.231	Ω
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 7 A	6.7	5.1	S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 7 A, V <sub>GS</sub> = 0 V	0.90	0.90	V
Dynamic <sup>b</sup>					
Input Capacitance	C <sub>iss</sub>		1520	1449	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	118	78	рF
Reverse Transfer Capacitance	C <sub>rss</sub>		8	5	
Total Gate Charge	Qg		41	42	
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 480 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 7 \text{ A}$	9	9	nC
Gate-Drain Charge	Q <sub>ad</sub>		17	17	

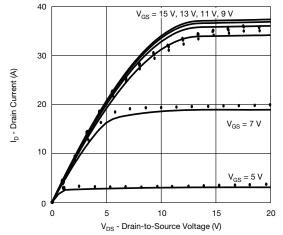
#### Notes

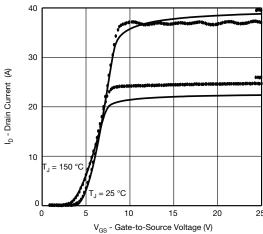
- a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

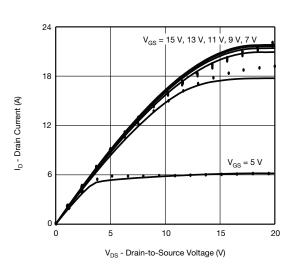
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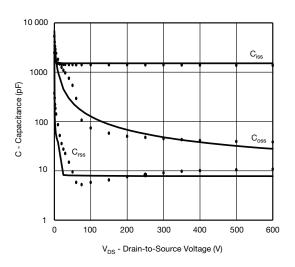
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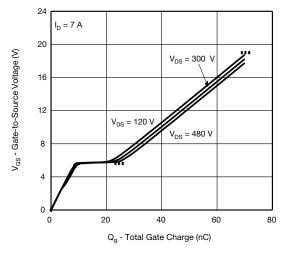
## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25~^{\circ}\text{C}$ , unless otherwise noted)

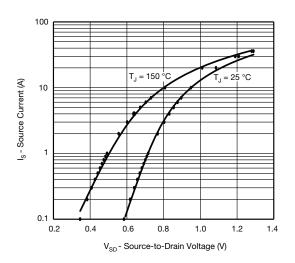












#### Note

Dots and squares represent measured data.
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