

EF Series Power MOSFET With Fast Body Diode



N-Channel MOSFET

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V	0.061
Q_g max. (nC)	189	
Q_{gs} (nC)	26	
Q_{gd} (nC)	55	
Configuration	Single	

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free and halogen-free	SiHP38N60EF-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	600	V
Gate-source voltage	V_{GS}	± 30	V
Continuous drain current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	40
		$T_C = 100$ °C	25
Pulsed drain current ^a	I_{DM}	111	A
Linear derating factor		2.5	W/°C
Single pulse avalanche energy ^b	E_{AS}	508	mJ
Maximum power dissipation	P_D	313	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Drain-source voltage slope	dv/dt	$T_J = 125$ °C	100
Reverse diode dv/dt ^d		50	
Soldering recommendations (peak temperature) ^c	For 10 s	260	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 6.0$ A
- 1.6 mm from case
- $I_{SD} = 23.5$ A, $di/dt = 250$ A/ μ s, starting $T_J = 25$ °C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	0.4	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	600	-	-	V	
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 10\text{ mA}$	-	0.72	-	V/ $^\circ\text{C}$	
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	-	4	V	
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA	
		$V_{GS} = \pm 30\text{ V}$	-	-	± 1	μA	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA	
		$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	2	mA	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 23.5\text{ A}$	-	0.061	0.070	Ω	
Forward transconductance ^a	g_{fs}	$V_{DS} = 30\text{ V}$, $I_D = 23.5\text{ A}$	-	13	-	S	
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$	-	3576	-	pF	
Output capacitance	C_{oss}		-	167	-		
Reverse transfer capacitance	C_{rss}		-	5	-		
Effective output capacitance, energy related ^a	$C_{o(er)}$		$V_{DS} = 0\text{ V to } 480\text{ V}$, $V_{GS} = 0\text{ V}$	-	104		-
Effective output capacitance, time related ^b	$C_{o(tr)}$			-	535		-
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 23.5\text{ A}$, $V_{DS} = 480\text{ V}$	-	126	189	nC	
Gate-source charge	Q_{gs}		-	26	-		
Gate-drain charge	Q_{gd}		-	55	-		
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 480\text{ V}$, $I_D = 23.5\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 9.1\text{ }\Omega$	-	35	70	ns	
Rise time	t_r		-	63	126		
Turn-off delay time	$t_{d(off)}$		-	143	286		
Fall time	t_f		-	67	134		
Gate input resistance	R_g		$f = 1\text{ MHz}$, open drain	0.2	0.5		1.0
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	40	A	
Pulsed diode forward current	I_{SM}		-	-	111		
Diode forward voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 23.5\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1.2	V	
Reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = I_S = 23.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_R = 400\text{ V}$	-	160	320	ns	
Reverse recovery charge	Q_{rr}		-	1.2	2.4	μC	
Reverse recovery current	I_{RRM}		-	14.3	-	A	

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

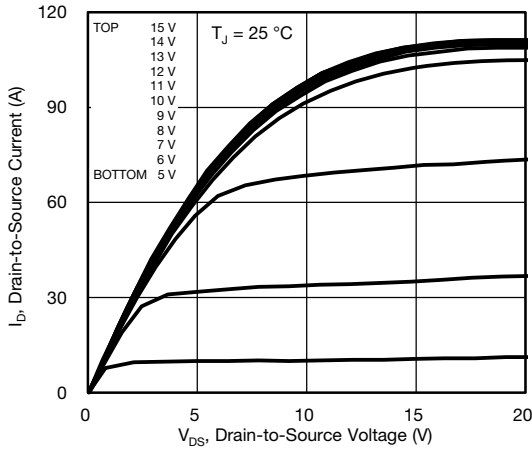


Fig. 1 - Typical Output Characteristics

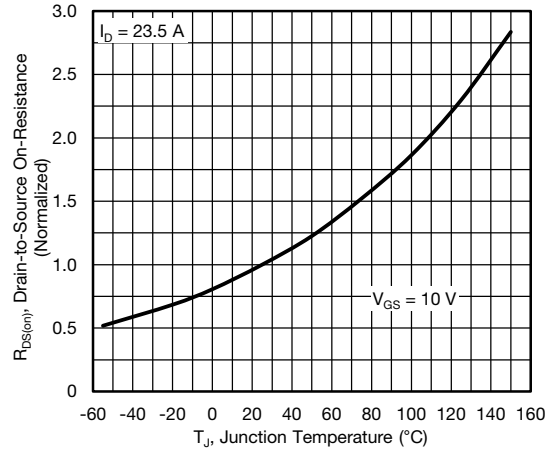


Fig. 4 - Normalized On-Resistance vs. Temperature

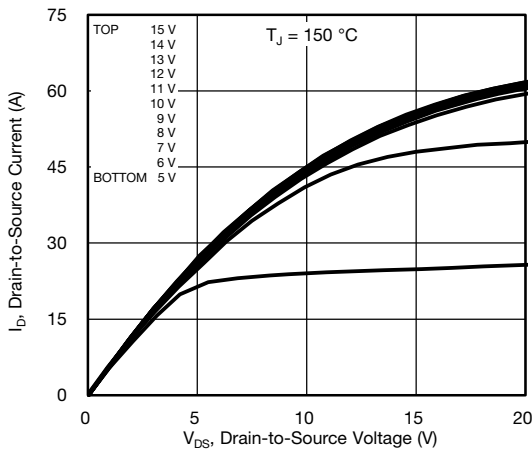


Fig. 2 - Typical Output Characteristics

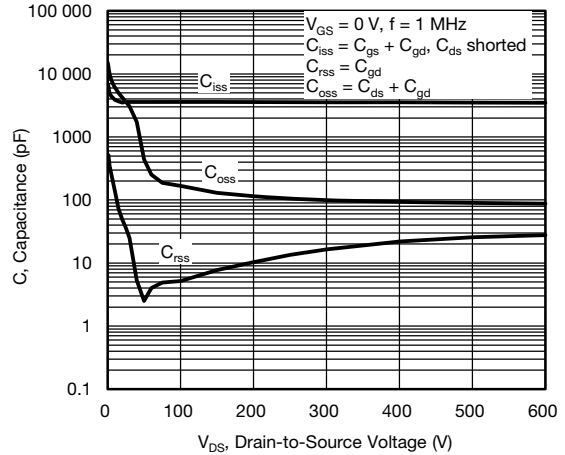


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

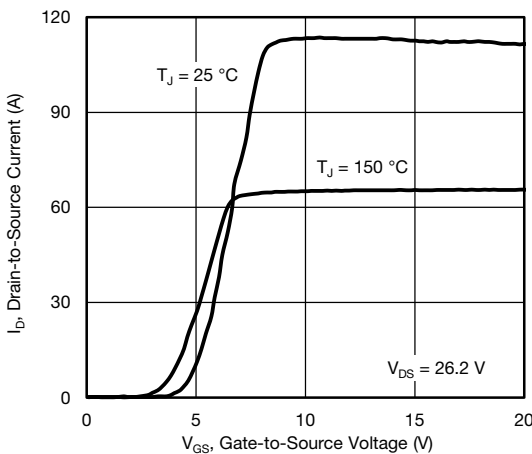


Fig. 3 - Typical Transfer Characteristics

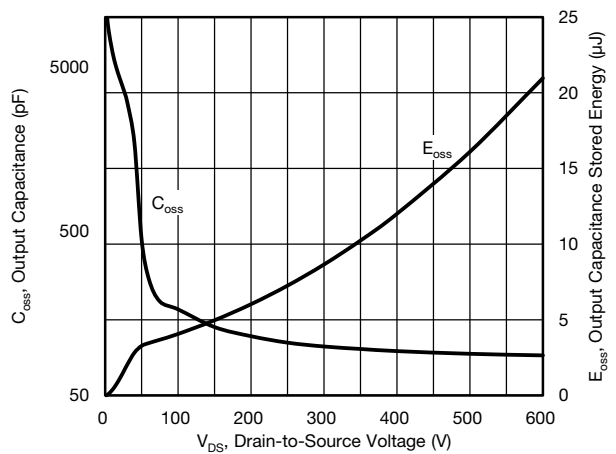


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

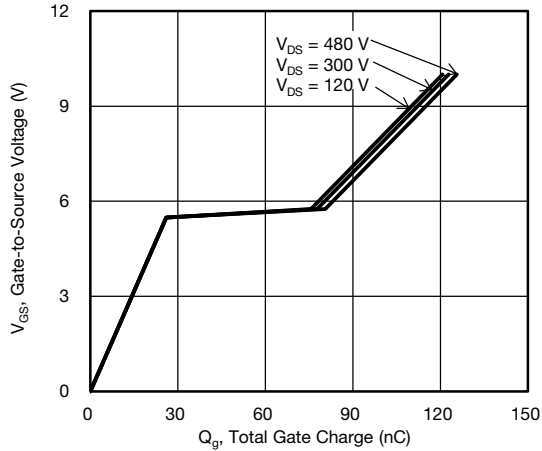


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

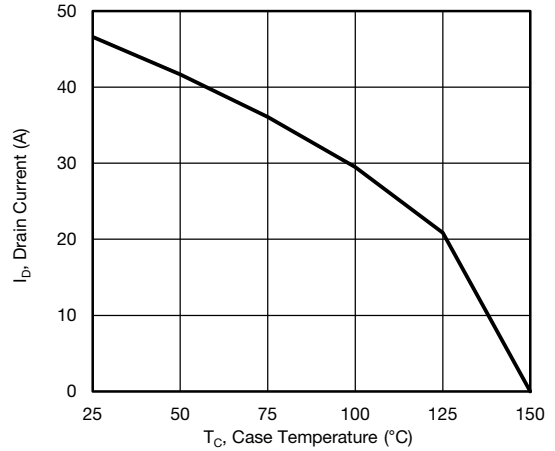


Fig. 10 - Maximum Drain Current vs. Case Temperature

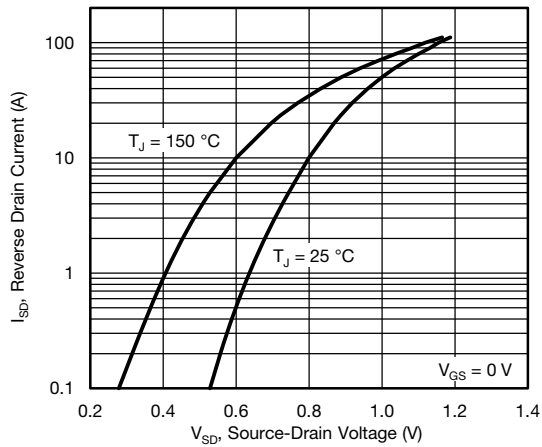


Fig. 8 - Typical Source-Drain Diode Forward Voltage

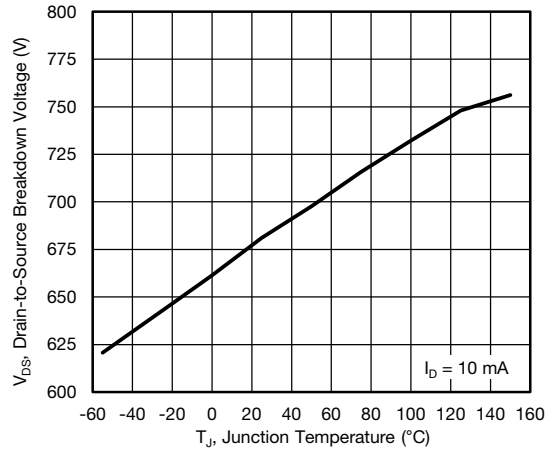


Fig. 11 - Temperature vs. Drain-to-Source Voltage

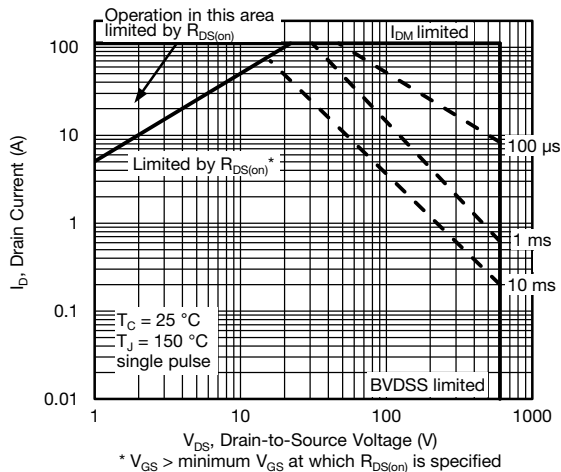


Fig. 9 - Maximum Safe Operating Area

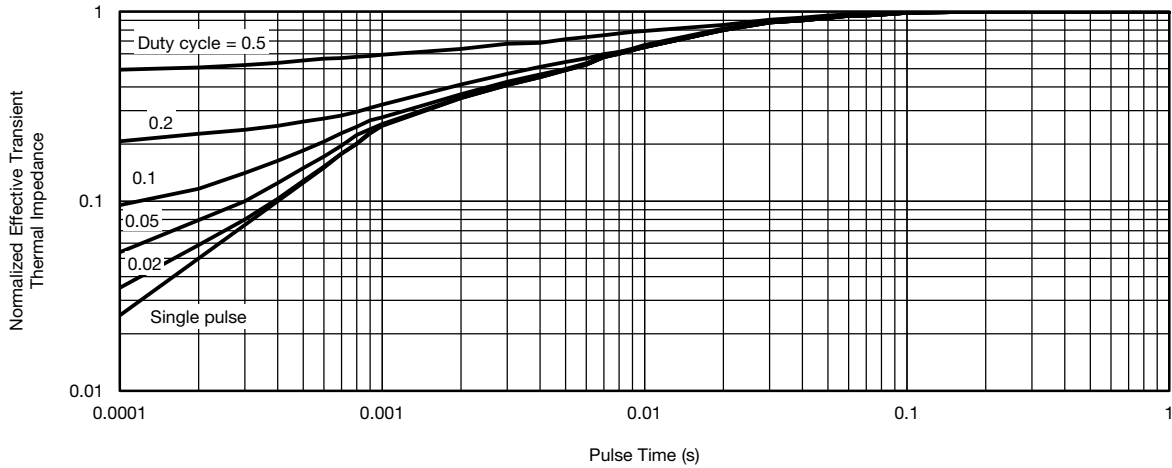


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

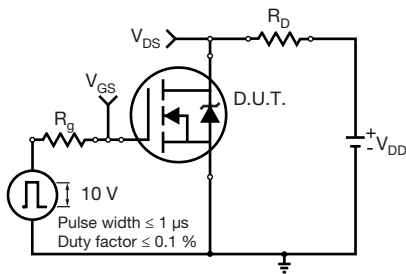


Fig. 13 - Switching Time Test Circuit



Fig. 16 - Unclamped Inductive Waveforms

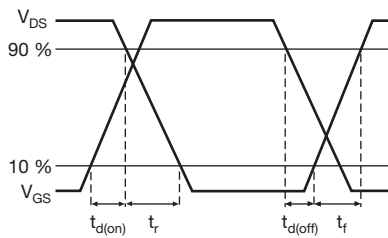


Fig. 14 - Switching Time Waveforms

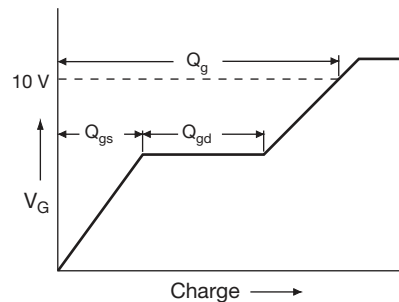


Fig. 17 - Basic Gate Charge Waveform

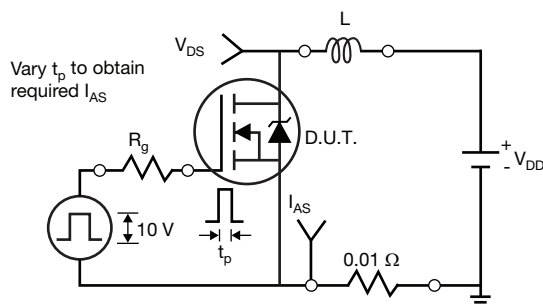
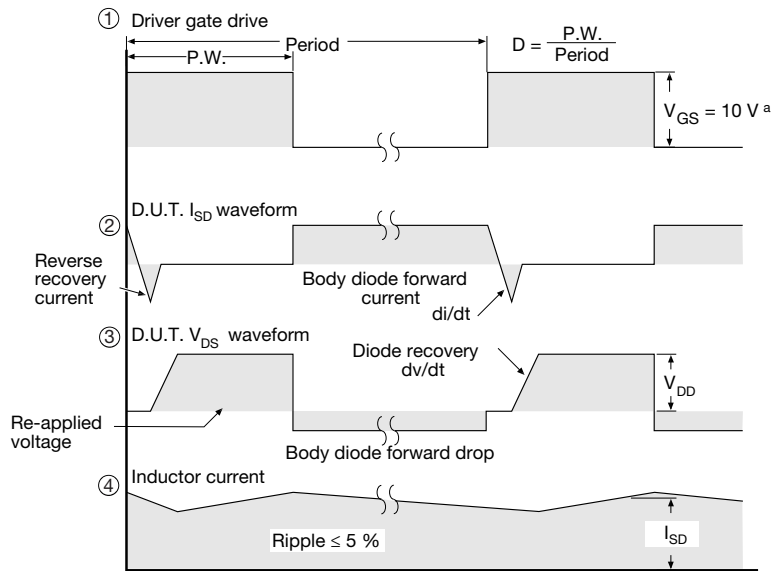
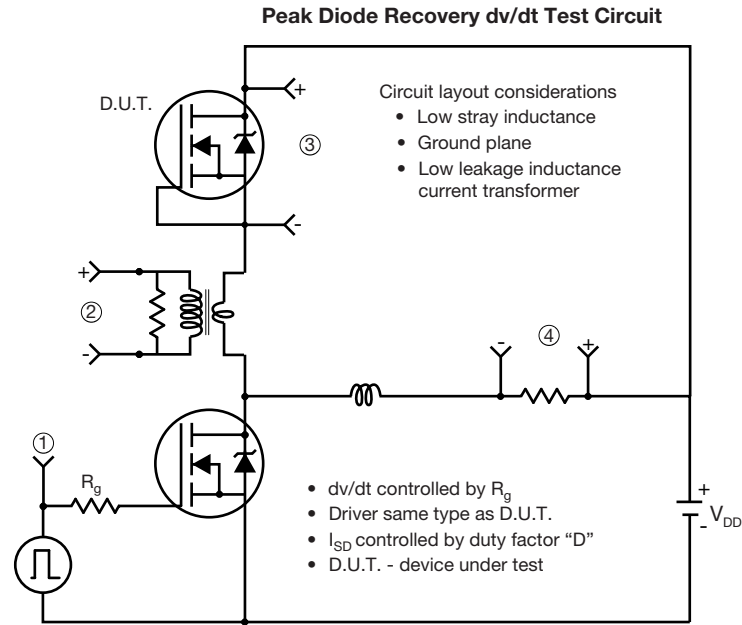


Fig. 15 - Unclamped Inductive Test Circuit



Fig. 18 - Gate Charge Test Circuit



Note
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 19 - For N-Channel

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TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
ØP	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: E21-0621-Rev. D, 04-Nov-2021
DWG: 6031

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



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