# SPICE Device Model SiHU4N80E



**Vishay Siliconix** 

# **E Series Power MOSFET**

### DESCRIPTION

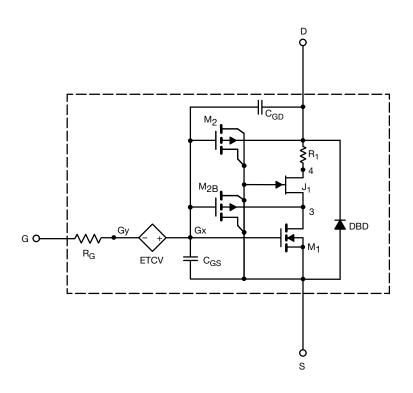
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over 25 °C to 150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### **CHARACTERISTICS**

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over 25 °C to 150 °C temperature range
- Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



#### Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits

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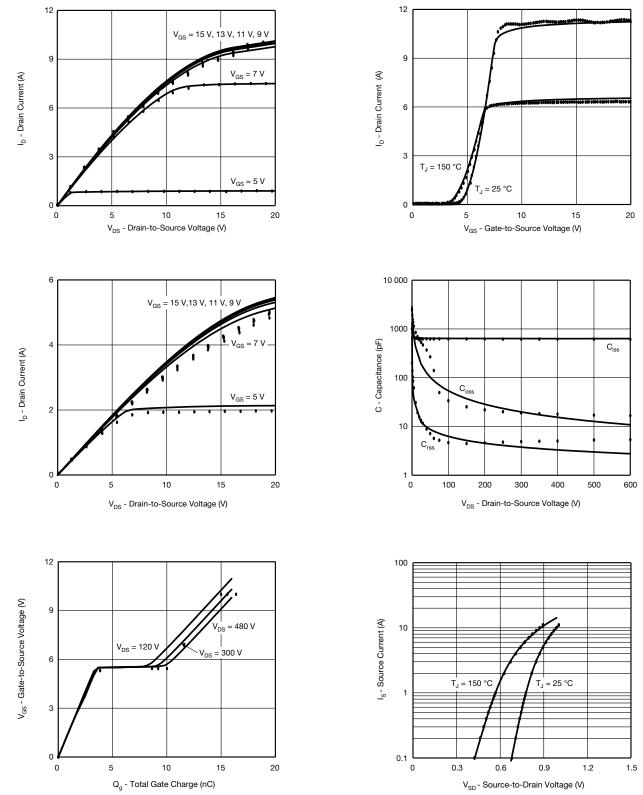
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<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	3	-	V
Drain-source on-state resistance	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 2 \text{ A}$	1.1	1.1	Ω
Forward transconductance	9 <sub>fs</sub>	$V_{DS} = 30 \text{ V}, \text{ I}_{D} = 2 \text{ A}$	2.5	1.5	S
Dynamic					
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, f = 1 MHz	639	622	pF
Output capacitance	C <sub>oss</sub>		55	34	
Reverse transfer capacitance	C <sub>rss</sub>		6	5	
Total gate charge	Qg	$V_{DS}$ = 480 V, $V_{GS}$ = 10 V, $I_{D}$ = 2 A	16	16	nC
Gate-source charge	Q <sub>gs</sub>		4	4	
Gate-drain charge	Q <sub>gd</sub>		6	6	
Drain-Source Body Diode Characteris	stics				
Reverse recovery time	t <sub>rr</sub>	$T_J = 25 \text{ °C}, I_F = I_S = 2 \text{ A},$ di/dt = 100 A/µs, V <sub>R</sub> = 25 V	260	248	ns
Reverse recovery charge	Q <sub>rr</sub>		3	1.4	μC



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### COMPARISON OF MODEL WITH MEASURED DATA (T<sub>J</sub> = 25 °C, unless otherwise noted)



#### Note

• Dots and squares represent measured data Copyright: Vishay Intertechnology, Inc.

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