

## E Series Power MOSFET

### DESCRIPTION

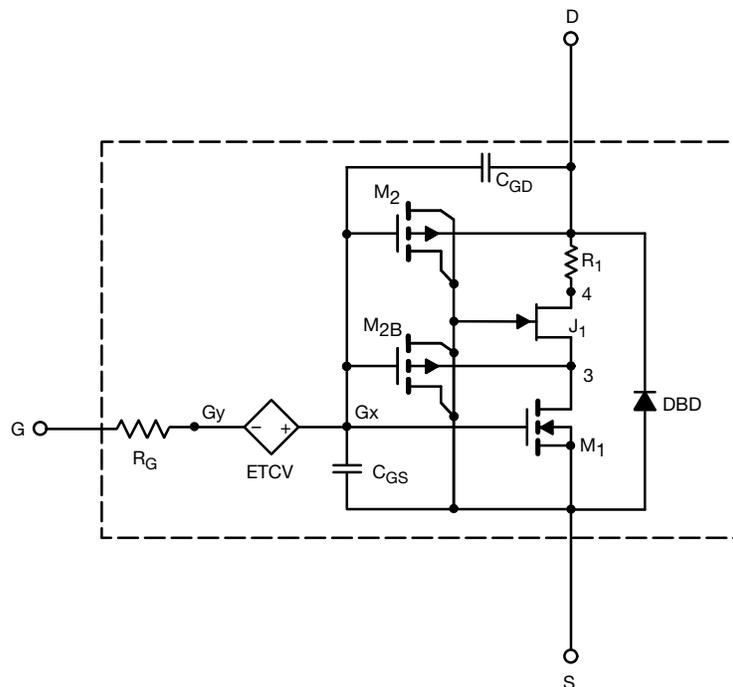
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over 25 °C to 150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over 25 °C to 150 °C temperature range
- Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



### Note

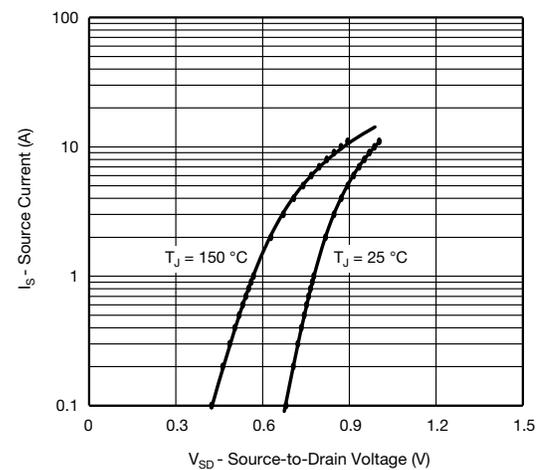
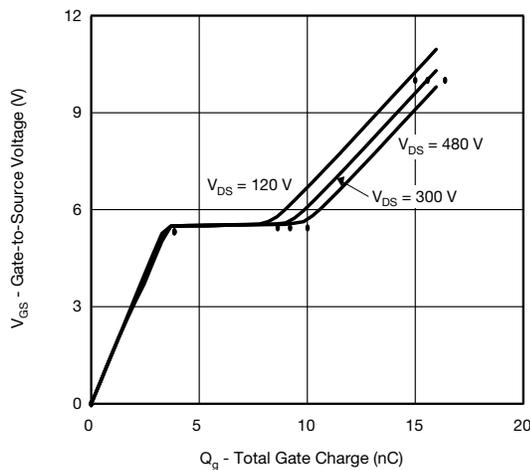
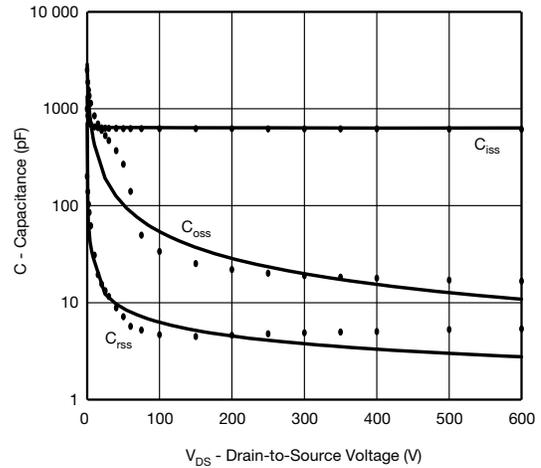
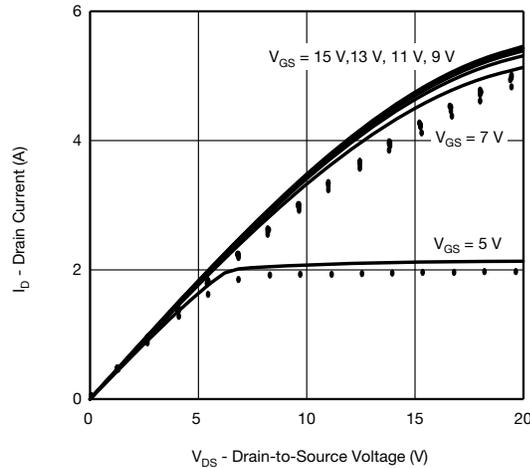
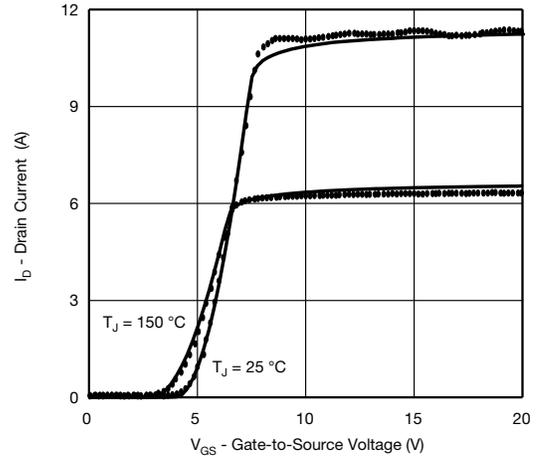
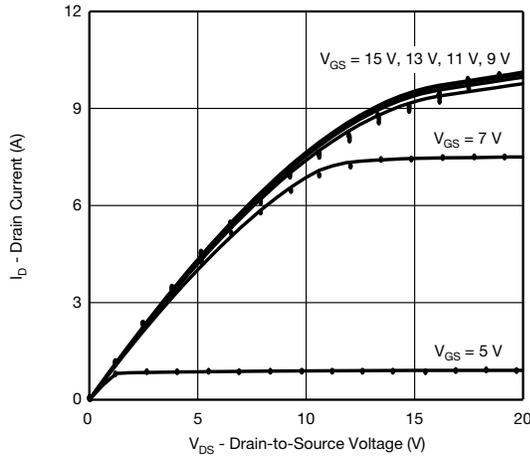
- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
<b>Static</b>					
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	-	V
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 2\text{ A}$	1.1	1.1	$\Omega$
Forward transconductance	$g_{fs}$	$V_{DS} = 30\text{ V}, I_D = 2\text{ A}$	2.5	1.5	S
<b>Dynamic</b>					
Input capacitance	$C_{iss}$	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	639	622	pF
Output capacitance	$C_{oss}$		55	34	
Reverse transfer capacitance	$C_{rss}$		6	5	
Total gate charge	$Q_g$	$V_{DS} = 480\text{ V}, V_{GS} = 10\text{ V}, I_D = 2\text{ A}$	16	16	nC
Gate-source charge	$Q_{gs}$		4	4	
Gate-drain charge	$Q_{gd}$		6	6	
<b>Drain-Source Body Diode Characteristics</b>					
Reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 2\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$	260	248	ns
Reverse recovery charge	$Q_{rr}$		3	1.4	$\mu\text{C}$



## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



### Note

- Dots and squares represent measured data

Copyright: Vishay Intertechnology, Inc.