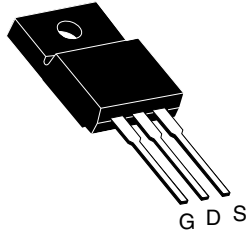


## EF Series Power MOSFET With Fast Body Diode

**TO-220 FULLPAK**


N-Channel MOSFET

### FEATURES

- A specific on resistance ( $m\Omega\text{-cm}^2$ ) reduction of 25 %
- Low figure-of-merit (FOM)  $R_{\text{on}} \times Q_g$
- Low input capacitance ( $C_{\text{iss}}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**

### PRODUCT SUMMARY

$V_{\text{DS}}$ (V) at $T_J$ max.	650	
$R_{\text{DS(on)}}$ typ. ( $\Omega$ ) at 25 °C	$V_{\text{GS}} = 10 \text{ V}$	0.084
$Q_g$ max. (nC)	134	
$Q_{\text{gs}}$ (nC)	16	
$Q_{\text{gd}}$ (nC)	48	
Configuration	Single	

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

### ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free and halogen-free	SiHF35N60EF-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25 \text{ }^\circ\text{C}$ , unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{\text{DS}}$	600	V
Gate-source voltage	$V_{\text{GS}}$	$\pm 30$	
Continuous drain current ( $T_J = 150 \text{ }^\circ\text{C}$ ) <sup>e</sup>	$V_{\text{GS}}$ at 10 V	$T_C = 25 \text{ }^\circ\text{C}$	A
		$T_C = 100 \text{ }^\circ\text{C}$	
Pulsed drain current <sup>a</sup>	$I_{\text{DM}}$	80	
Linear derating factor		2.0	W/ $^\circ\text{C}$
Single pulse avalanche energy <sup>b</sup>	$E_{\text{AS}}$	298	mJ
Maximum power dissipation	$P_{\text{D}}$	39	W
Operating junction and storage temperature range	$T_J, T_{\text{stg}}$	-55 to +150	$^\circ\text{C}$
Drain-source voltage slope	dv/dt	100	V/ns
Reverse diode dv/dt <sup>d</sup>		50	
Soldering recommendations (peak temperature) <sup>c</sup>	For 10 s	260	$^\circ\text{C}$
Mounting torque	M3 screw	0.6	Nm

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{\text{DD}} = 140 \text{ V}$ , starting  $T_J = 25 \text{ }^\circ\text{C}$ ,  $L = 28.2 \text{ mH}$ ,  $R_g = 25 \text{ } \Omega$ ,  $I_{\text{AS}} = 4.6 \text{ A}$
- 1.6 mm from case
- $I_{\text{SD}} = 17 \text{ A}$ ,  $di/dt = 300 \text{ A}/\mu\text{s}$ , starting  $T_J = 25 \text{ }^\circ\text{C}$
- Limited by maximum junction temperature



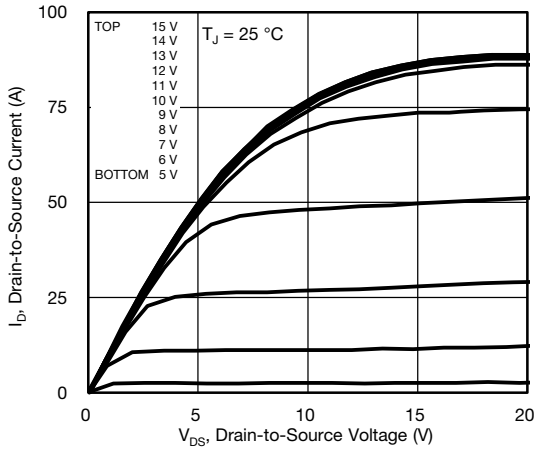
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R <sub>thJA</sub>	-	65	°C/W
Maximum junction-to-case (drain)	R <sub>thJC</sub>	-	3.2	

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		600	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 10 mA		-	0.66	-	V/°C
Gate-source threshold voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
		V <sub>GS</sub> = ± 30 V		-	-	± 1	μA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V		-	-	1	μA
		V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	500	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 17 A	-	0.084	0.097	Ω
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 17 A		-	8	-	S
<b>Dynamic</b>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1 MHz		-	2568	-	pF
Output capacitance	C <sub>oss</sub>			-	113	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	7	-	
Effective output capacitance, energy related <sup>a</sup>	C <sub>o(er)</sub>			-	81	-	
Effective output capacitance, time related <sup>b</sup>	C <sub>o(tr)</sub>	V <sub>DS</sub> = 0 V to 480 V, V <sub>GS</sub> = 0 V		-	421	-	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 17 A, V <sub>DS</sub> = 480 V	-	89	134	nC
Gate-source charge	Q <sub>gs</sub>			-	16	-	
Gate-drain charge	Q <sub>gd</sub>			-	48	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 17 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω		-	28	56	ns
Rise time	t <sub>r</sub>			-	85	170	
Turn-off delay time	t <sub>d(off)</sub>			-	96	192	
Fall time	t <sub>f</sub>			-	61	122	
Gate input resistance	R <sub>g</sub>	f = 1 MHz, open drain		0.2	0.5	1.0	Ω
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	32	A
Pulsed diode forward current	I <sub>SM</sub>			-	-	80	
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 17 A, V <sub>GS</sub> = 0 V		-	-	1.2	V
Reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 17 A, di/dt = 100 A/μs, V <sub>R</sub> = 400 V		-	150	300	ns
Reverse recovery charge	Q <sub>rr</sub>			-	1.1	2.2	μC
Reverse recovery current	I <sub>RRM</sub>			-	14	-	A

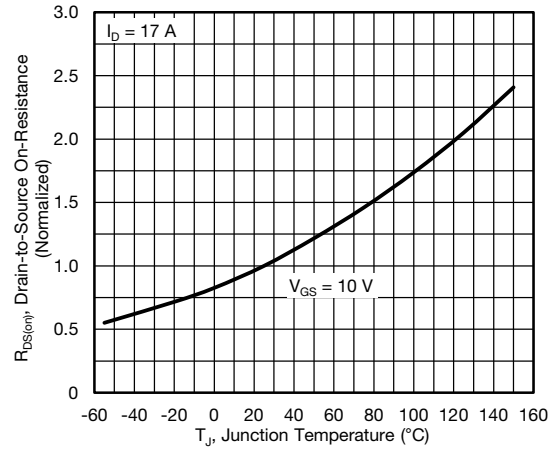
**Notes**

- a. C<sub>oss(er)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DSS</sub>
- b. C<sub>oss(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DSS</sub>

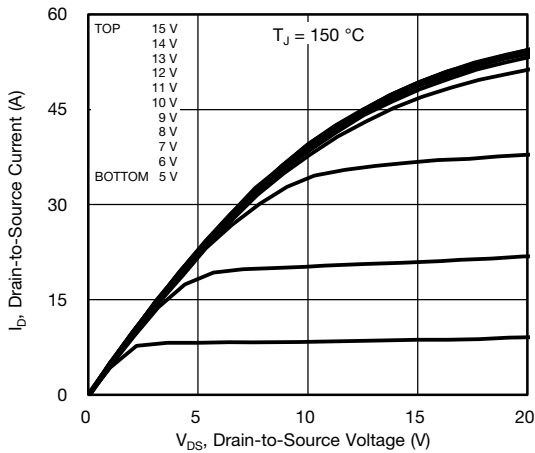
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



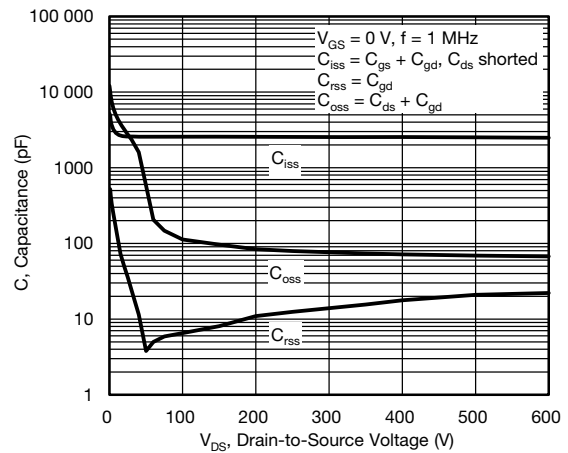
**Fig. 1 - Typical Output Characteristics**



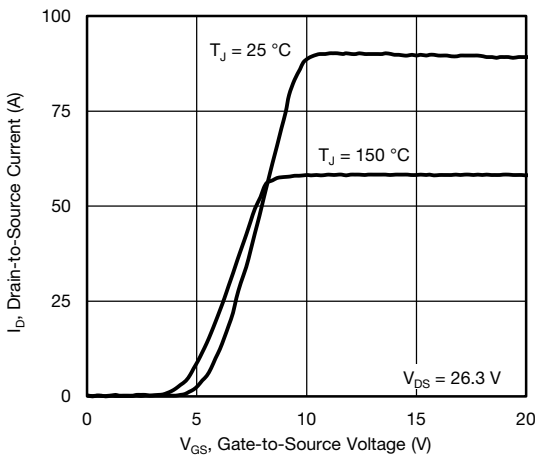
**Fig. 4 - Normalized On-Resistance vs. Temperature**



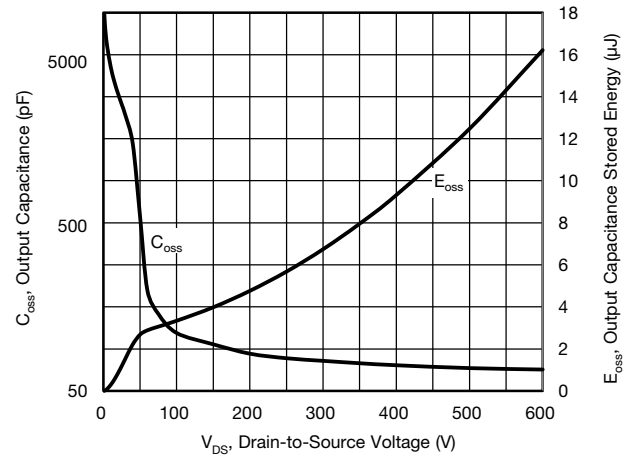
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**

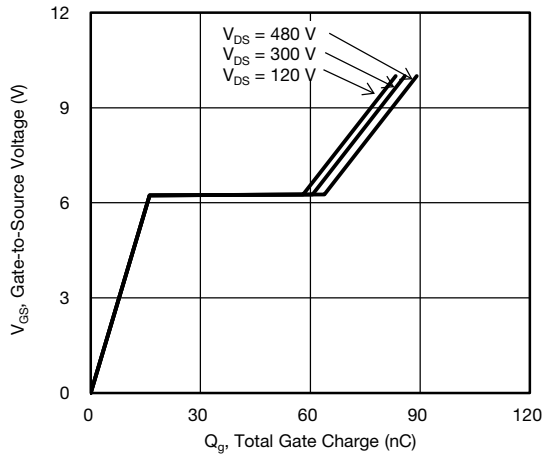


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

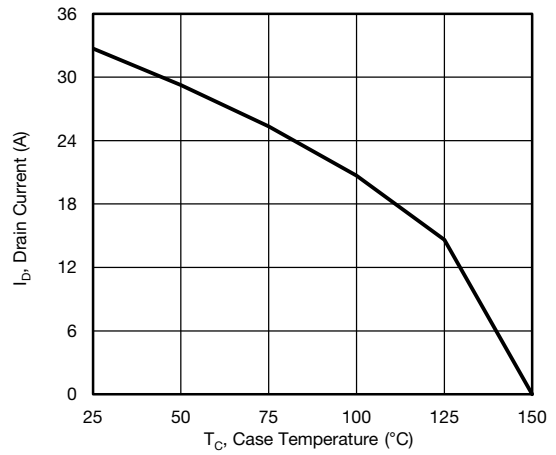


Fig. 10 - Maximum Drain Current vs. Case Temperature

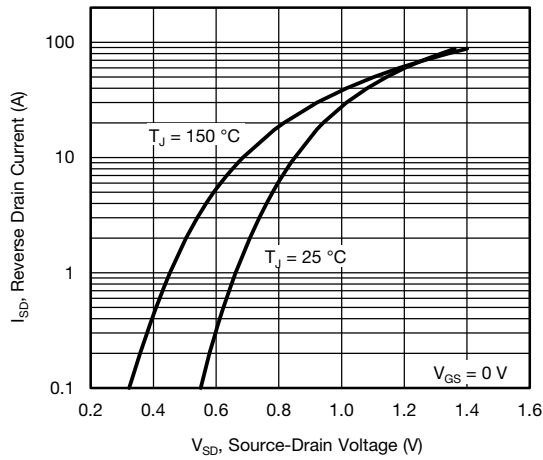


Fig. 8 - Typical Source-Drain Diode Forward Voltage

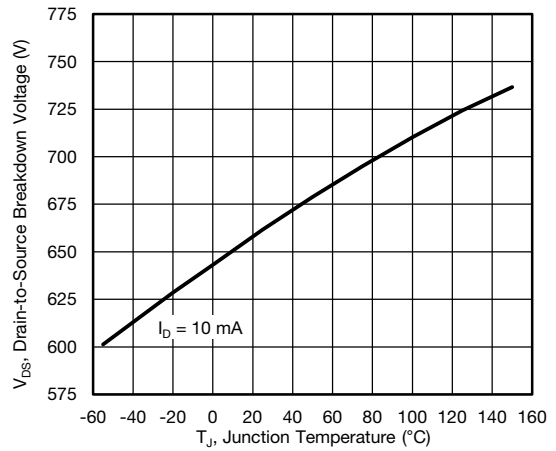


Fig. 11 - Temperature vs. Drain-to-Source Voltage

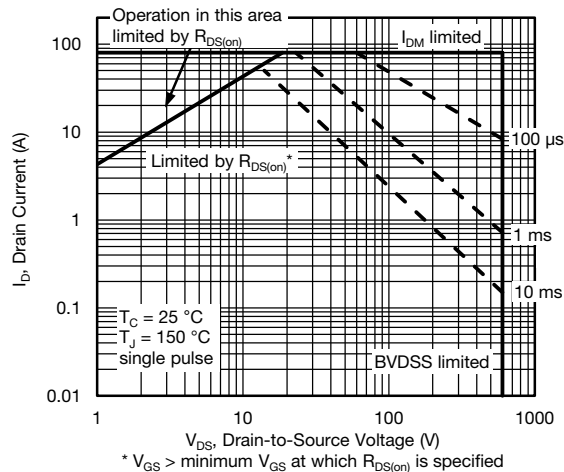


Fig. 9 - Maximum Safe Operating Area

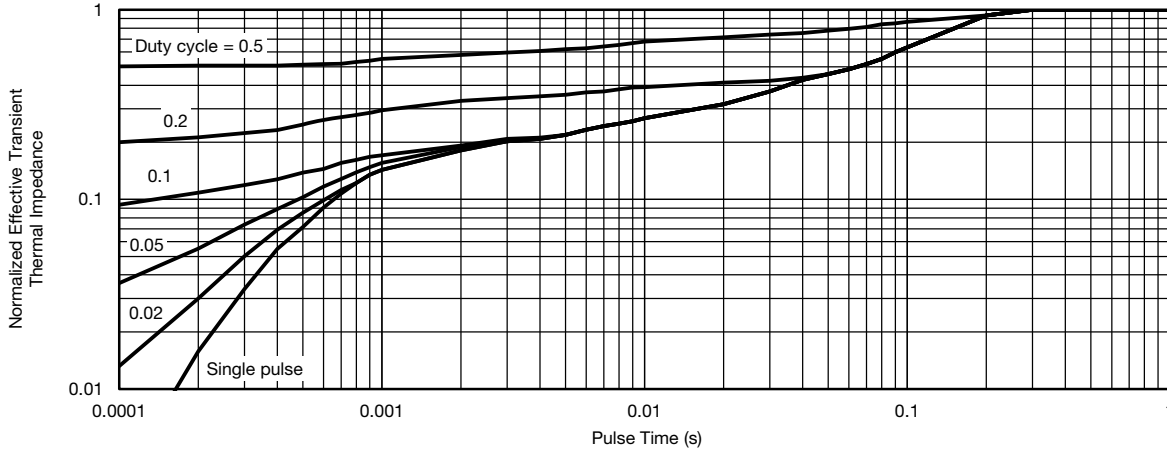


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case



Fig. 13 - Switching Time Test Circuit



Fig. 16 - Unclamped Inductive Waveforms



Fig. 14 - Switching Time Waveforms



Fig. 17 - Basic Gate Charge Waveform

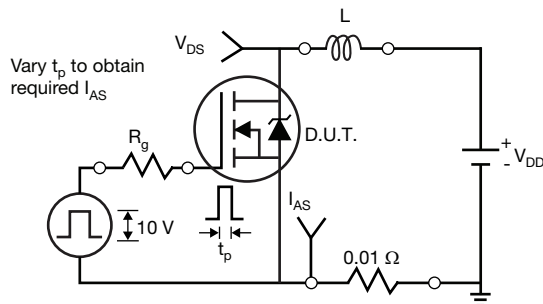
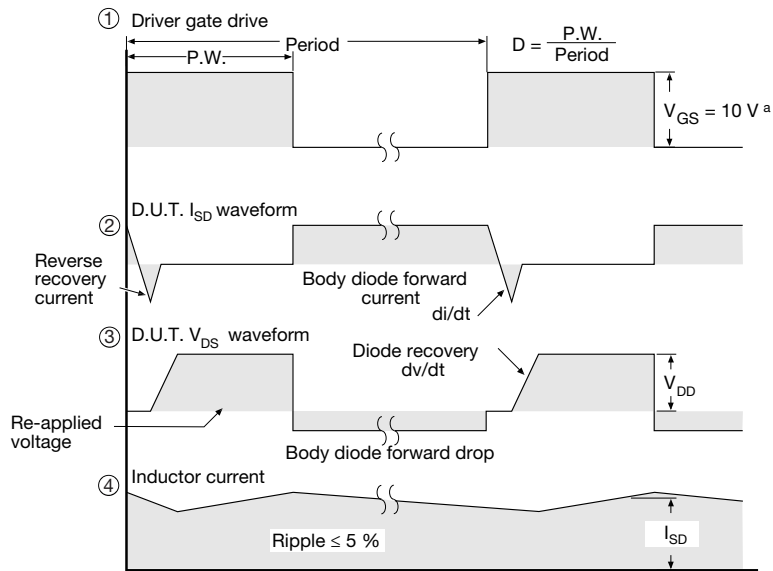


Fig. 15 - Unclamped Inductive Test Circuit



Fig. 18 - Gate Charge Test Circuit



**Note**  
a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 19 - For N-Channel**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon



*Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?92110](http://www.vishay.com/ppg?92110).*



# TO-220 FULLPAK (High Voltage)

## OPTION 1: FACILITY CODE = 9



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54 BSC		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
$\varnothing R$	3.08	3.18	3.28

### Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking





OPTION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020

ECN: E19-0180-Rev. D, 08-Apr-2019  
DWG: 5972

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking



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